Junu Kasim

As an engineer with 4 years of experience in physical design and 7 years in the semiconductor industry, I have developed strong analytical skills and growing technical expertise in integrated circuit design and development. I am eager to apply my knowledge and continue learning, with a focus on contributing to complex challenges and advancing technologies. I am open to opportunities across multiple areas, including digital design, mixed-signal design/verification, and application engineering, where I can leverage my experience to drive innovation and success.

Work Experience

• Master's Thesis 01/2024 - 02/2025
Infineon Technologies Villach, Austria

- Developed a state-of-the-art Hybrid Switched-Capacitor DC-DC buck converter topology for high voltage ratios, focusing on optimizing power efficiency.
- Designed gate drivers, level shifters in 130nm BCD technology. Performed simulations to optimize performance for various load-line values.
- Collaborated with cross-functional teams for topological validation using MATLAB/Simulink-Cadence/Spectre co-simulations.

• Research Assistant 04/2023 - 12/2023
Carinthia University of Applied Sciences Villach, Austria

- Contributed to a research team on analog layout automation, conducting literature reviews and porting frameworks to TSMC 65nm technology.
- Developed Python scripts for data analysis and automation using Jupyter Notebook.

• Physical Design Engineer 05/2018 - 09/2022
Synapse Techno Design Innovations Pvt. Ltd. Bangalore, India

- Handled multiple IP designs in various technology nodes like 55nm, 22nm, 14nm, 12nm, 7nm, 6nm, and 5nm.
- Led complete end-to-end design flow from RTL to GDSII for multiple projects, ensuring successful tape-outs.
- Collaborated with sign-off teams, resolved critical power issues, and performed physical verification like DRC, LVS, LEC, ERC, and Static Time Analysis (STA).
- Implemented functional and metal ECOs and addressed crosstalk and Electron Migration(EM) issues.
- Mentored and assisted junior engineers in their design work, providing guidance and facilitating their understanding of the PNR/APR flow.
- Developed small automation scripts using SKILL and TCL for PNR flow optimization and timing sign-off fixes.

Education

Masters in Integrated Systems and Circuits Design(M.Sc)
Carinthia University of Applied Sciences Villach, Austria
09/2022 - 02/2025

Bachelor of Engineering in Electronics and Communication(B.tech)
KMEA Engineering College Ernakulam, India
05/2013 - 06/2017

Contact

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Nationality: Indian
Date of Birth: 01/08/1995

Skills

- **Languages**: TCL, Python, Verilog, SystemVerilog, VHDL
- **EDA Tools**: Innovus, ICC2, PrimeTime, Calibre, Tempus, ModelSim, Synopsys Design Compiler (DC), Xilinx Vivado, SPICE, Mixed-mode simulation, Virtuoso, Spectre, Layout L, ADE.
- **Operating Systems**: Unix/Linux.

Master's Program Project

Integrating Dual Slope ADC

- Designed an integrating dual slope ADC as a part of the Master program.
- Complete mixed-signal IC development process for an ADC project, including concept development, analog and digital circuit design, Synthesis, Formal verification and layout using TSMC 65nm technology.
- Conducted post-fabrication testing and lab characterization of the chip.

Certification and Courses

PG Diploma in VLSI & Embedded Hardware Design
NIELIT Kozhikode, India
FPGA Architecture and Programming using Verilog HDL
NIELIT Kozhikode, India

Languages

- **English**:Full Professional Proficiency; strong verbal and written communication skills
- **German**: Goethe A1 Certificate (Basic Proficiency)