Analog IC Design Lab
COURSE PROJECT

Design and analysis of a 2-stage op-amp with high gain bandwidth product

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EEE - VLSI & Nanoelectronics

Contents

1 EXPERIMENT

Design a 2-stage Op-amp in 180 nm technology targeting different applications.

2 OBJECTIVE

Design and analyze a 2-stage op-amp with a high GainBandwidth with the Design specification mentioned below.

2.1 General Design Specifications

- **A Reference current source = 20µA.**
- **Supply voltage = 1.8V.**
- **Slew Rate $\geq$ 1 V/µs**
- **ICMR = 0.6-1.4 V**
- **Load Capacitance C_L = 10 pF**
- **Phase Margin $\geq$ 60 degrees**

2.2 High Gain Bandwidth Design Specifications

- **Gain $\geq$40dB**
- **GBW $\geq$ 70MHz**
- **Power Dissipation $\leq$ 1mW**
- **L $\leq$ 2μm**

3 2 STAGE OPAMP

The operational amplifier as the name suggests is an amplifier with a certain operation. Here a 2 stage opamp implies two kinds of amplifiers are cascaded such as to achieve the characteristics of both the amplifiers.

In this experiment, a differential amplifier is cascaded with a common source amplifier to achieve a high gain, and for high gain bandwidth product. A two-stage operational amplifier consists of a differential amplifier at the input stage, while the second stage is a high gain stage biased by the output of the differential amplifier. As explained before, a two-stage operational amplifier exhibits two poles below the unity open-loop gain. There is a sta-

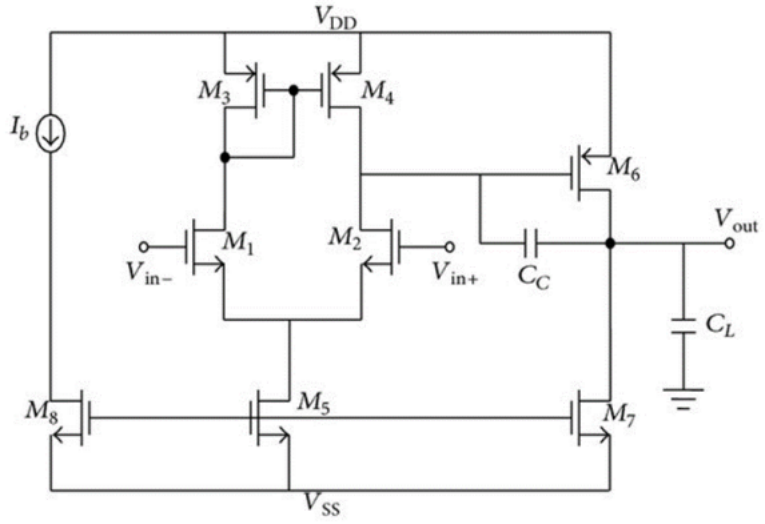

Figure 1: Circuit of 2 stage opamp

bility problem even though the two stages are compensated, when cascading the two stages, the circuit ends up with three high-impedance nodes. Consequently, two poles will be below the unit gain cross-over frequency, which will cause instability. Hence, introducing a single capacitor will dominate the other poles. So that the gain cross-over frequency will only be affected by one pole. The Poles and capacitance are known to be inversely proportional to each other. Therefore, a high capacitance must be introduced to create the dominating pole. To put it simply, we apply the Miller Theorem to one

capacitance. Therefore, it will offer a big capacitance with a little value, as Cc in the circuit above.

An amplifier's Gain Band Width Product is just the product of its Open Loop gain times the frequency range where its gain is reduced to -20 dB.

To calculate the suitable W/L ratio of each transistor in the above figure, the following process steps are used.

- Initially assuming a 60-degree phase margin and unity gain frequency is at least 10 times that of the provided gain bandwidth product. This assumption provides us with a miller capacitance of C_c at least $0.22C_L$.
- With the given slew rate which is the current through I5 over C_c, the current through MOSFET M5 is obtained.
- Using the gain bandwidth product, the gm for mosfet M1 is obtained which in turn provides us with the W/L ratio of M1 and M2 because both are symmetric.
- For the W/L ratio of M3 and M4, make use of the max ICMR as the gate voltage and use min ICMR to find the W/L ratio of M5.
- For M6, the gain bandwidth product is used such that the unity gain frequency is 10 times it. And since M6 and M4 are current mirrors the ratio of their aspect ratio is the same as the ratio of currents through them.
- similarly, M5 and M7 forms a current mirror.

4 2 stage OPAMP design

4.1 Design procedure

Step 1

Assuming that for a stable system, the phase margin is 60 degrees and zero frequency at greater than 5 times Gain Bandwidth product. So, by solving

the equation of one zero and two pole system, with the above Assumptions we got the equation,

$$C_c \geq 0.22C_L \tag{1}$$

They given C_L is 10 pF.so we got miller capacitance is

$$C_c > 2.2pF \tag{2}$$

Step 2

This design focuses on the high gain bandwidth of a two-stage opamp. One of the provided design parameters specified that the power *leq* 1mW and reference current source is 20µA.

$$power \leq 1 * 10^{-3}W$$
$$1.8 * (I_{ref} + I_5 + I_7) \leq 10^{-3}$$
$$I_5 + I_7 \leq 535.55\mu A$$

Fixing I_5 is 80µA and I_7 is 440µA.

Step 3

$$slew - rate = \frac{I_5}{C_c} \tag{3}$$

Given slew rate minimum 1V/μs. Assumed the slew rate to be 20V/μs.

$$C_c = 4pF \tag{4}$$

Step 4

The gain bandwidth product is the voltage unit gain frequency. Because there is a dominant pole, there will be a 20dB decay at unit gain frequency.

$$gm_1 = 2\pi * GBW * C_c \tag{5}$$

then gm_1 is

$$gm_1 = 1759.291\mu A \tag{6}$$

with

$$gm_1 = \sqrt{2I_d\mu_n C_{ox}\frac{W}{L}_1} \tag{7}$$

substituting the values in the above equation then

$$\frac{W}{L}_1 = 113.066 = \frac{W}{L}_2 \tag{8}$$

Step 5

maximum ICMR is 1.4V. In the above circuit, for M1 to be in saturation

$$V_{d1} > V_g - V_{th1} \tag{9}$$

$$V_g < (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L} 3}}) + Vth1 \tag{10}$$

here gate voltage is the maximum ICMR voltage. Substituting all the values

$$ICMRmax > (Vdd - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L} 3}}) + Vth1 \tag{11}$$

$$\frac{W}{L}_3 = \frac{W}{L}_4 > 3.6448 \tag{12}$$

Step 6

ICMR minimum is 0.4V. For all transistors to be in saturation.

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L} 1}} - Vthn \tag{13}$$

substituting all the values,

$$V_{dast} = 0.0045V \tag{14}$$

But the minimum overdrive voltage should be 0.1V, V_{dsat} is assumed as 0.1V, then substituting the value in the current equation

$$\frac{W}{L}_5 = 46.76 \tag{15}$$

Step 7

M6 and M4 are in the current mirror.

$$\frac{(W/L)_6}{(W/L)_4} = \frac{I_6}{I_4} \tag{16}$$

this gives

$$\frac{W}{L}_6 = 40.095 \tag{17}$$

Step 8

$$\frac{(W/L)_7}{(W/L)_5} = \frac{I_7}{I_5} \tag{18}$$

M6 and M7 are in series so both currents are equal.

$$(W/L)_7 = 257.175 \tag{19}$$

and since both M5 and M8 form a current mirror with a ratio of currents 4:1.

$$(W/L)_8 = 11.69 \tag{20}$$

Now that all the (W/L) ratios have been found, individual transistor lengths are to be calculated. Since the optimization to be done on obtaining high bandwidth implies that the circuit is a high-frequency circuit. For high-frequency circuits, the design is done on minimum lengths so the length of transistors is considered as 360nm. Gain of two two-stage opamp is

$$gain = gm_1 gm_2 (r01||r04)(ro6||ro7) \tag{21}$$

5 RESULTS AND CONCLUSIONS

5.1 DC ANALYSIS

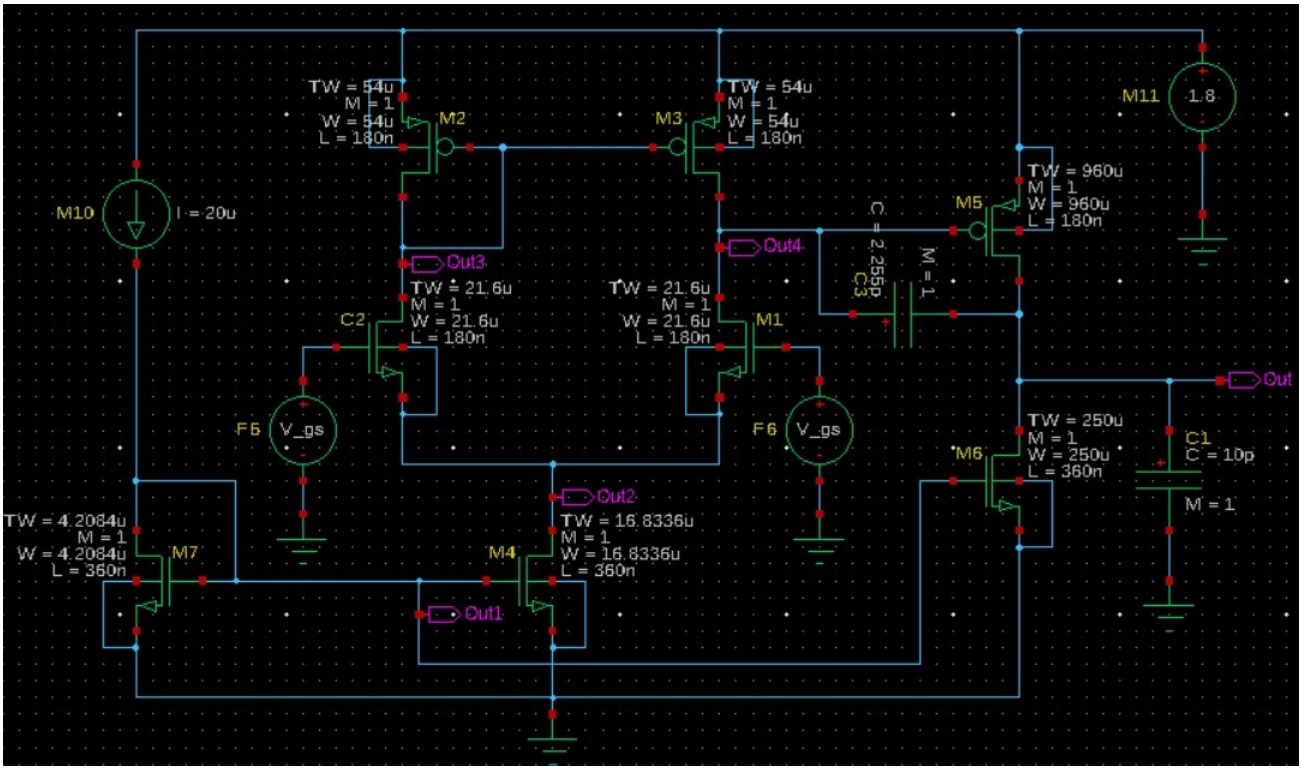

Figure 2: schematic of DC analysis

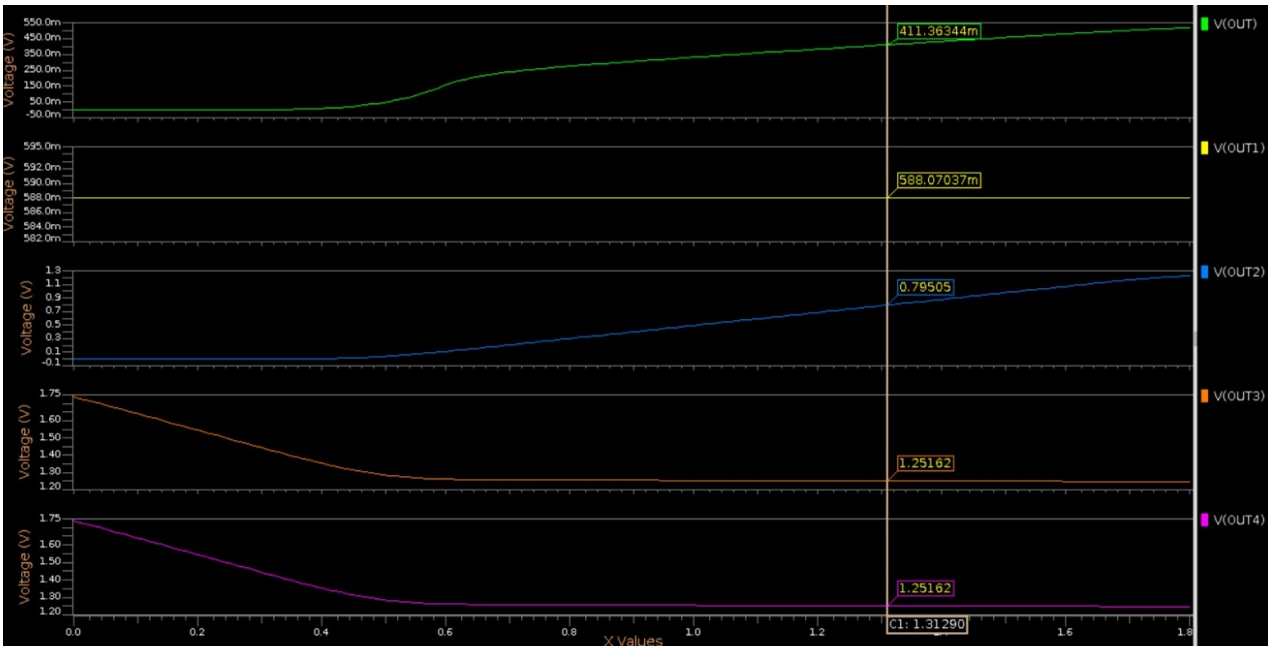

Figure 3: Operating Point for transistors in saturation

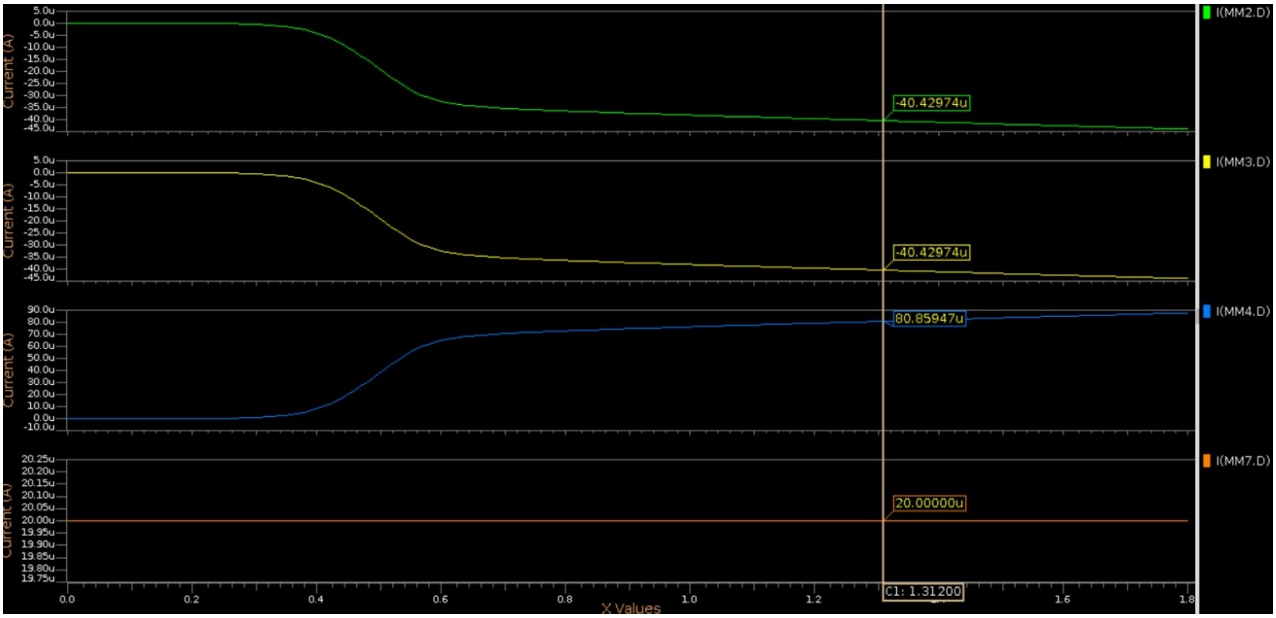

Figure 4: Operating Point for transistors in saturation

5.2 AC ANALYSIS

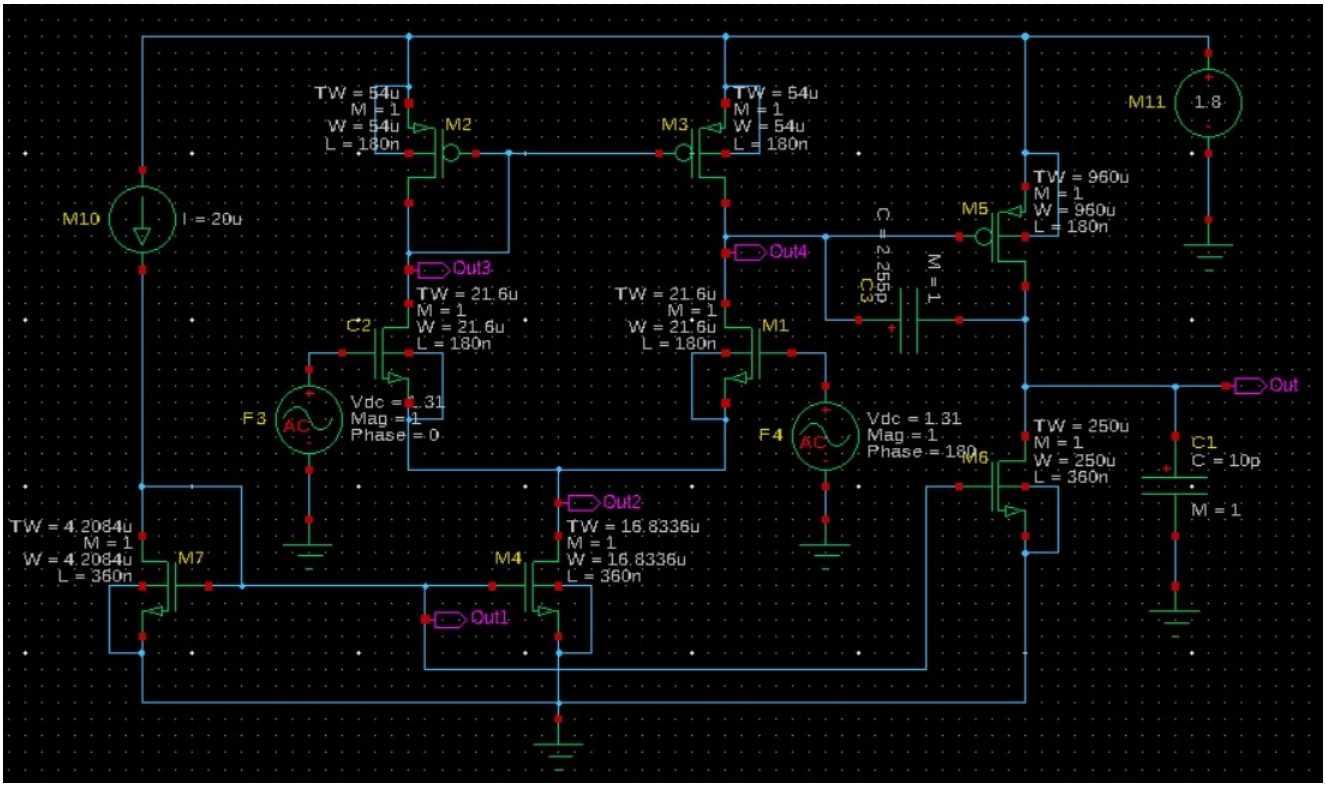

Figure 5: schematic of AC analysis

- **To find the common mode gain, the same input is applied at both ends of the input. Then AC analysis is done to find the gain.**
- **To find PSRR the AC input is applied in place of Vdd, dc bias is applied at the input gate of the transistors and one branch input is connected to the output. AC analysis is then done and gain is found out.**

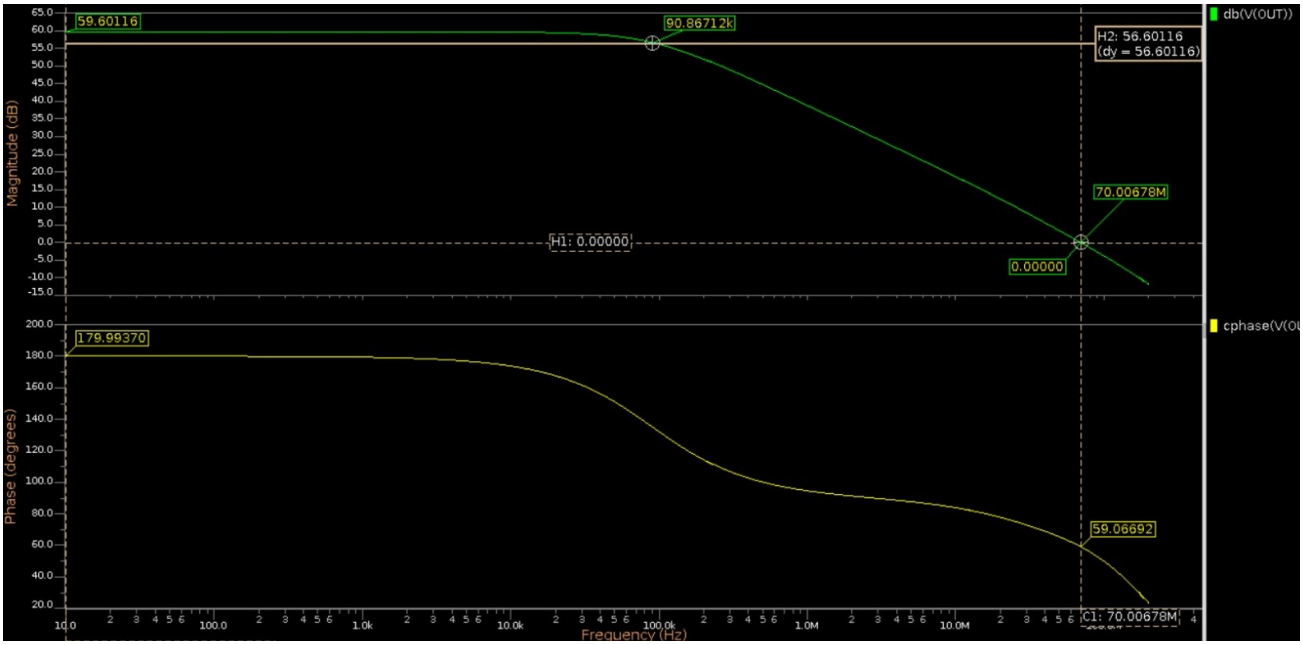

Figure 6: Gain, Bandwidth, Unity gain frequency and phase margin

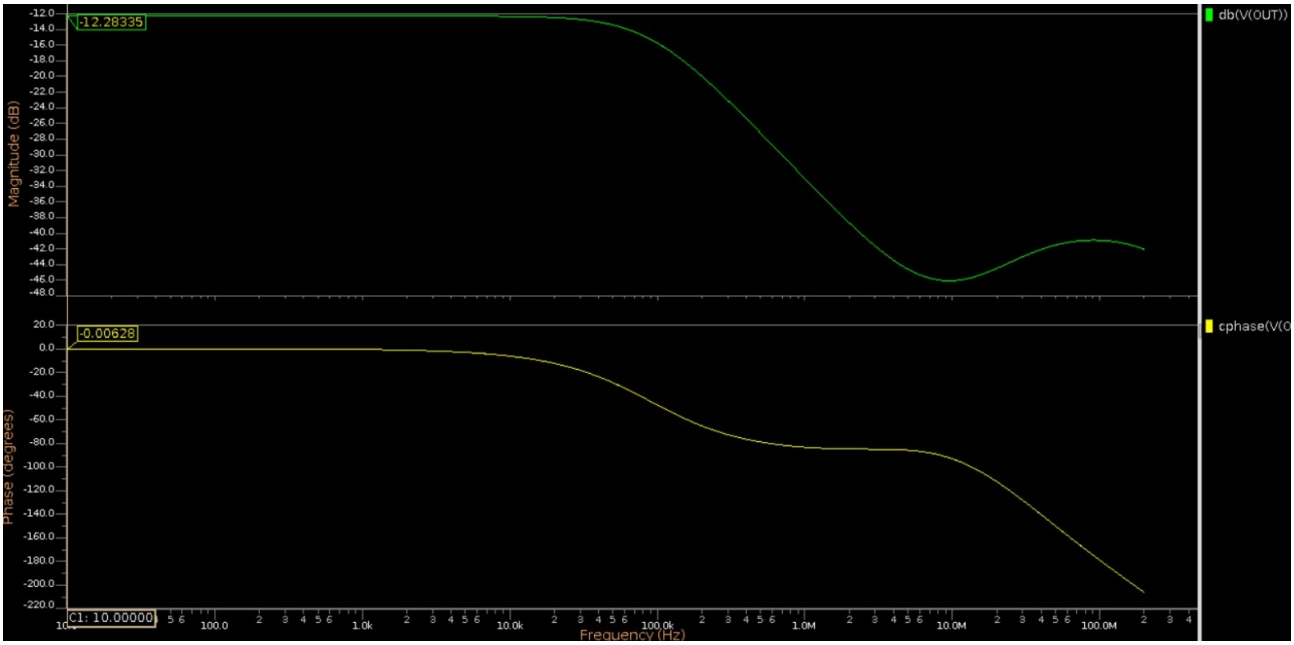

Figure 7: Common Mode Gain

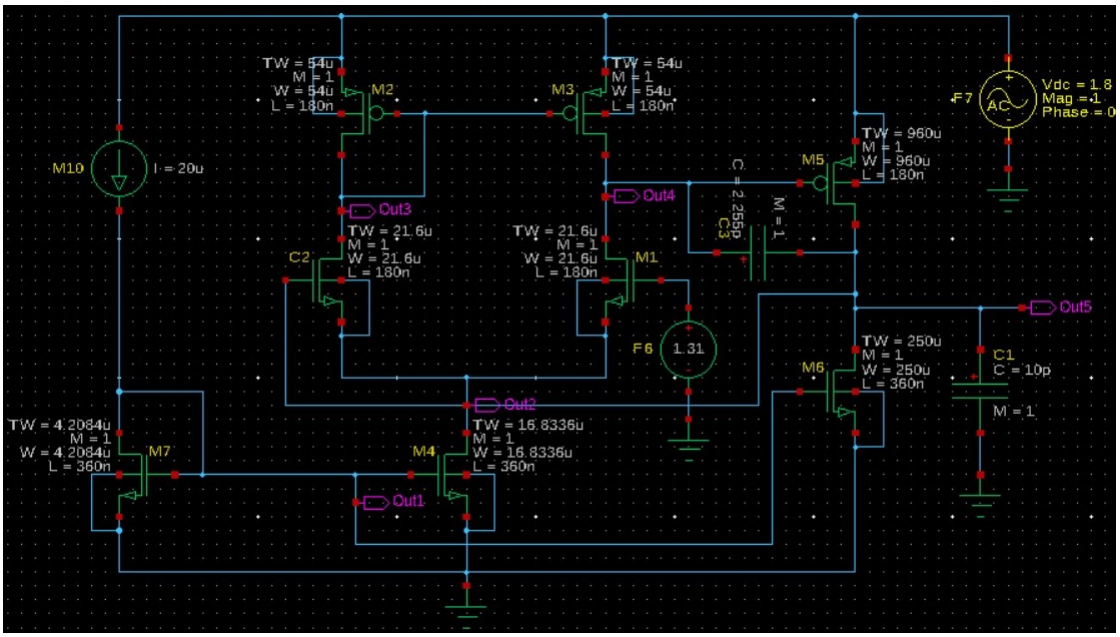

Figure 8: schematic of PSRR in AC analysis

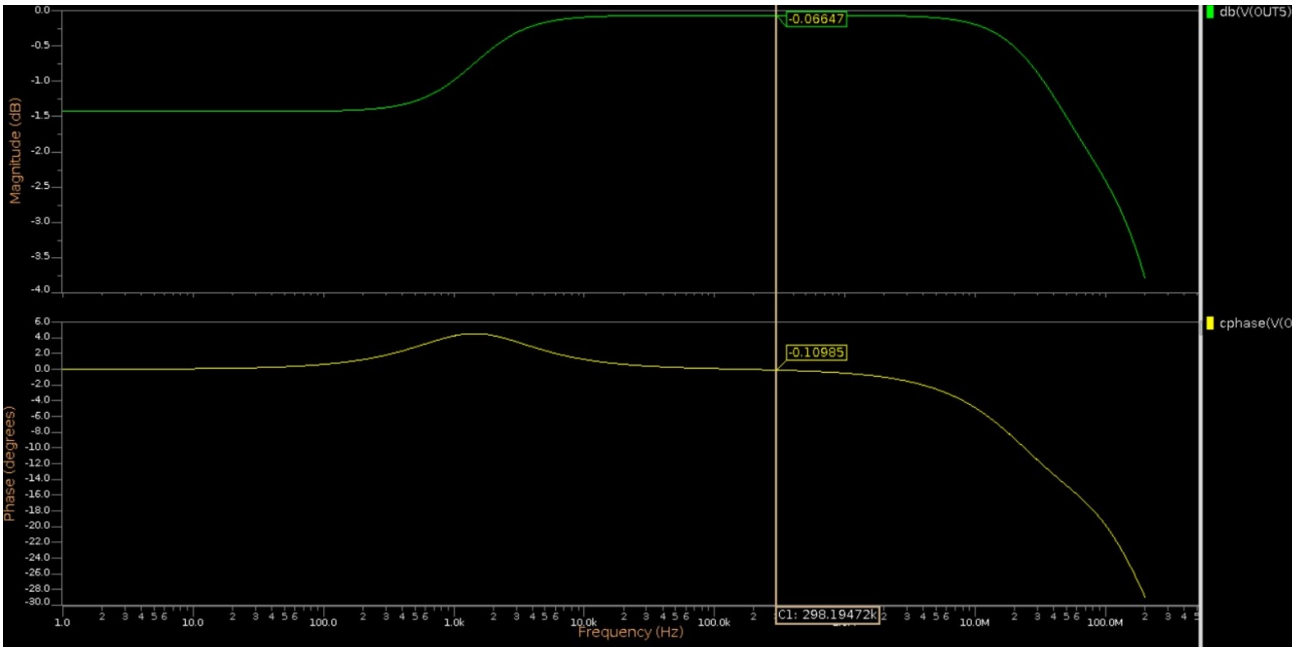

Figure 9: Plot to measure PSRR

5.3 TRANSIENT ANALYSIS

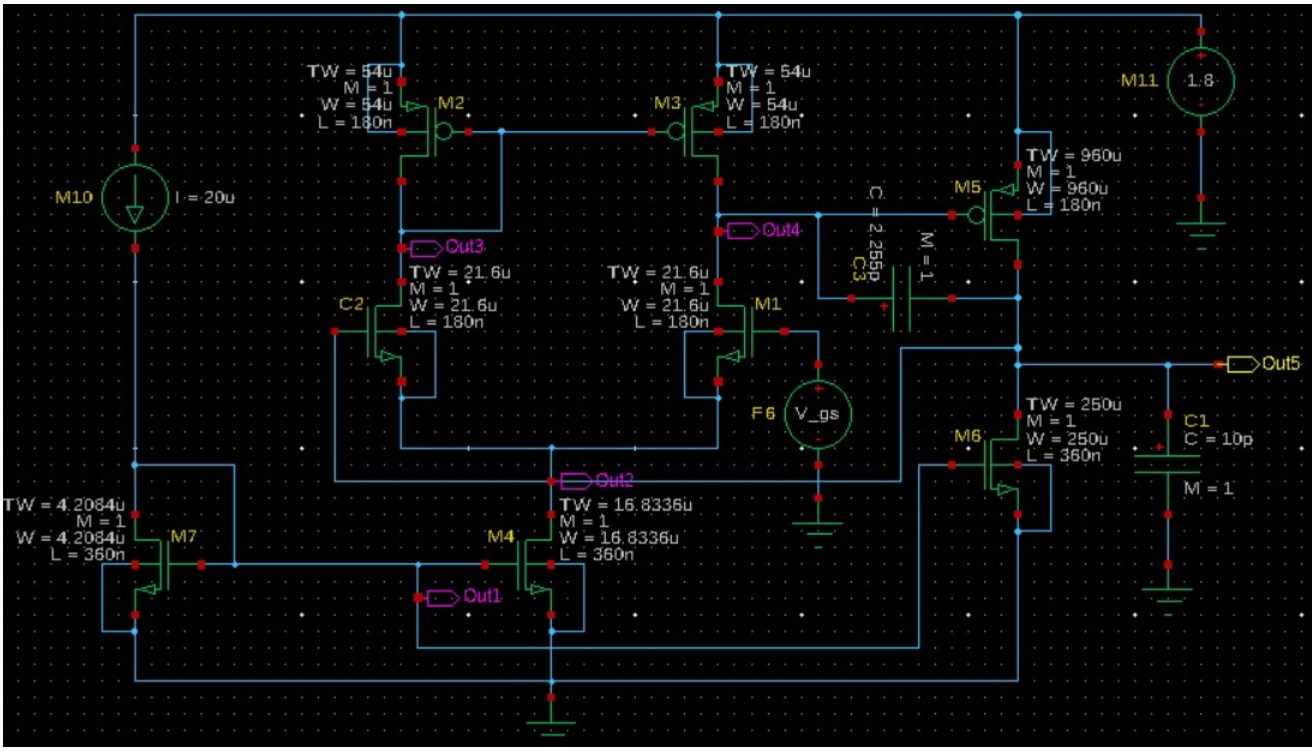

Figure 10: schematic of ICMR/OCMR analysis

- **For ICMR and OCMR, The branch in which the output is sensed will be connected to the output, and a DC sweep is done to find the minimum to maximum input and minimum to maximum output.**
- **For Slew Rate, for a maximum slew rate the entire current should flow through only a single branch.; For that, a square pulse is input at one end and the other is grounded. Transient analysis is done then the max difference in output in a period gives the slew rate of the design im[plemented]**

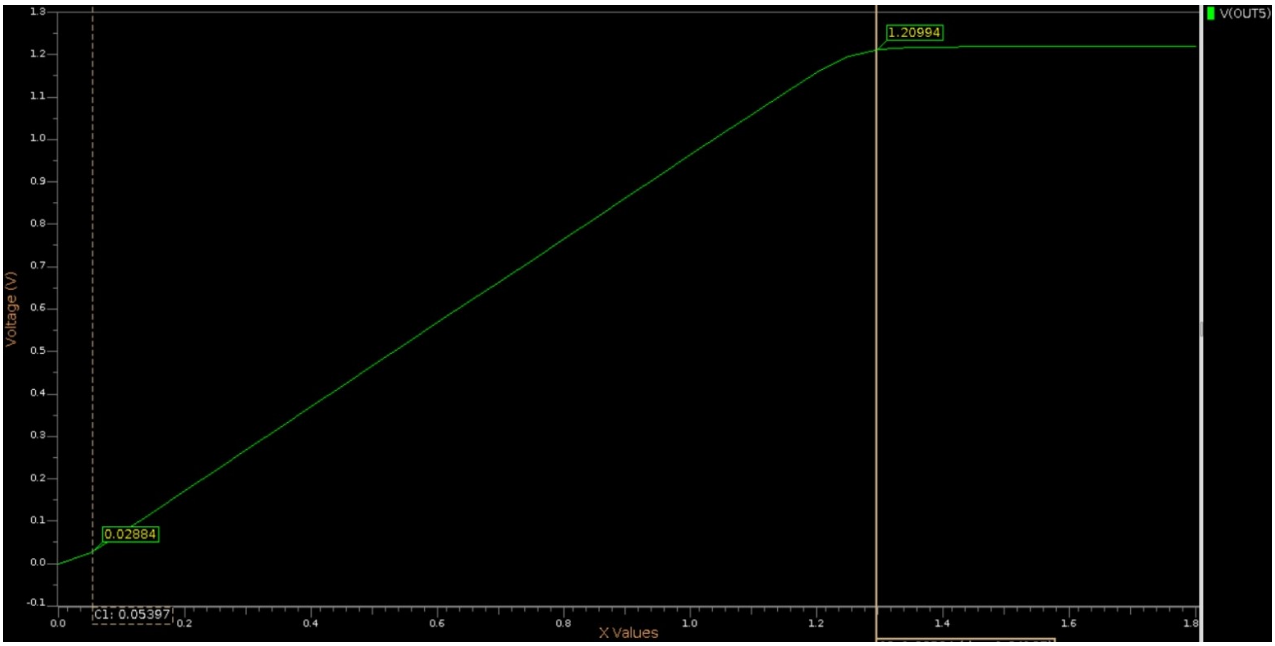

Figure 11: Plot for ICMR and OCMR

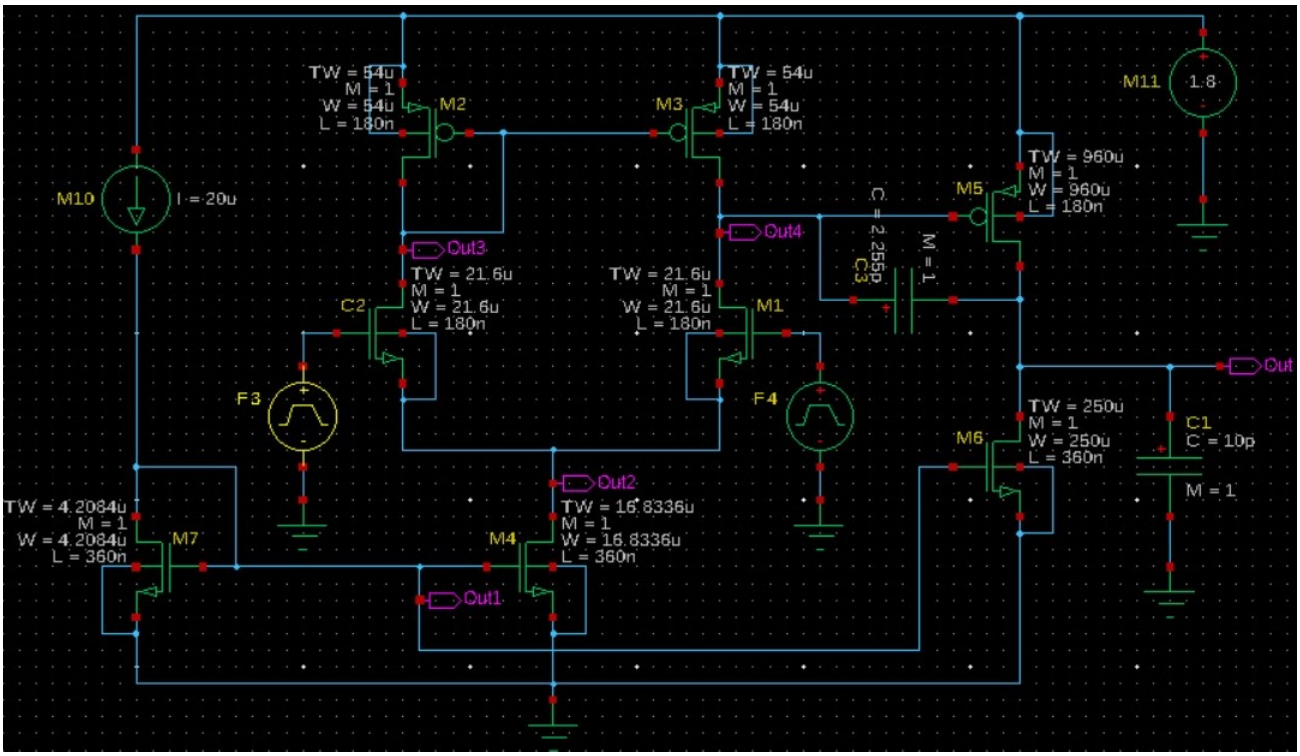

Figure 12: Schematic for Slew Rate

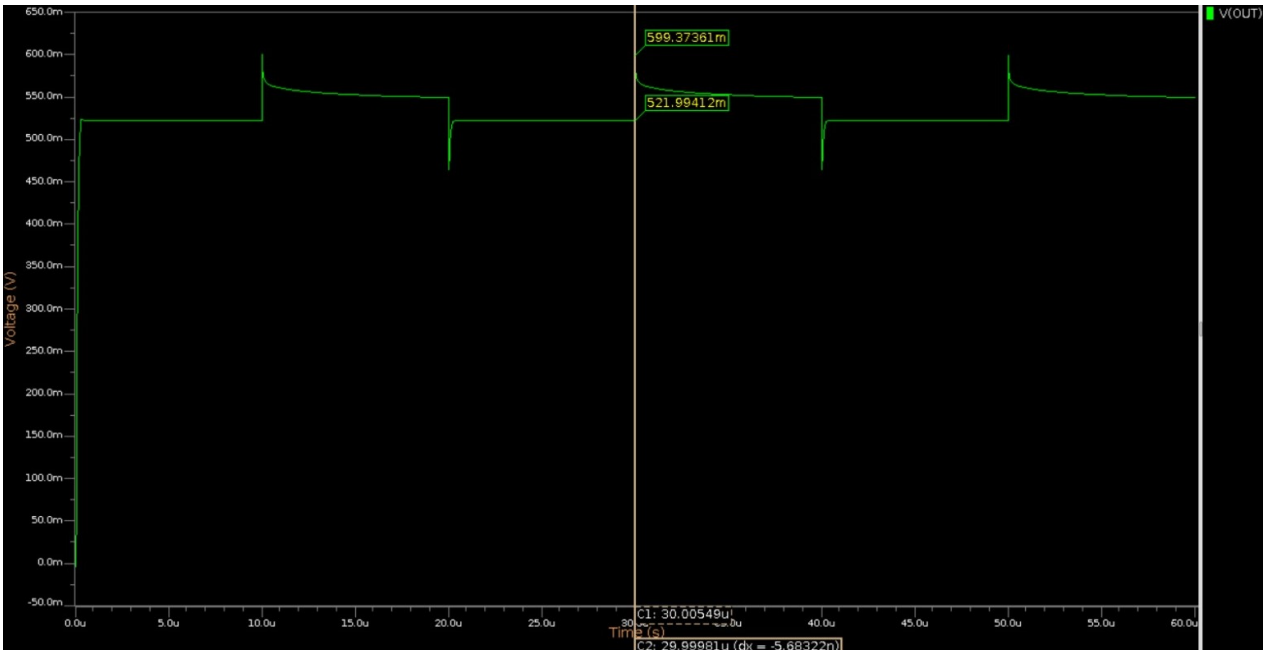

Figure 13: Plot for Slew Rate

Table 1: Aspect Ratios of each transistor and capacitances used in the circuit

Transistor	W/L ratio
M1	2160 nm/180 nm
M2	2160 nm/180 nm
M3	54000 nm/180 nm
M4	54000 nm/360 nm
M5	16833 nm/360 nm
M6	960 um/180 nm
M7	250 um/360 nm
M8	4.208 um/360 nm

Capacitor	Value
C_C	2.255 pF
C_L	10 pF

Variable	Theoretical	Practical
Gain	40dB	59.6dB
Gain-Bandwidth	70 MHz	70.00678 MHz
CMRR		-12.28dB
PSRR		-0.066dB
Phase-Margin	60	59.066
Bandwidth		90.867 kHz
ICMR		0.058-1.29V
OCMR		0.028-1.2V
Slew Rate	1 V/μs	13.615 V/μs

Table 2: Comparison between theoretical and experimental Values obtained

6 CONCLUSIONS

- Designed and implemented 2-stage opamp with high gain bandwidth.
- The assumption that the phase margin is 60 degrees is satisfied.
- Possible minimum lengths taken to achieve high gain bandwidth.
- The Practical value of C_c is taken smaller than the theoretical to achieve high GBW and optimal phase margin as these parameters are inversely proportional to it.
- Results obtained match with theoretical values.