Analog IC Design Lab Experiment 7

Design and Analysis of fully Differential Telescopic OP-AMP circuit



Submitted by,
Bodepu Kasi Viswanadham Naidu
Roll No - 234102411

EEE - VLSI & NANOELECTRONICS

Contents

1	EXPERIMENT	2
2	OBJECTIVE	2
3	DESIGN SPECIFICATIONS	2
4	THEORY 4.1 DIFFERENTIAL TELESCOPIC OP-AMP	2 3
5	DESIGN PROCEDURE AND SIMULATIONS 5.1 Design	5 5
6	RESULTS AND CONCLUSIONS 6.1 DC ANALYSIS	9
7	CONCLUSIONS	15

1 EXPERIMENT

Analysis, and design of fully differential telescopic OP-AMP circuits.

2 OBJECTIVE

To obtain a maximum output swing, maximum gain, higher bandwidth, & lower power consumption with a suitable aspect ratio.

3 DESIGN SPECIFICATIONS

- The target design gain is \geq 60 dB.
- The design should have a GBW \geq 200 MHz.
- Power dissipation $\leq 10 \text{ mW}$
- Slew rate $\geq 50 \text{ V/}\mu\text{S}$

4 THEORY

SLEW RATE

Slew Rate is defined as the maximum rate of output change per micro-second. To determine that in this experiment or in differential amplifiers the maximum output is when the total tail current flows through one of its branches. It is given by

$$SR = \frac{dV_{out}}{dt}|_{max} \tag{1}$$

ICMR

This abbreviation expands to the Input Common Mode Range. It is the range of input in the common node that can be applied so that all the transistors in the circuit are in saturation.

CMRR

It is the Common Mode Rejection Ratio and is defined as the ratio of differential gain to that of common mode gain. This should be as high as possible as it needs to eliminate the common mode signal.

$$CMRR = \frac{A_d}{A_c} \tag{2}$$

PSRR

It is the power supply rejection ratio. PSRR determines the ability of the circuit to maintain the same output voltage with variation in supply voltage. This should also be high.

$$PSRR = \frac{\delta V_{DD}}{\delta V_{out}} \tag{3}$$

4.1 DIFFERENTIAL TELESCOPIC OP-AMP

Single-stage telescoping Op-amps have limited output swings and can be difficult to sort inputs and outputs. This issue can be mitigated by employing folded

However, cascode Op-amps have higher power dissipation, lower voltage gain, and lower pole frequencies. To use these two single-stage topologies, we use a tiny tail current to increase gain and a broad swing cascode setup to generate a huge output swing.

Fully differential amplifiers offer advantages such as increased output voltage swing and noise immunity, reduced even order harmonics, and high output dynamic range.

Fully differential telescopic opamps are more power-efficient than fully differential folded cascade opamps. To avoid overshooting, we chose a differential output stage with a simple design and aim to keep the tail device modest.

Cascode layouts can boost the voltage gain of CMOS transistor amplifier stages. This type of op-amp is known as a telescopic-cascode because the cascodes are linked in series with the transistors in the differential pair. This

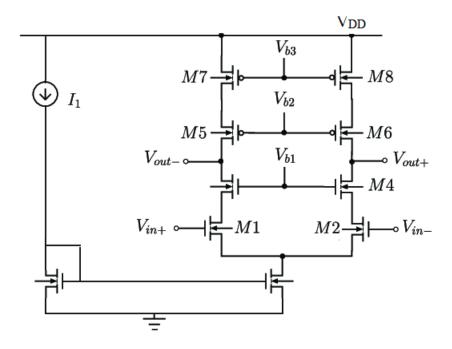


Figure 1: Circuit of a Fully Differential Telescopic OPAMP

results in a straight-line connection between the transistors in each branch of the circuit.

In this circuit, there is two branches for differential input and output. In each branch, there is a cascode that is two stacks of nmos and pmos to provide for high output swing. The gain is given by

$$Gain = -g_{mn}(g_{mn}r_{dsn}^2||g_{mp}r_{dsp}^2)$$
 (4)

5 DESIGN PROCEDURE AND SIMULA-TIONS

5.1 Design

Power Dissipation

The power dissipation is given to be ≤ 10 mW. This shows the current driven by the supply voltage.

$$(I_1 + I_{M9})V_{DD} = 10mW (5)$$

With $V_{DD} = 1.8$ V, The total current is obtained to be 5.55mA. By that $I_{M9} = 5$ mA and $I_1 = 0.5$ mA. Now that the current in the current mirror is known, the ratio between their aspect ratios is

$$\frac{(W/L)_9}{(W/L)_{10}} = 10\tag{6}$$

Bias Voltage

It is asked to design a high-swing implies that

$$2(V_{DD} - (V_{OD7} + V_{OD5} + V_{OD3} + V_{OD1} + V_{OD9})) = 1.8$$
$$V_{OD7} + V_{OD5} + V_{OD3} + V_{OD1} + V_{OD9} = 0.9$$

Assuming the overdrive voltage for each transistor in a branch, if the transistor has more current it has more overdrive voltage.

$$V_{0D9} = 0.3V$$

$$V_{0D7} = 0.2V$$

$$V_{0D5} = 0.2V$$

$$V_{0D3} = 0.1V$$

$$V_{0D1} = 0.1V$$

Using these overdrive voltages, the aspect ratios can be found with the MOS-FET saturation current equation. The 4 nmos stack is identical and all 4

pmos are identical. This gives

$$(\frac{W}{L})_{M1} = (\frac{W}{L})_{M2} = (\frac{W}{L})_{M3} = (\frac{W}{L})_{M4} = 1461.29$$

$$(\frac{W}{L})_{M5} = (\frac{W}{L})_{M6} = (\frac{W}{L})_{M7} = (\frac{W}{L})_{M8} = 912$$

$$(\frac{W}{L})_{M9} = 325$$

$$(\frac{W}{L})_{M10} = 32.5$$

From the overdrive voltages and current, the gate voltage of each MOSFET is known. This gives

$$V_{G1} = V_{G2} = 0.862V$$

$$V_{G3} = V_{G4} = 1V$$

$$V_{G5} = V_{G6} = 0.9V$$

$$V_{G1} = V_{G2} = 1.064V$$

Bandwidth with slew rate

Slew Rate $\geq 50\mu$, implies

$$\frac{I_{M9}}{C_L} = slewRate$$

$$\Longrightarrow C_L \le 100pF$$
 and
$$GBW = \frac{g_m}{2\pi C_L} = 200MHz$$

$$\Longrightarrow C_L \le 30pF$$

TransConductance And Gain

Since minimum-length MOSFETs are being used. The transconductance for nmos and pmos can be found out by

$$g_m = \frac{2I_d}{V_{GS} - V_t}$$

The transconductance of nmos and pmos is

$$g_{mn} = 50m\Omega^{-1}$$
$$g_{mp} = 25m\Omega^{-1}$$

6 RESULTS AND CONCLUSIONS

6.1 DC ANALYSIS

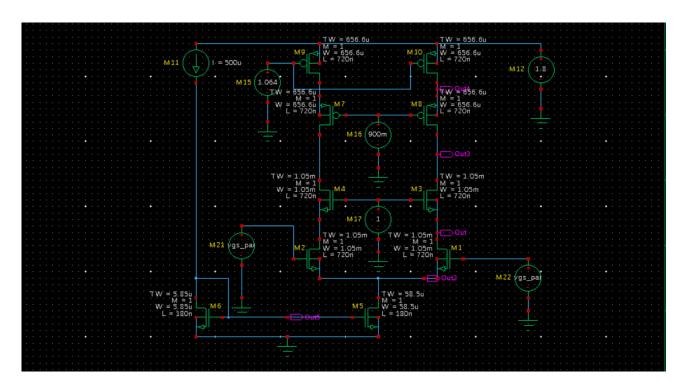


Figure 2: schematic of DC analysis

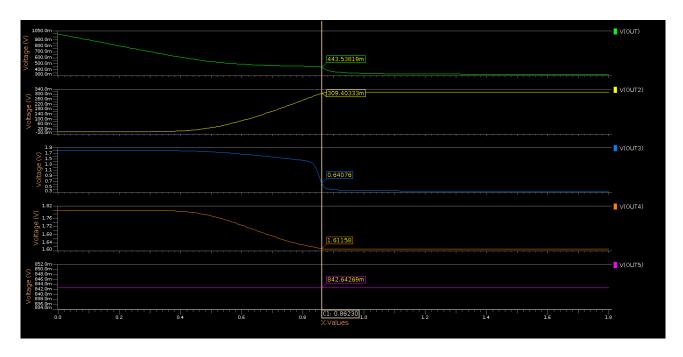


Figure 3: Operating Point for transistors in saturation

6.2 AC ANALYSIS

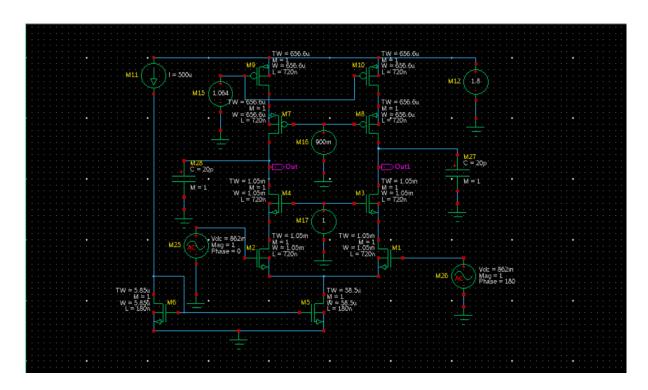


Figure 4: schematic of AC analysis

- To find the common mode gain, the same input is applied at both ends of the input. Then AC analysis is done to find the gain.
- To find PSRR the AC input is applied in place of Vdd, dc bias is applied at the input gate of the transistors and one branch input is connected to the output. AC analysis is then done and gain is found out.

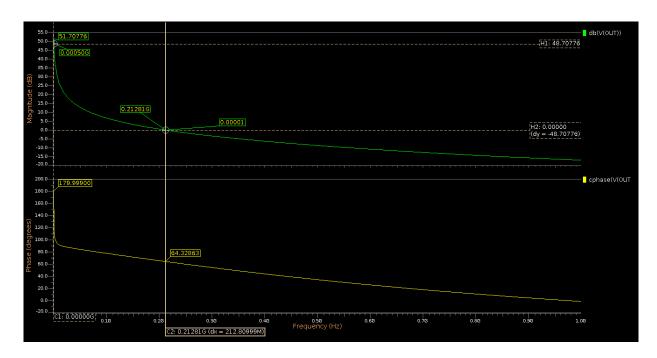


Figure 5: Gain, Bandwidth, Unity gain frequency and phase margin

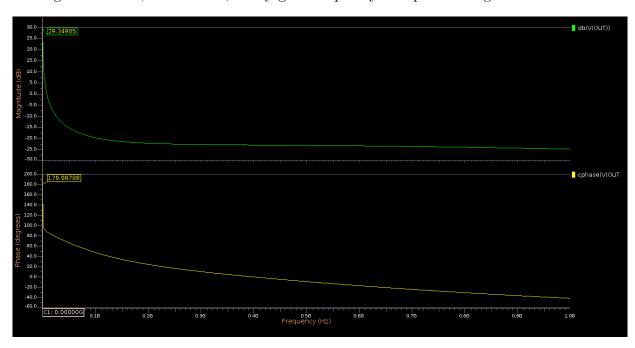


Figure 6: Common Mode Gain

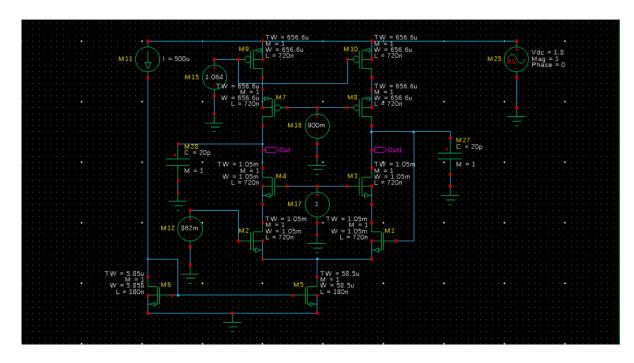


Figure 7: schematic of PSRR in AC analysis $\,$

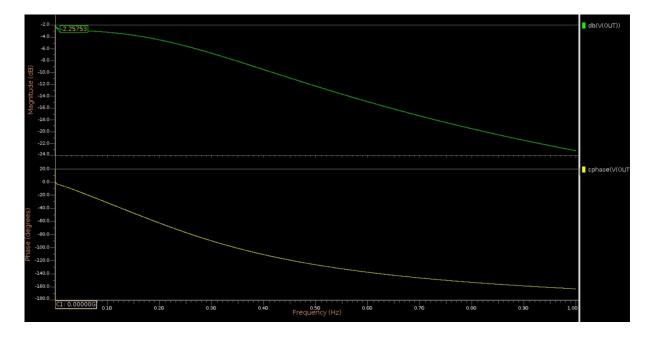


Figure 8: Plot to measure PSRR

6.3 TRANSIENT ANALYSIS

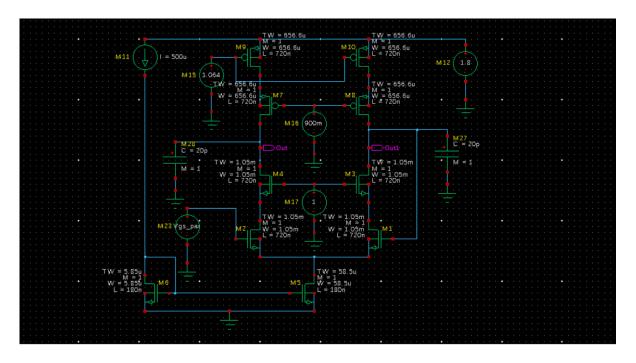


Figure 9: schematic of ICMR/OCMR analysis

- For ICMR and OCMR, The branch in which the output is sensed will be connected to the output and a DC sweep is done to find the minimum to maximum input and minimum to maximum output.
- For Slew Rate, for a maximum slew rate the entire current should flow through only a single branch.; For that, a square pulse is input at one end and the other is grounded. Transient analysis is done then the max difference in output in a period gives the slew rate of the design im[plemented]

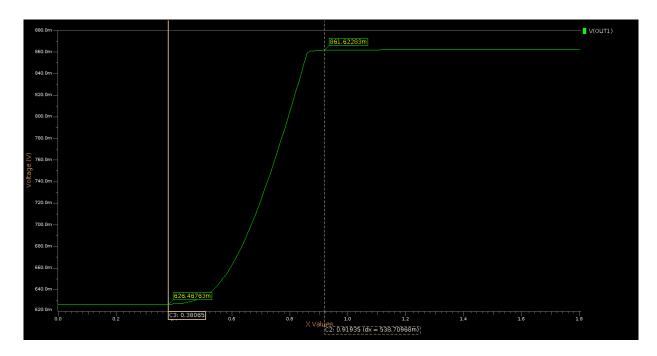


Figure 10: Plot for ICMR and OCMR $\,$



Figure 11: Operating Point for transistors in saturation

RESULTS

MOSFET	ASPECT RATIO	m W/L
M1, M2, M3 & M4	1462	1.05 m / 720 n
M5, M6, M7 & M8	912	$655\mu/720n$
M9	325	$58.5\mu/180n$
M10	33	$5.85\mu/180n$

Table 1: W/L ratios of every transistor

MOSFET	V_G	V_{GS}	V_{DS}	I_d
M1, M2	0.862 V	0.553 V	0.134 V	2.1mA
M3, M4	1 V	0.577V	0.197 V	2.1mA
M5, M6	0.9 V	-0.711V	-0.970V	-2.1mA
M7, M8	1.064V	-0.736V	-0.189V	-2.1mA
M9, M10	0.842V	0.842V	0.309V	4.2mA
M10	0.842V	0.842V	0.842V	4.2mA

Table 2: Bias Voltages' of every transistor $\,$

Variable	Theoretical	Practical
Gain	60 dB	51.707 dB
Bandwidth	-	$0.50~\mathrm{MHz}$
GBW	200 MHz	212 MHz
PM	-	64.32
CMRR	-	29.34 dB
PSRR	=	-2.25 dB

Table 3: Results obtained in AC analysis $\,$

Variable	Theoretical	Practical
Slew Rate	$50 \text{ V/}\mu\text{s}$	$88.24 \text{ V}/\mu\text{s}$
ICMR	-	0.538 V
OCMR	-	0.235 V

Table 4: Results obtained in Transient analysis

7 CONCLUSIONS

- Designed and Implemented a telescope amplifier with high gain and high swing.
- Due to the high current through the MOSFETs and relatively low overdrive voltages the aspect ratio came out to be very high.
- This high current implies that the resistance in the tail is much less hence the CMRR is less.