Indian Institute of Information Technology, Sri City, Chittoor
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Analog to Digital and Digital to Analog Converters

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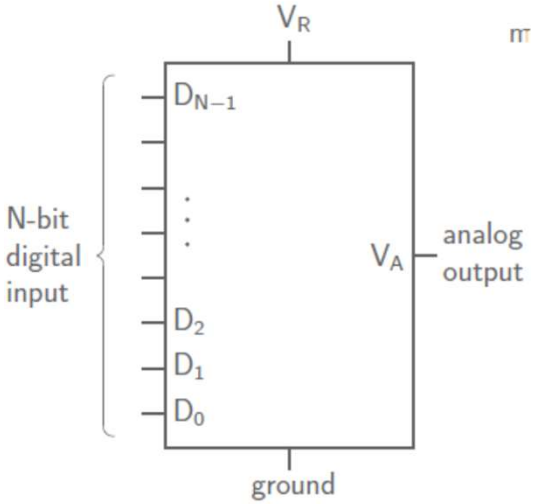
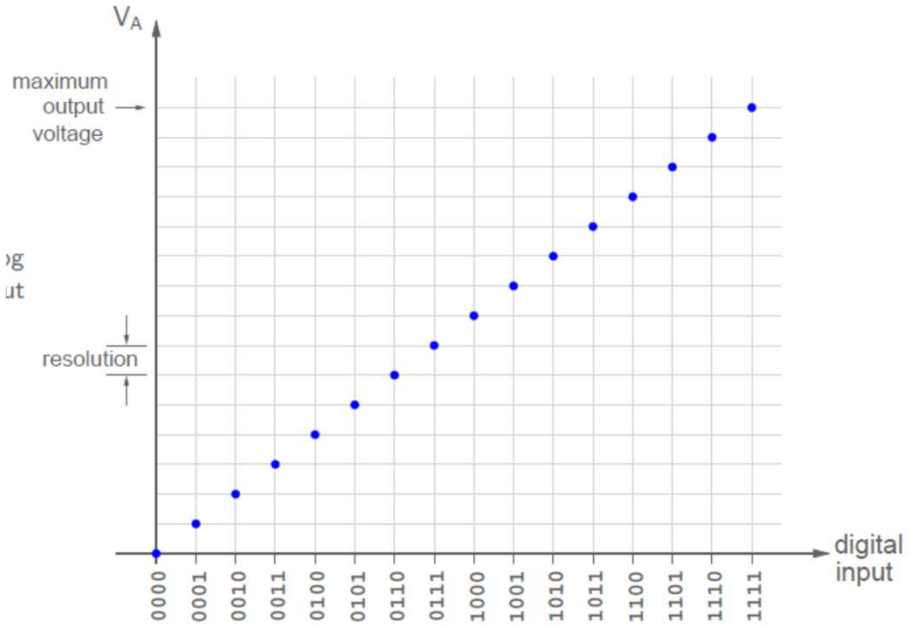
Introduction

- Physical quantities (e.g., Temparature, a voltage or a speech signal) are analog analog in nature, varying continuously with time.
- Digital format offers several advantages: digital signal processing, storage, use of computers, robust transmission, etc.
- An ADC (Analog-to-Digital Converter) is used to convert an analog signal to the digital format.
- The reverse conversion (from digital to analog) is also required. For example, music stored in a DVD in digital format must be converted to an analog voltage for playing out on a speaker.
- A DAC (Digital-to-Analog Converter) is used to convert a digital signal to the analog format.

Digital to Analog Converters

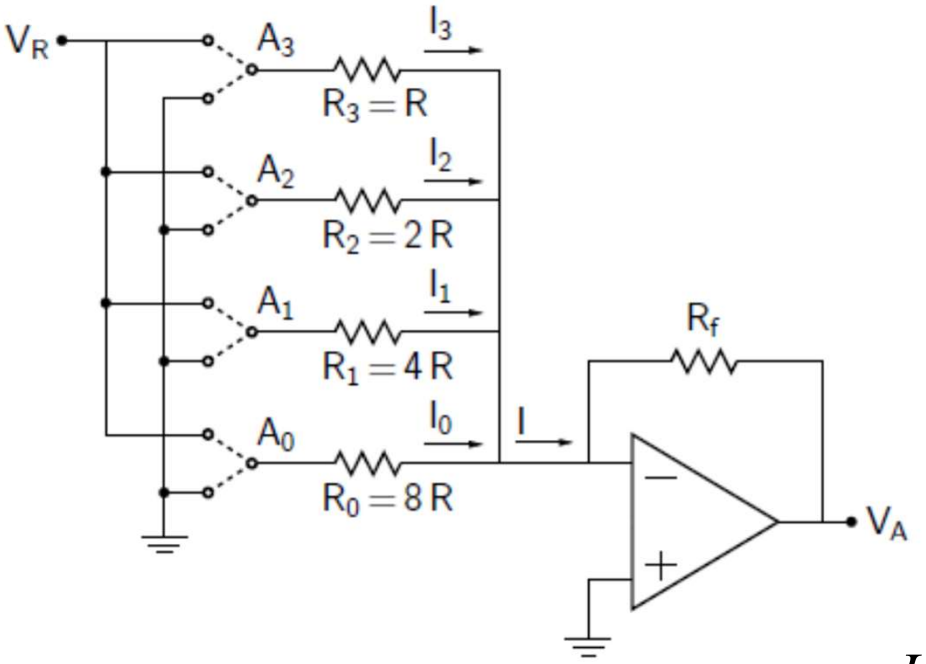


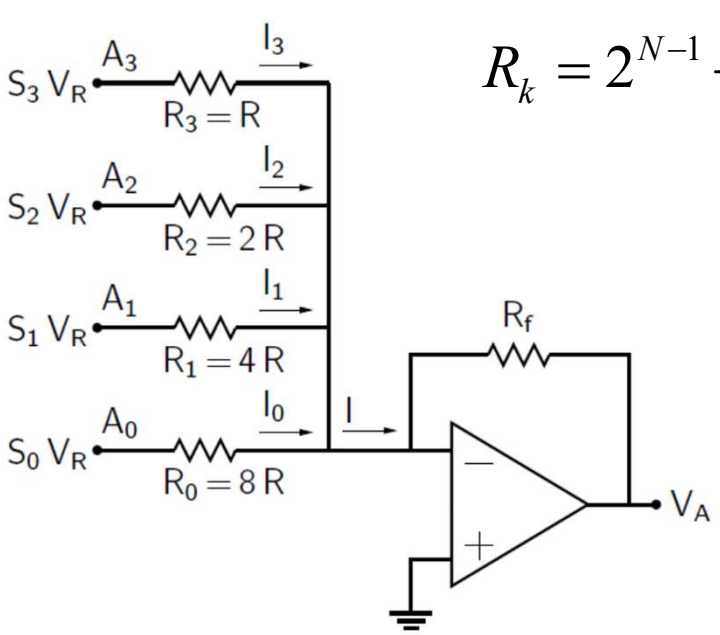


For a 4-bit DAC, with input $S_3S_2S_1S_0$, the output voltage is
$V_A = K\left[(S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0)\right]$.
In general, $V_A = K \sum_0^{N-1} S_k 2^k$.

K is proportional to the reference voltage V_R. Its value depends on how the DAC is implemented.

DAC using Binary-weighted resistors





$$R_k = 2^{N-1}\frac{R}{2^k}$$

$$I = I_0 + I_1 + I_2 + I_3$$

$$I_0 = \frac{S_o V_R}{R_o} \qquad I_1 = \frac{S_1 V_R}{R_1}$$

DAC using Binary-weighted resistors

If the input bit S_k is 1, A_k gets connected to V_R; else, it gets connected to ground.
$\rightarrow V(A_k) = S_k \times V_R$.

Since the inverting terminal of the Op Amp is at virtual ground,

$$I_k = \frac{V(A_k) - 0}{R_k} = \frac{S_k\, V_R}{R_k} .$$

Using $R_k = 2^{N-1}\, R/2^k$, we get $I = \dfrac{V_R}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$ ($N = 4$ here).

The output voltage is $V_o = -R_f\, I = -V_R\, \dfrac{R_f}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$.

- Consider an 8-bit DAC with V_R =5 V. What is the smallest value of R which will limit the current drawn from the supply (V_R) to 10 mA?

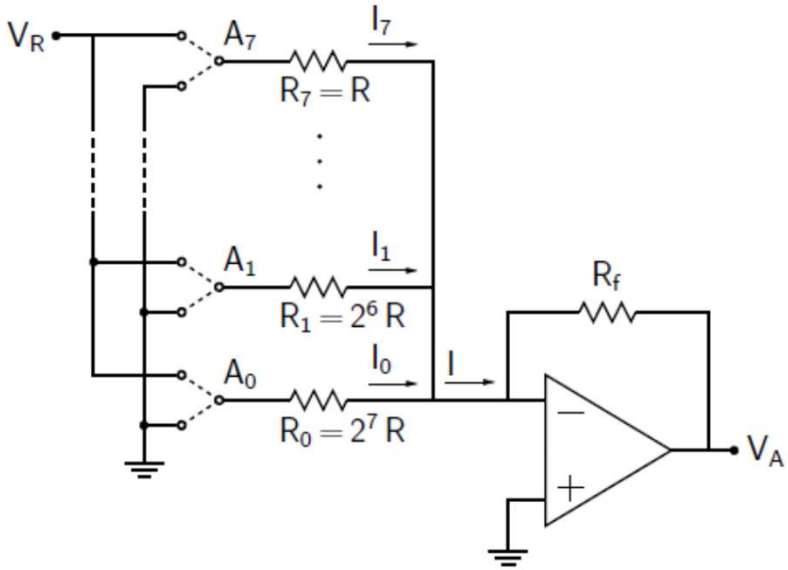
Maximum current is drawn from V_R when the input is 1111 1111.

$\rightarrow$ All nodes A_0 to A_7 get connected to V_R.

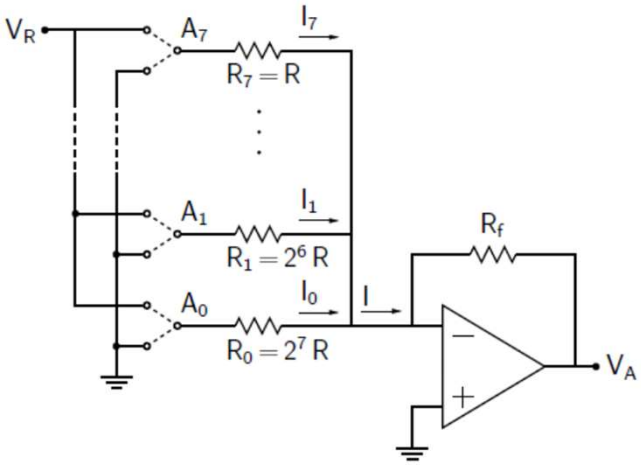
$$\rightarrow 10\,\text{mA} = \frac{V_R}{R} + \frac{V_R}{2R} + \cdots + \frac{V_R}{2^7 R} = \frac{1}{2^7}\,\frac{V_R}{R}\left(2^0 + 2^1 + \cdots + 2^7\right)$$

$$= \frac{1}{2^7}\,\frac{V_R}{R}\left(2^8 - 1\right) = \frac{255}{128}\,\frac{V_R}{R}$$

$$\rightarrow R_{\text{min}} = \frac{5\,\text{V}}{10\,\text{mA}} \times \frac{255}{128} = 996\,\Omega\,.$$



- If R_f =R, what is the resolution (i.e., V_A corresponding to the input LSB changing from 0 to 1 with other input bits constant)?



$$V_A = -V_R \frac{R_f}{2^{N-1}R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right]$$

$$\rightarrow \Delta V_A = \frac{V_R}{2^{N-1}}\frac{R_f}{R} = \frac{5\,\text{V}}{2^{8-1}} \times 1 = \frac{5}{128} = 0.0391\,\text{V}.$$

- What is the maximum output voltage (in magnitude)?

$$V_A = -\frac{V_R}{2^{N-1}}\frac{R_f}{R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right].$$

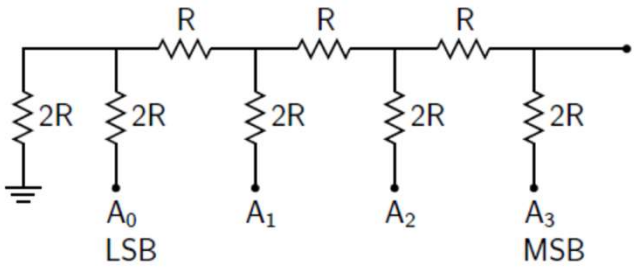
Maximum V_A (in magnitude) is obtained when the input is 1111 1111.

$$|V_A|^{\max} = \frac{5}{128} \times 1 \times \left[2^0 + 2^1 + \cdots + 2^7\right] = \frac{5}{128} \times \left(2^8 - 1\right) = 5 \times \frac{255}{128} = 9.961\,\text{V}.$$

- Find the output voltage corresponding to the input 1010 1101.

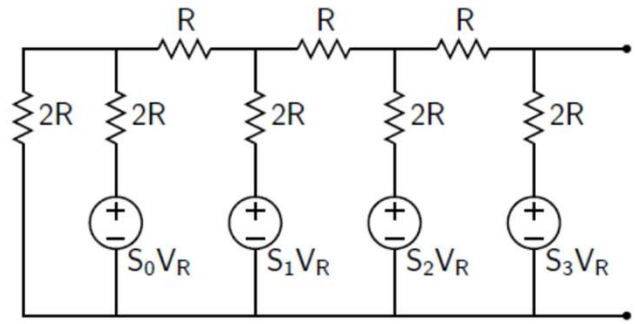
$$V_A = -\frac{V_R}{2^{N-1}}\frac{R_f}{R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right].$$
$$= -\frac{5}{128} \times 1 \times \left[2^7 + 2^5 + 2^3 + 2^2 + 2^0\right] = -5 \times \frac{173}{128} = -6.758\,\text{V}.$$

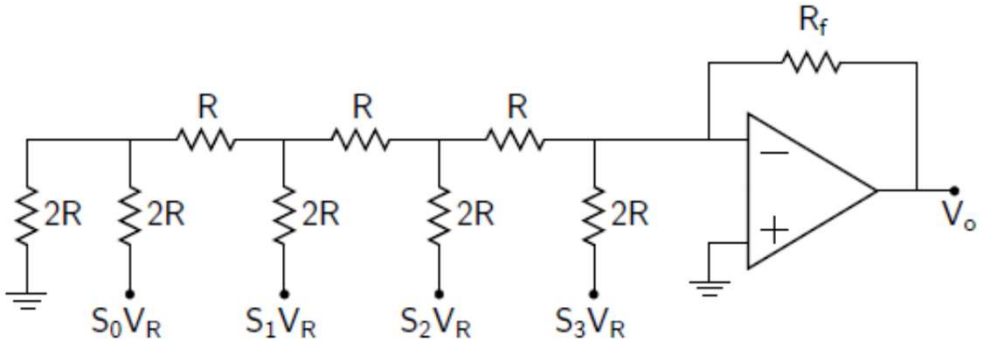
DAC with R-2R Ladder



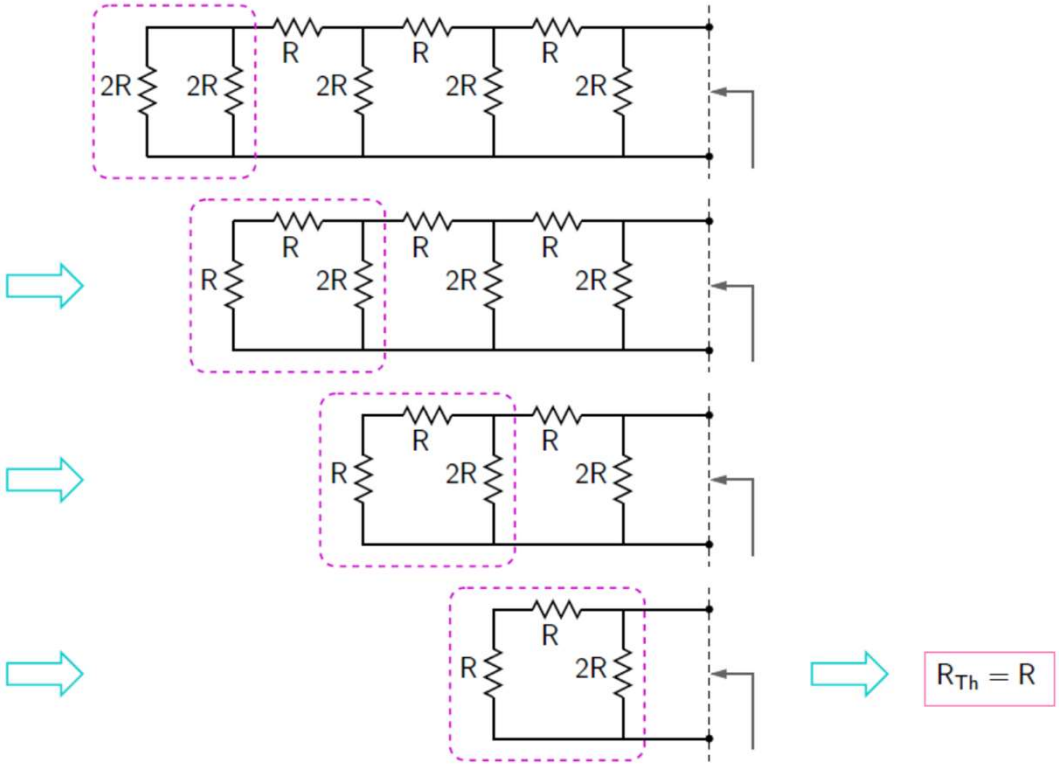
Node A_k is connected to V_R if input bit S_k is 1; else, it is connected to ground.

The original network is equivalent to

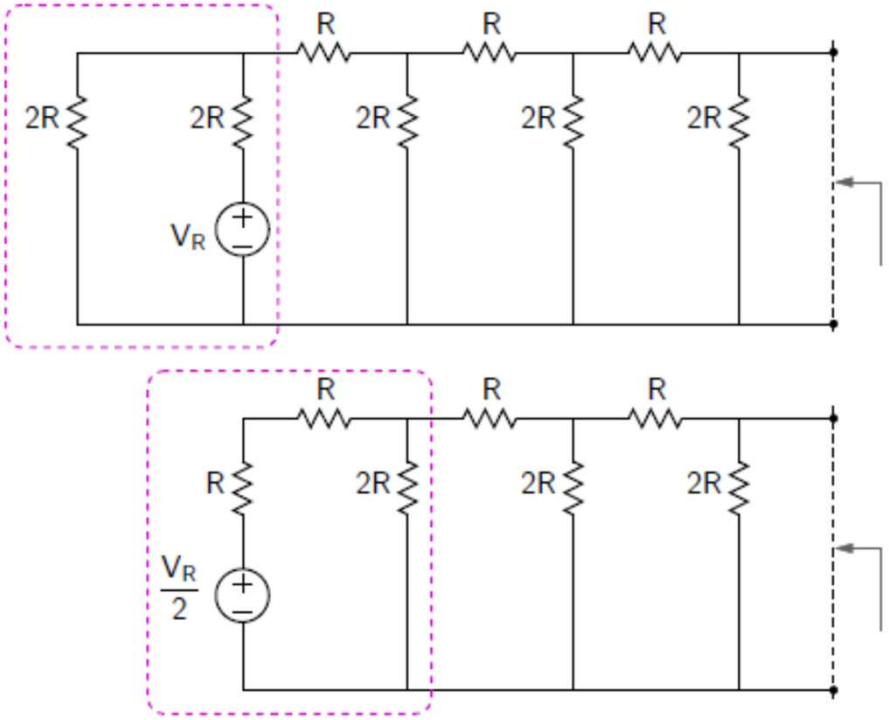


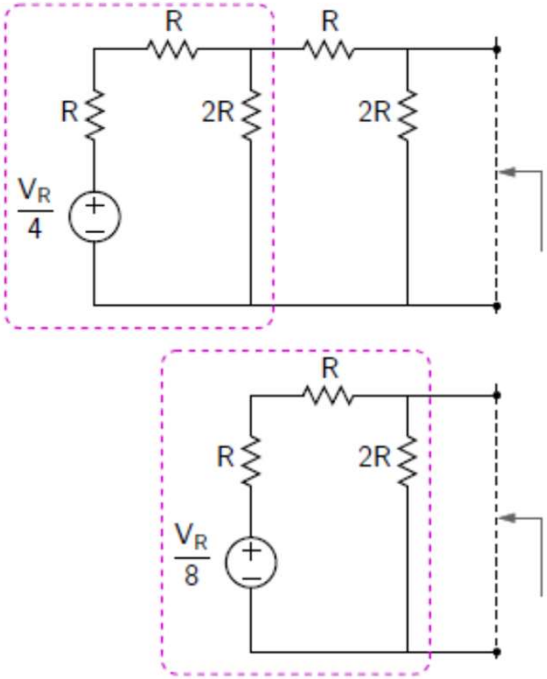


R-2R Ladder Network

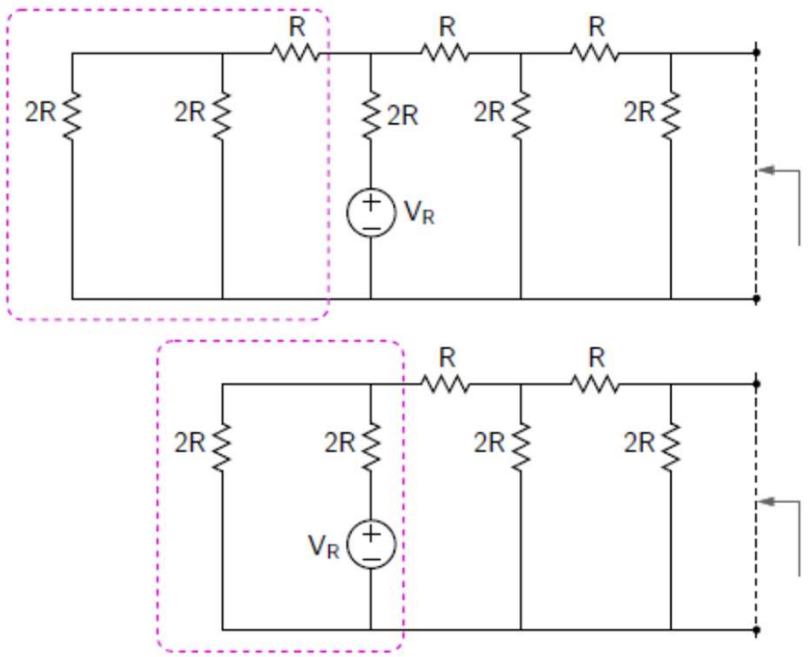


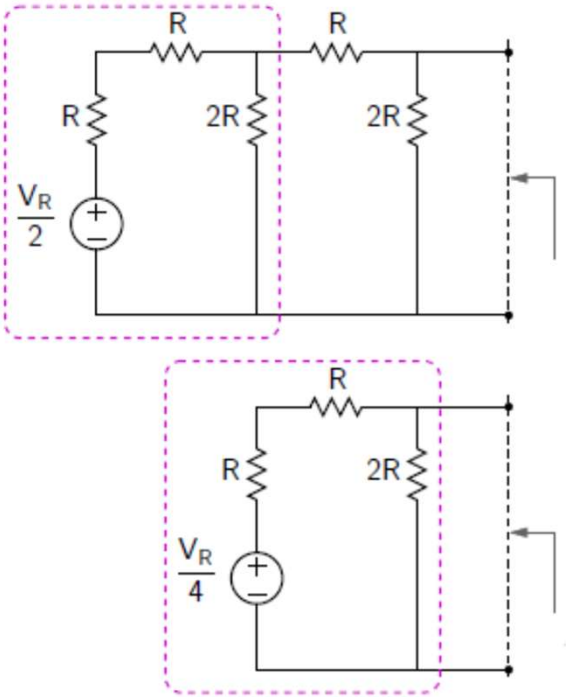
R-2R ladder network: V_{Th} for S_0 =1



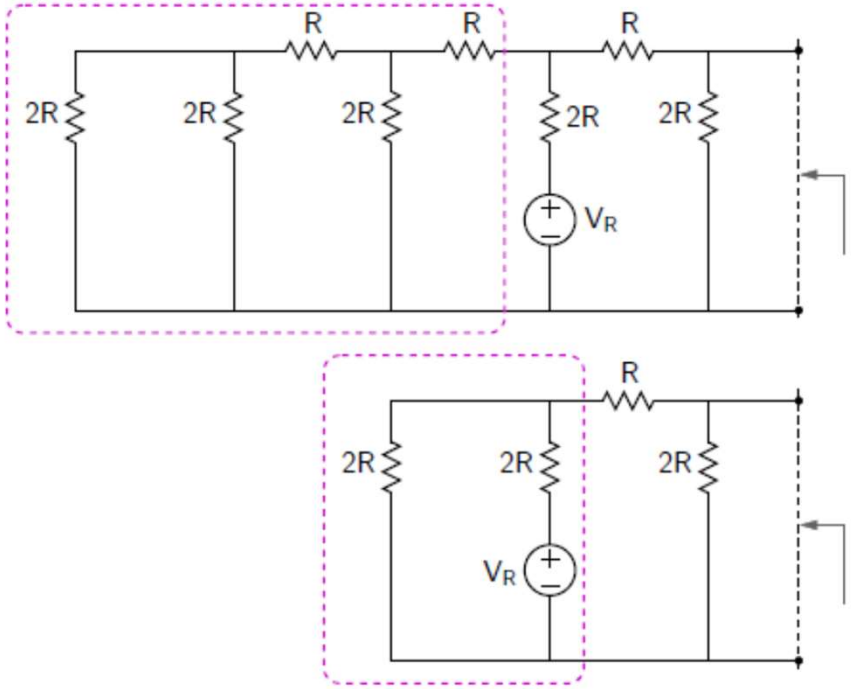


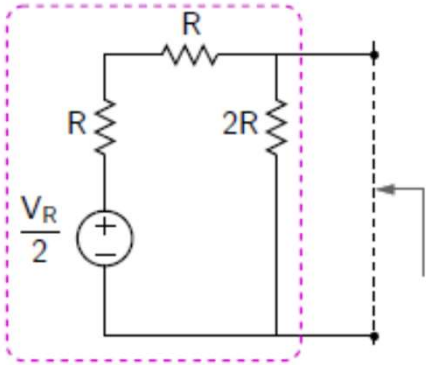
R-2R ladder network: V_{Th} for S_1 =1



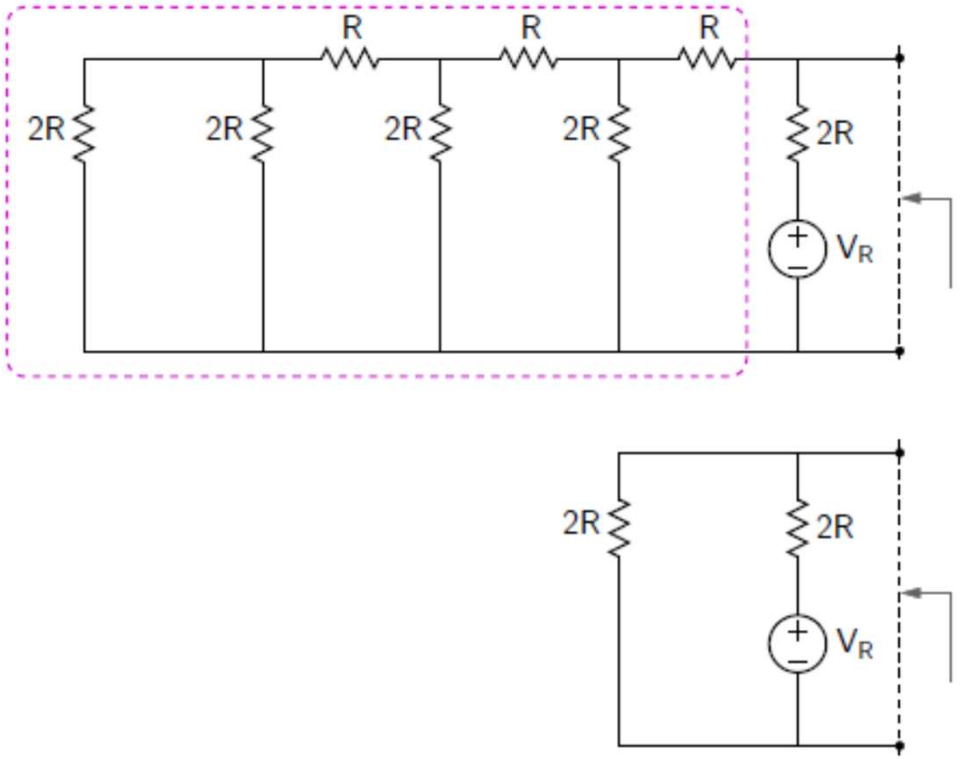


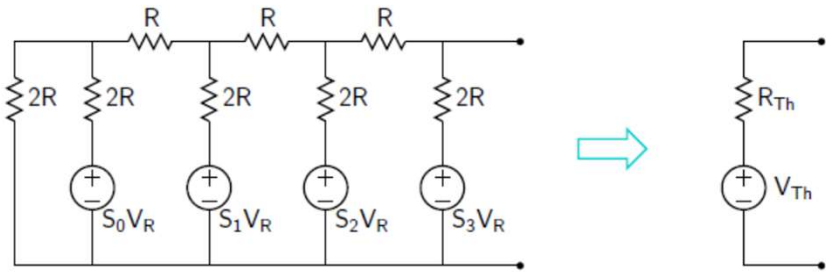
R-2R ladder network: V_{Th} for S_2 =1





R-2R ladder network: V_{Th} for S_3 =1



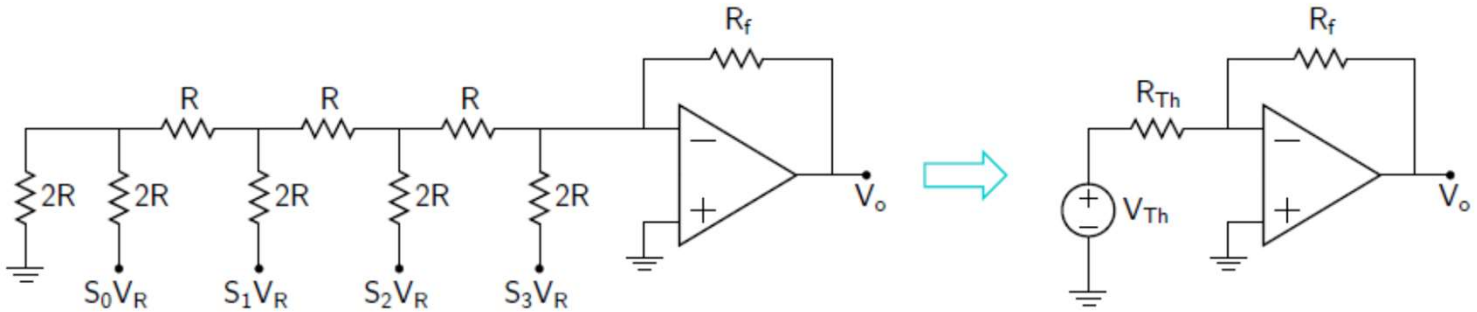


$$R_{Th} = R\,.$$

$$V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)}$$

$$= \frac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right]\,.$$

We can use the R-$2R$ ladder network and an Op Amp



$$V_o = -\frac{R_f}{R_{Th}}\,V_{Th} = -\frac{R_f}{R_{Th}}\,\frac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right]\,.$$

For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}}\,V_{Th} = -\dfrac{R_f}{R_{Th}}\,\dfrac{V_R}{2^N}\,\displaystyle\sum_{0}^{N-1} S_k 2^k\,.$

6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).