Indian Institute of Information Technology, Sri City, Chittoor
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Analog to Digital and Digital to Analog Converters

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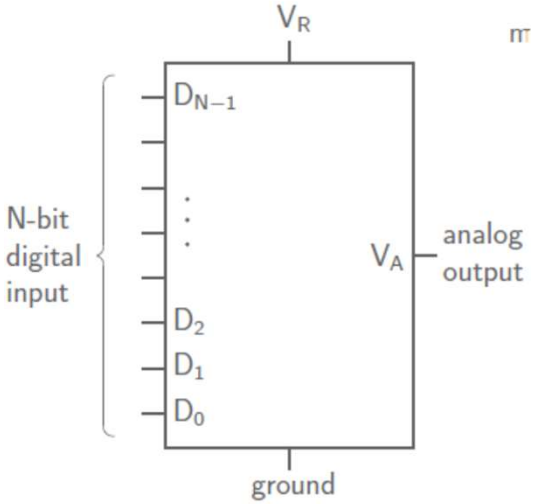
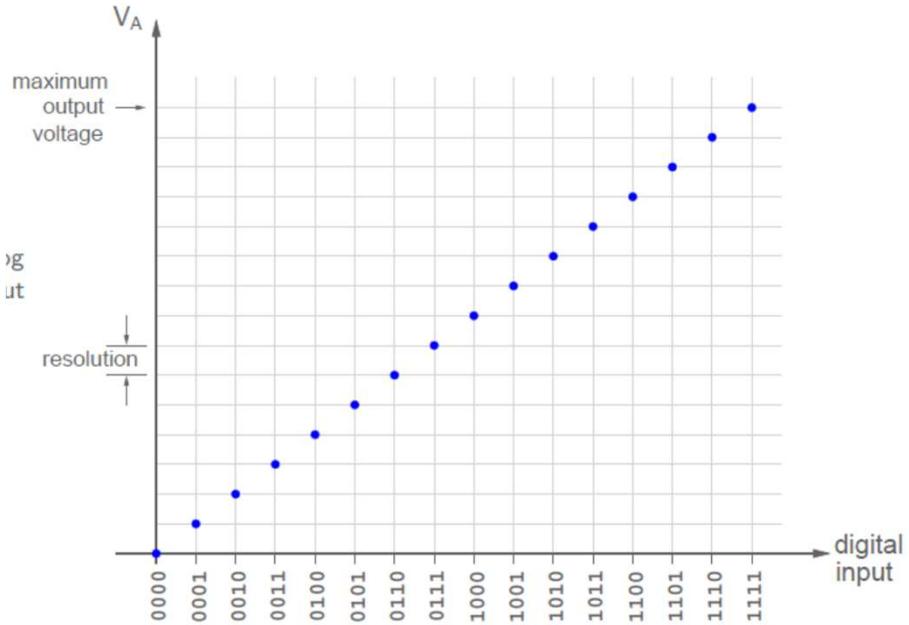
Introduction

- Physical quantities (e.g., Temparature, a voltage or a speech signal) are analog analog in nature, varying continuously with time.
- Digital format offers several advantages: digital signal processing, storage, use of computers, robust transmission, etc.
- An ADC (Analog-to-Digital Converter) is used to convert an analog signal to the digital format.
- The reverse conversion (from digital to analog) is also required. For example, music stored in a DVD in digital format must be converted to an analog voltage for playing out on a speaker.
- A DAC (Digital-to-Analog Converter) is used to convert a digital signal to the analog format.

Digital to Analog Converters

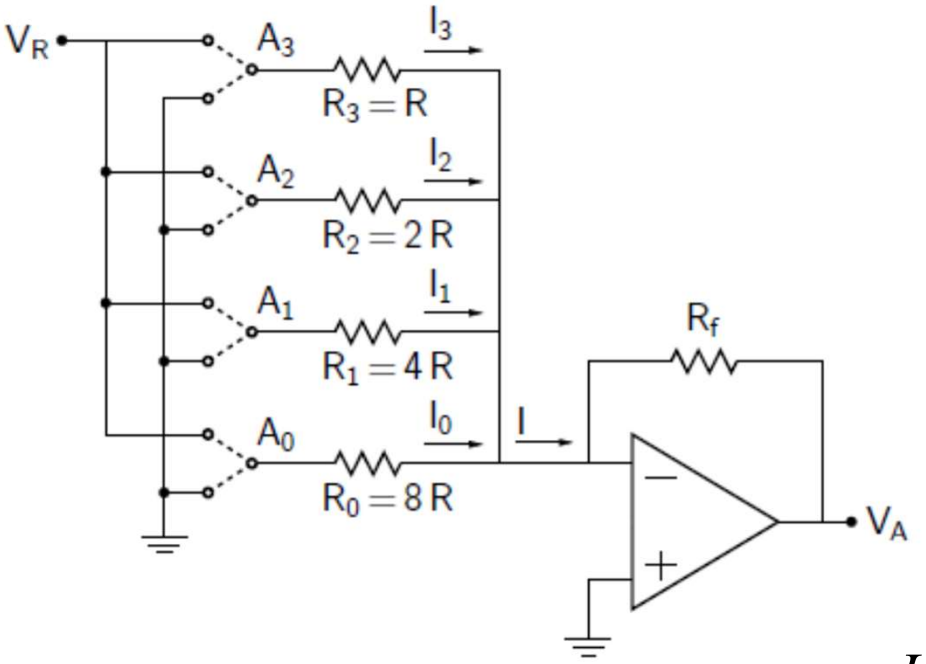


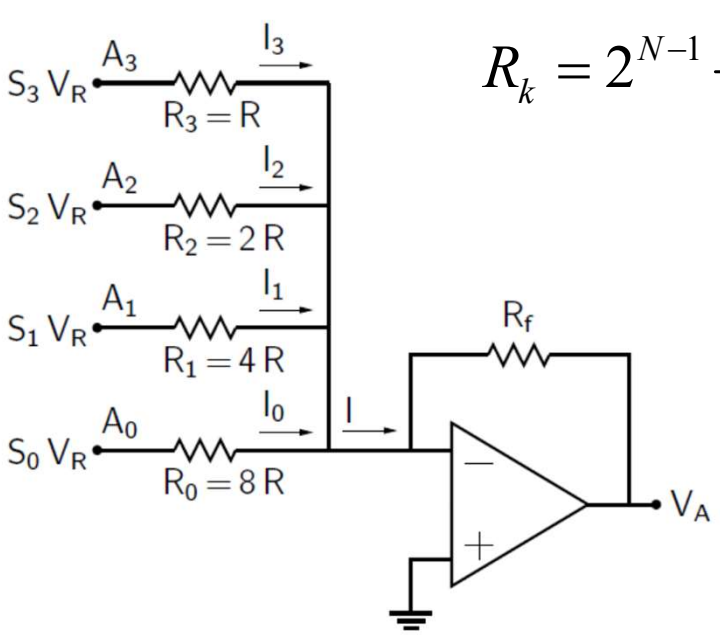


For a 4-bit DAC, with input $S_3S_2S_1S_0$, the output voltage is
$V_A = K\left[(S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0)\right]$.
In general, $V_A = K \sum_0^{N-1} S_k 2^k$.

K is proportional to the reference voltage V_R. Its value depends on how the DAC is implemented.

DAC using Binary-weighted resistors





$$R_k = 2^{N-1}\frac{R}{2^k}$$

$$I = I_0 + I_1 + I_2 + I_3$$

$$I_0 = \frac{S_o V_R}{R_o} \qquad I_1 = \frac{S_1 V_R}{R_1}$$

DAC using Binary-weighted resistors

If the input bit S_k is 1, A_k gets connected to V_R; else, it gets connected to ground.
$\rightarrow V(A_k) = S_k \times V_R$.

Since the inverting terminal of the Op Amp is at virtual ground,

$$I_k = \frac{V(A_k) - 0}{R_k} = \frac{S_k\, V_R}{R_k} .$$

Using $R_k = 2^{N-1}\, R/2^k$, we get $I = \dfrac{V_R}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$ ($N = 4$ here).

The output voltage is $V_o = -R_f\, I = -V_R\, \dfrac{R_f}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$.

- Consider an 8-bit DAC with V_R =5 V. What is the smallest value of R which will limit the current drawn from the supply (V_R) to 10 mA?

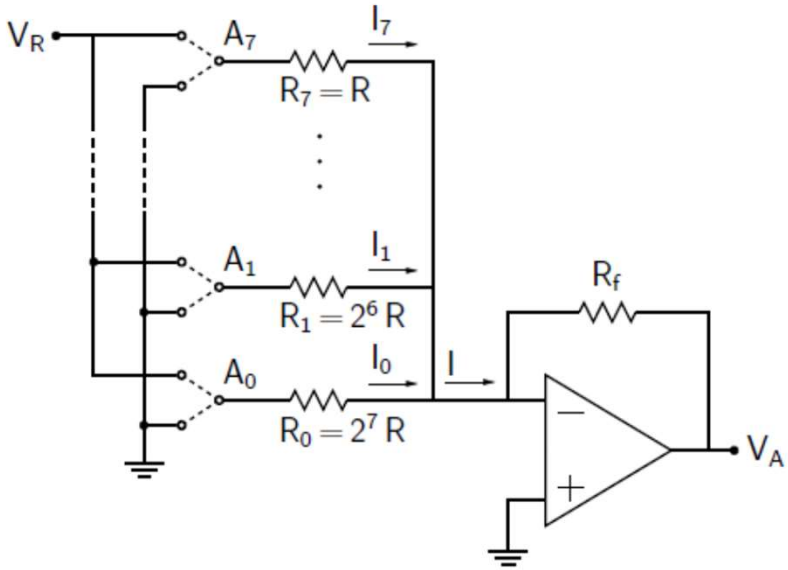
Maximum current is drawn from V_R when the input is 1111 1111.

$\rightarrow$ All nodes A_0 to A_7 get connected to V_R.

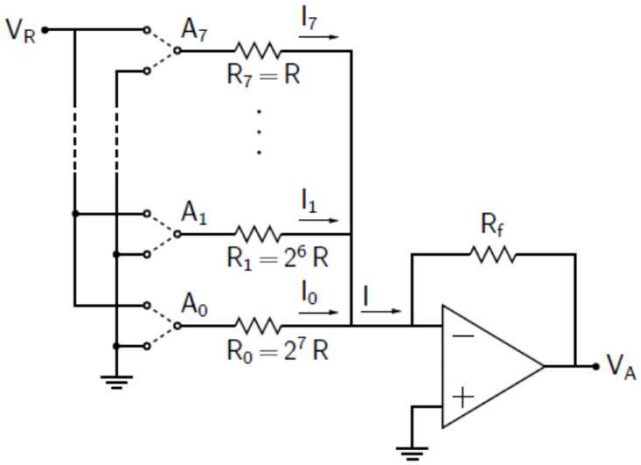
$$\rightarrow 10\,\text{mA} = \frac{V_R}{R} + \frac{V_R}{2R} + \cdots + \frac{V_R}{2^7 R} = \frac{1}{2^7}\,\frac{V_R}{R}\left(2^0 + 2^1 + \cdots + 2^7\right)$$

$$= \frac{1}{2^7}\,\frac{V_R}{R}\left(2^8 - 1\right) = \frac{255}{128}\,\frac{V_R}{R}$$

$$\rightarrow R_{\text{min}} = \frac{5\,\text{V}}{10\,\text{mA}} \times \frac{255}{128} = 996\,\Omega\,.$$



- If R_f =R, what is the resolution (i.e., V_A corresponding to the input LSB changing from 0 to 1 with other input bits constant)?



$$V_A = -V_R \frac{R_f}{2^{N-1}R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right]$$

$$\rightarrow \Delta V_A = \frac{V_R}{2^{N-1}}\frac{R_f}{R} = \frac{5\,\text{V}}{2^{8-1}} \times 1 = \frac{5}{128} = 0.0391\,\text{V}.$$

- What is the maximum output voltage (in magnitude)?

$$V_A = -\frac{V_R}{2^{N-1}}\frac{R_f}{R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right].$$

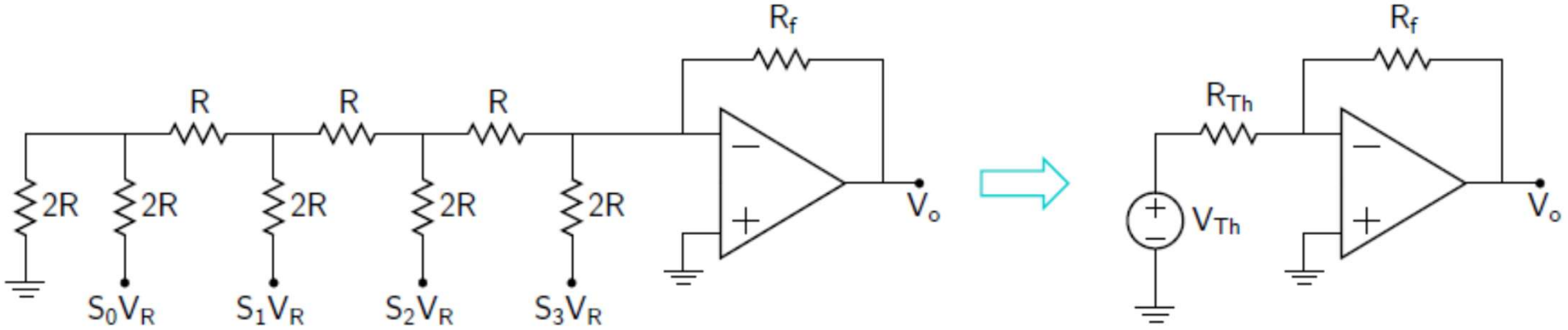
Maximum V_A (in magnitude) is obtained when the input is 1111 1111.

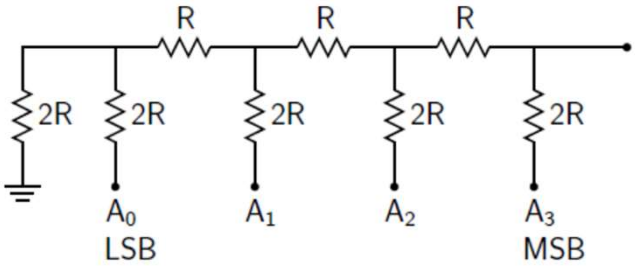
$$|V_A|^{\max} = \frac{5}{128} \times 1 \times \left[2^0 + 2^1 + \cdots + 2^7\right] = \frac{5}{128} \times \left(2^8 - 1\right) = 5 \times \frac{255}{128} = 9.961\,\text{V}.$$

- Find the output voltage corresponding to the input 1010 1101.

$$V_A = -\frac{V_R}{2^{N-1}}\frac{R_f}{R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right].$$
$$= -\frac{5}{128} \times 1 \times \left[2^7 + 2^5 + 2^3 + 2^2 + 2^0\right] = -5 \times \frac{173}{128} = -6.758\,\text{V}.$$

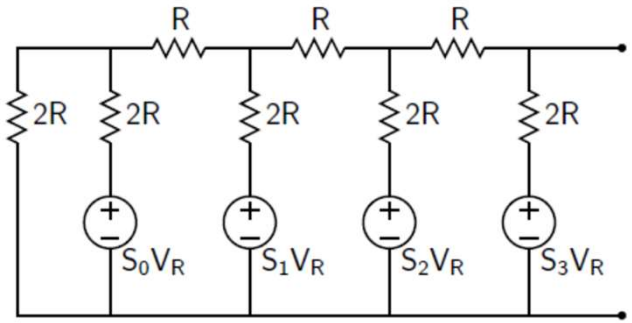
DAC with R-2R Ladder



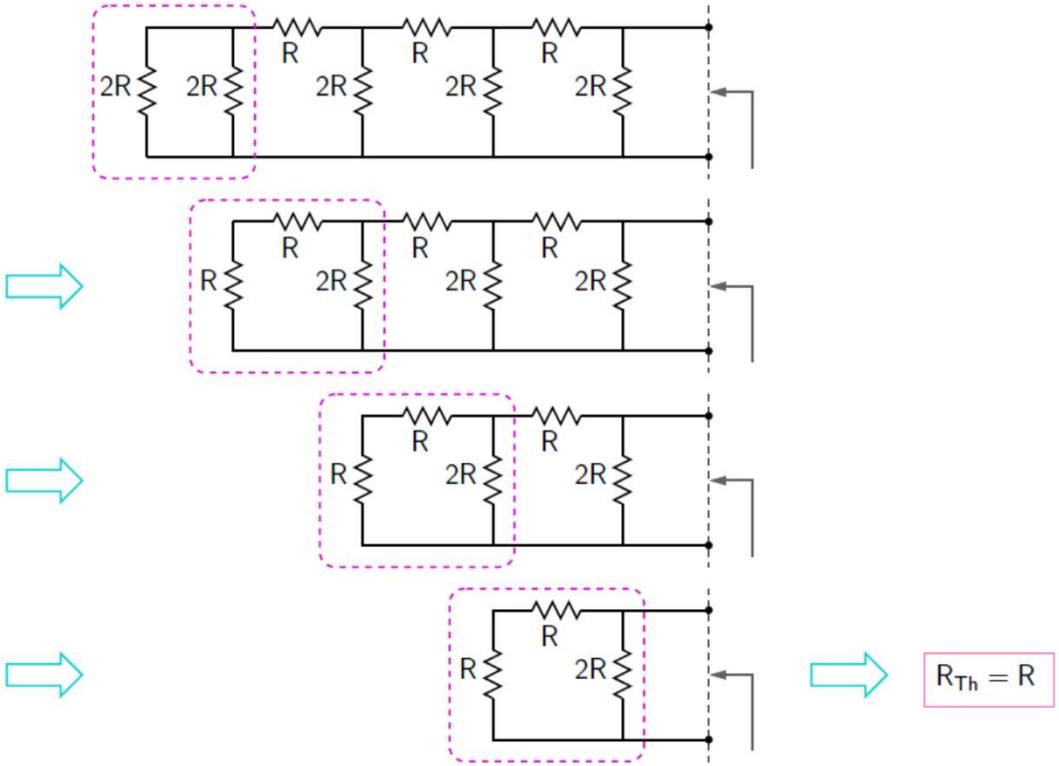


Node A_k is connected to V_R if input bit S_k is 1; else, it is connected to ground.

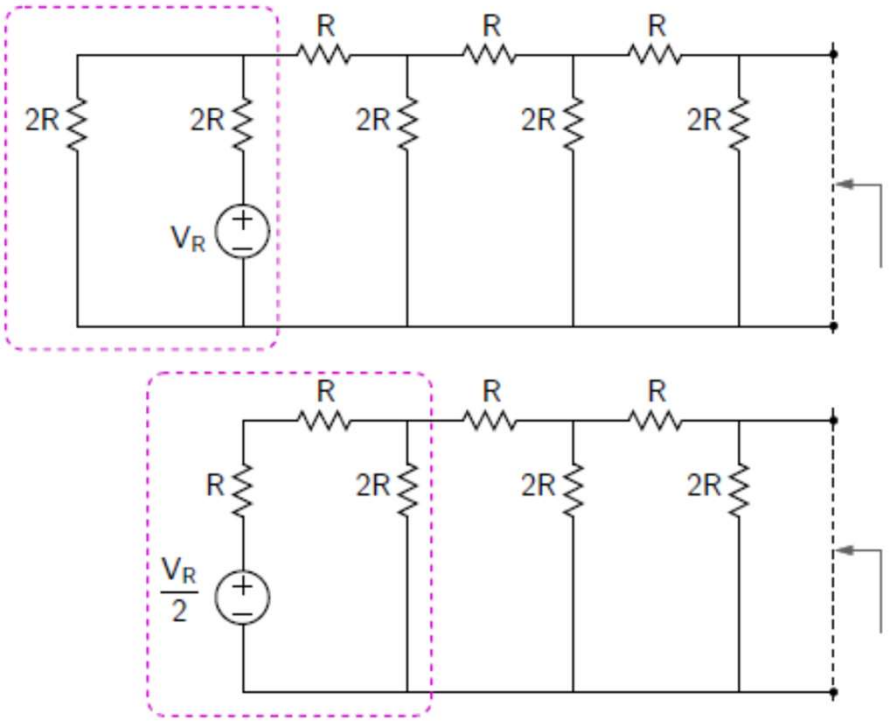
The original network is equivalent to

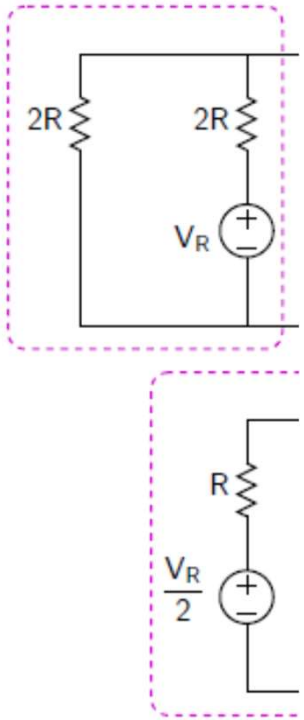


R-2R Ladder Network: Equivalent resistance

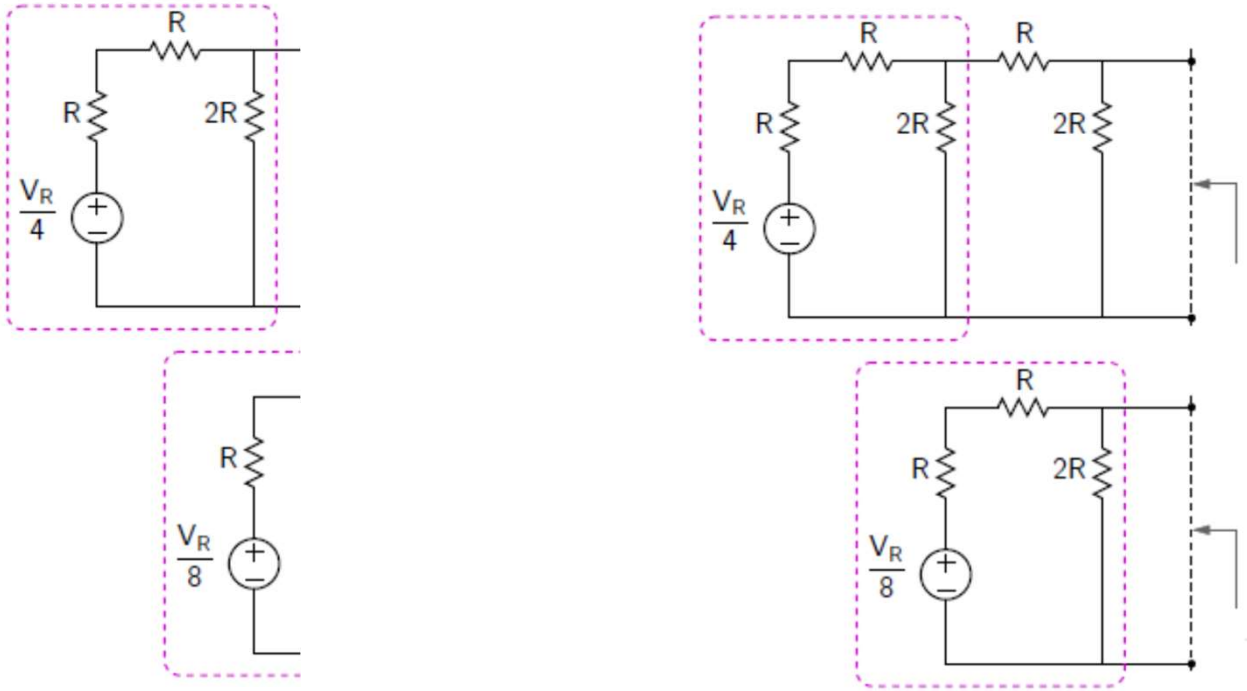


R-2R ladder network: V_{Th} for S_0 =1

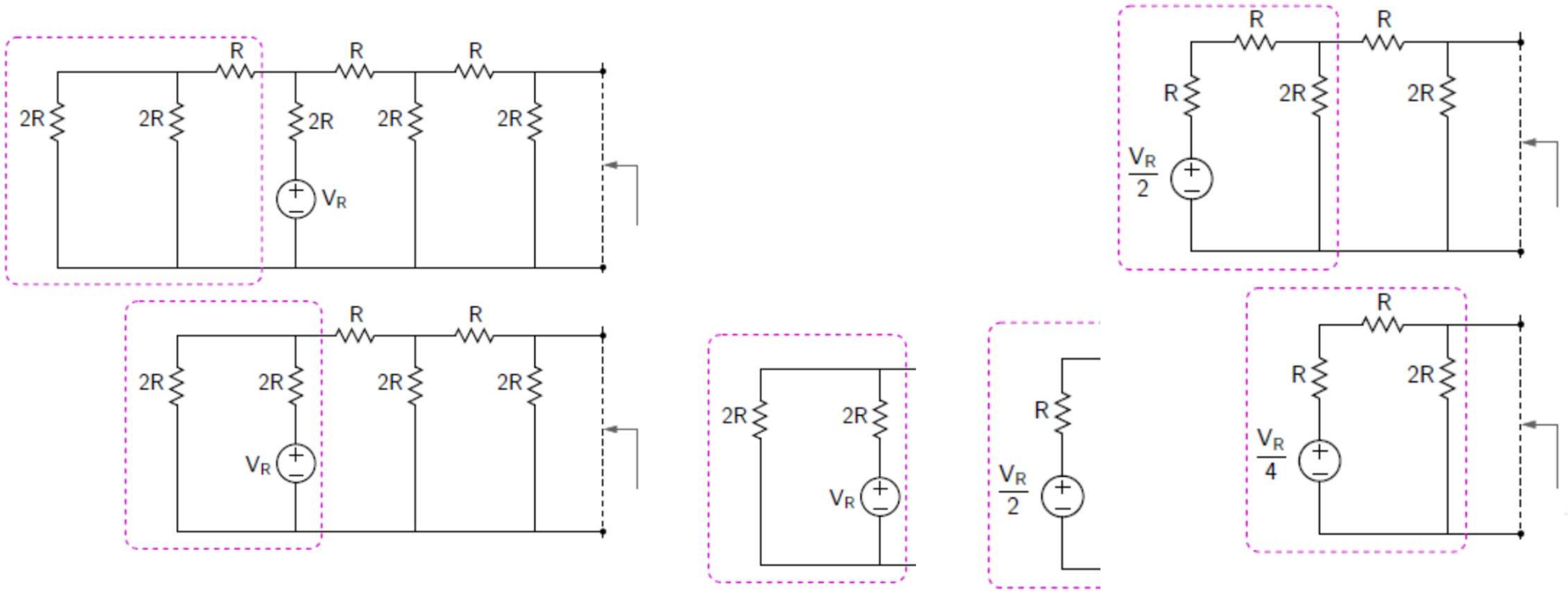




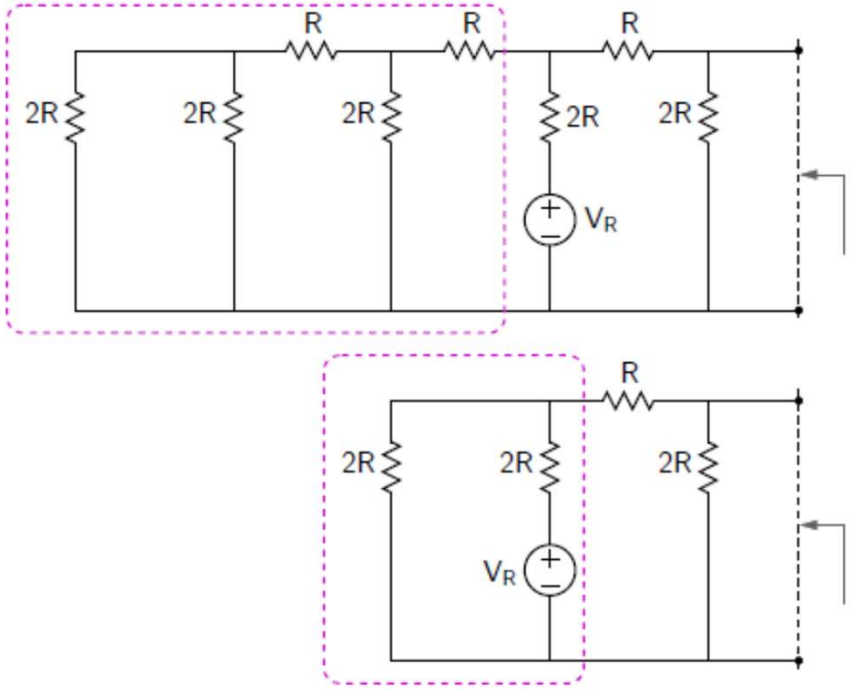
R-2R ladder network: V_{Th} for S_0 =1

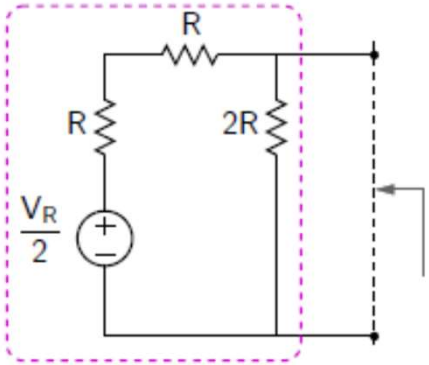


R-2R ladder network: V_{Th} for S_1 =1

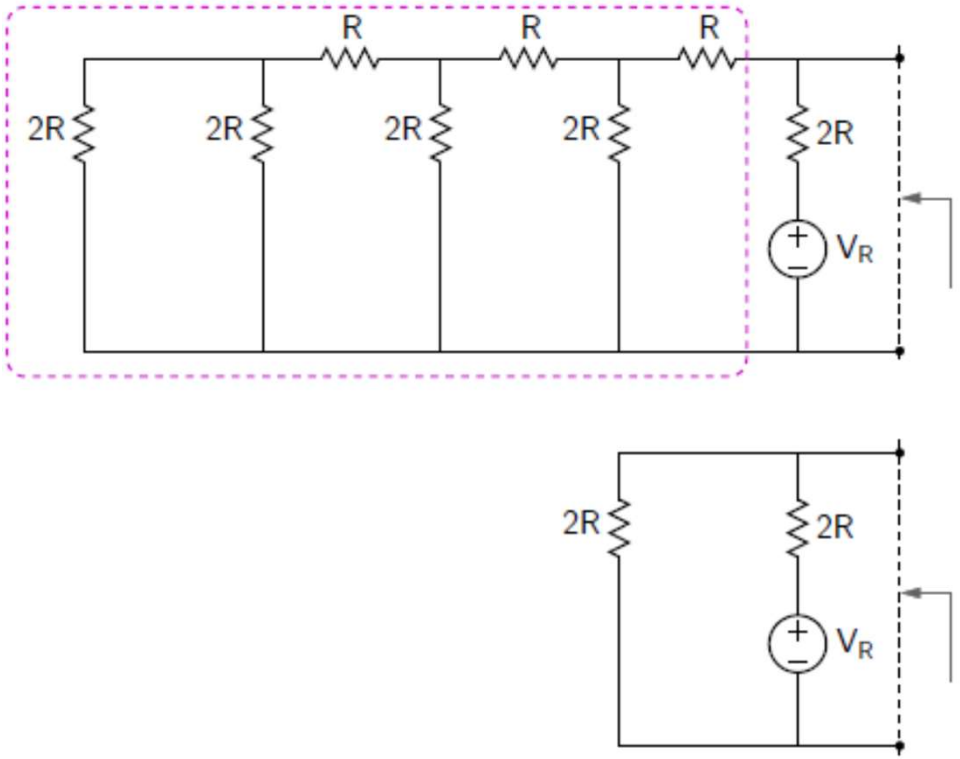


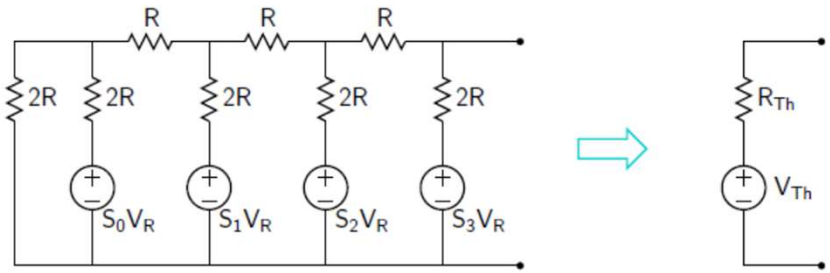
R-2R ladder network: V_{Th} for S_2 =1





R-2R ladder network: V_{Th} for S_3 =1



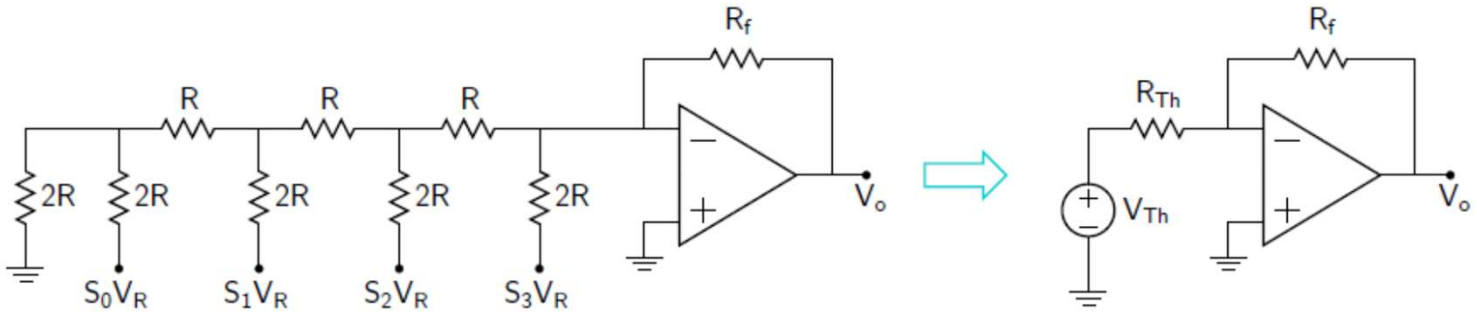


$$R_{Th} = R\,.$$

$$V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)}$$

$$= \frac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right]\,.$$

We can use the R-$2R$ ladder network and an Op Amp



$$V_o = -\frac{R_f}{R_{Th}}\,V_{Th} = -\frac{R_f}{R_{Th}}\,\frac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right]\,.$$

For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}}\,V_{Th} = -\dfrac{R_f}{R_{Th}}\,\dfrac{V_R}{2^N}\,\displaystyle\sum_{0}^{N-1} S_k 2^k\,.$

6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).

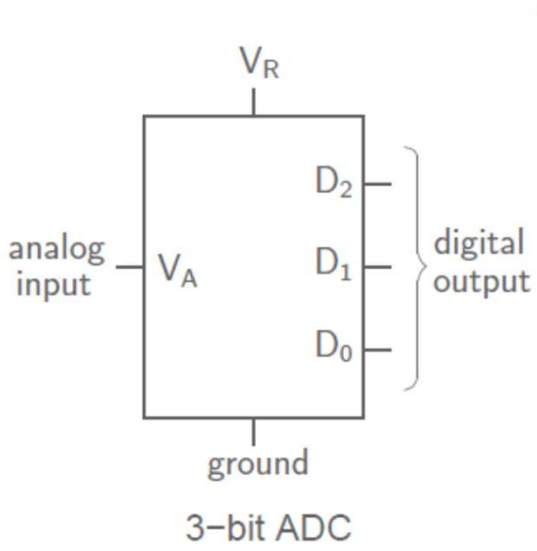
R-2R Ladder

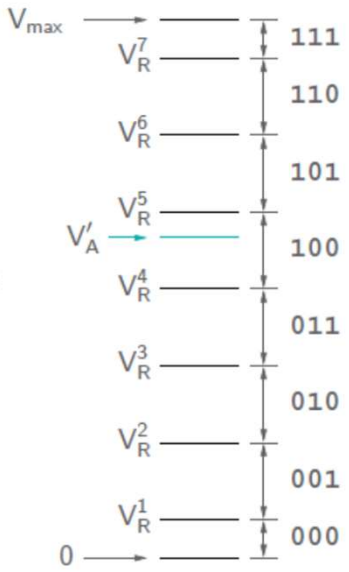
- Design a 3 bit R-2R ladder DAC, and determine Vo for the following input sequences, (a) 010 (b) 011 (c) 100, and (d) 101.

$$\text{For an N-bit DAC, } V_o = -\frac{R_f}{R_{Th}} V_{Th} = -\frac{R_f}{R_{Th}} \frac{V_R}{2^N} \sum_{0}^{N-1} S_k 2^k .$$

ADC: Introduction

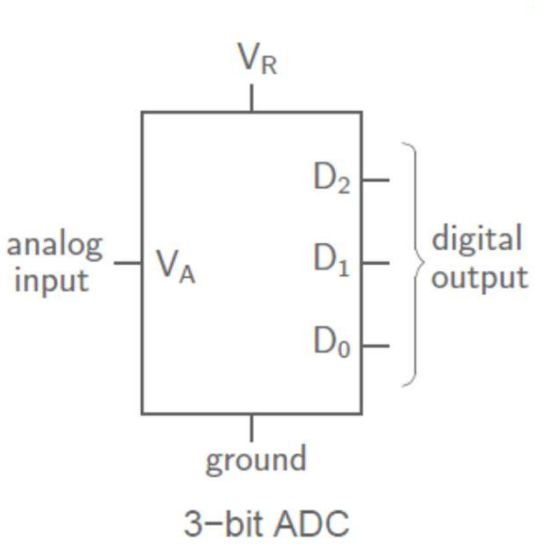
- If the input V_A is in the range $V^k_R < V_A < V^{k+1}_R$, the output is the binary number corresponding to the integer k.
- For example, for $V_A = V'_A$, the output is 100.
- We may think of each voltage interval (corresponding to 000, 001, etc.) as a "bin".
- The input voltage V'_A falls in the 100 bin; therefore, the output of the ADC would be 100.
- Note that, for an N-bit ADC, there would be 2^N bins.

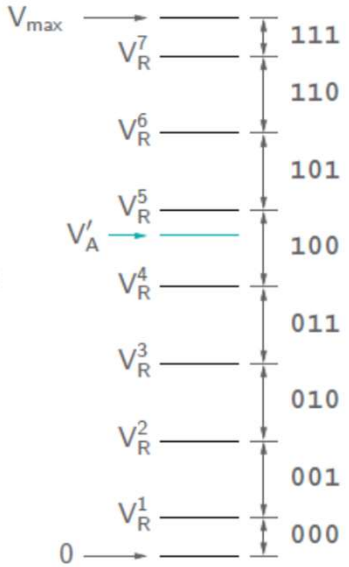




ADC: Introduction

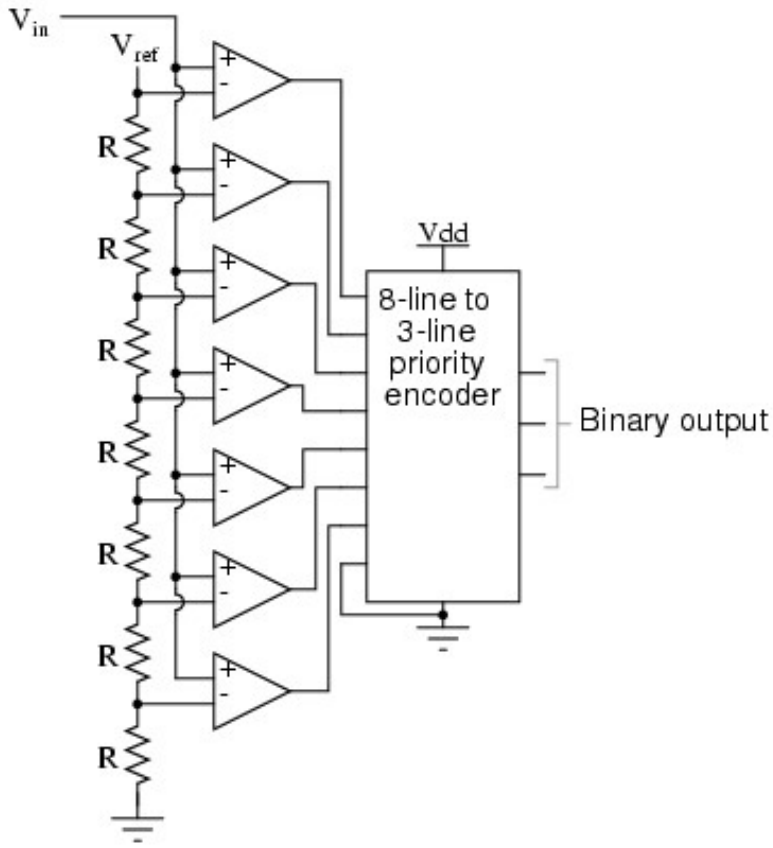
- The basic idea behind an ADC is simple:
  - Generate reference voltages V^1_R, V^2_R, etc.
  - Compare the input VA with each of V^i_R to figure out which bin it belongs to.
  - If V_A belongs to bin k (i.e., $V^k_R < V_A < V^{k+1}_R$), convert k to the binary format.
- A “parallel" ADC does exactly that.





The Parallel Comparator

- It is formed of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output
- V_{ref} is a stable reference voltage
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.

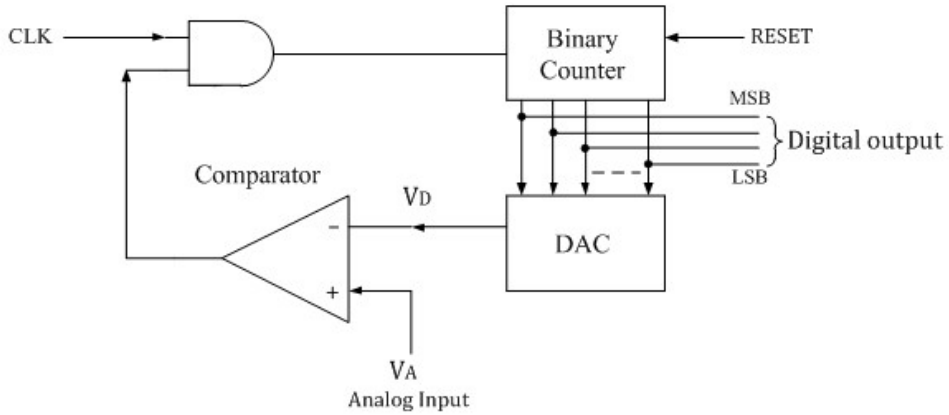


The Parallel Comparator

- It is the fastest and most expensive technique.
- it is the most component-intensive for any given number of output bits. This three-bit flash ADC requires seven comparators.
- A four-bit version would require 15 comparators. With each additional output bit, the number of required comparators doubles.
- N-bit version require 2^N -1 comparators

Counter Type ADC

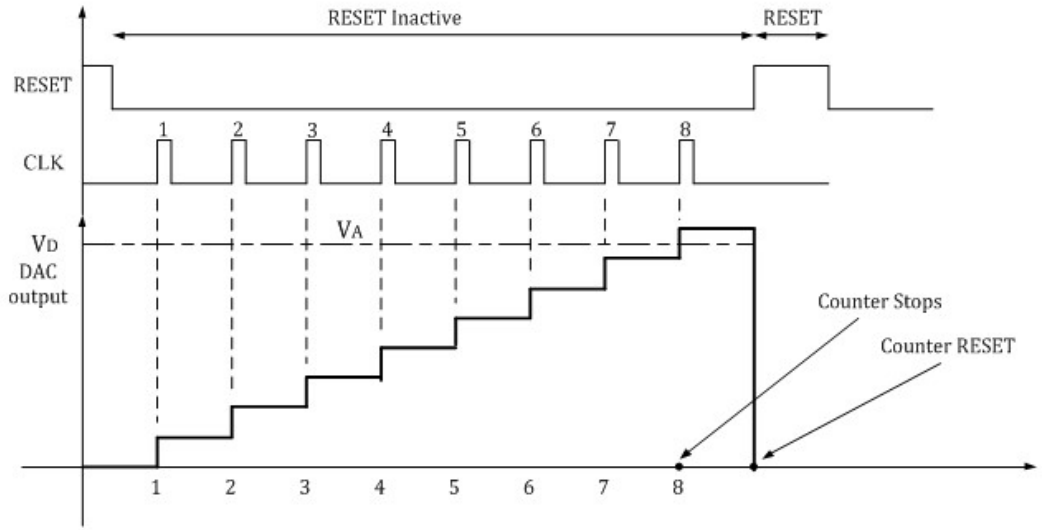
The counter type ADC is constructed using a binary counter, DAC and a comparator. The output voltage of a DAC is VD which is equivalent to corresponding digital input to DAC.



The n-bit binary counter is initially set to 0 by using reset command. Therefore the digital output is zero and the equivalent voltage V_D is also 0V.

When the reset command is removed, the clock pulses are allowed to go through AND gate and are counted by the binary counter.

The D to A converter (DAC) converts the digital output to an analog voltage and applied as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock.



Advantages:
1 Simple construction.
2 Easy to design and less expensive.
3 Speed can be adjusted by adjusting the clock frequency.

The number of clock pulses increases with time and the analog input voltage VD is a rising staircase waveform as shown in figure.
The counting will continue until the DAC output VD, equals and just rises more than unknown analog input voltage VA. Then the comparator output becomes low and this disables the AND gate from passing the clock.
The counting stops at the instance VA< VD, and at that instant the counter stops its progress and the conversion is said to be complete.
The numbers stored in the n-bit counter is the equivalent n-bit digital data for the given analog input voltage.

Successive Approximation type ADC

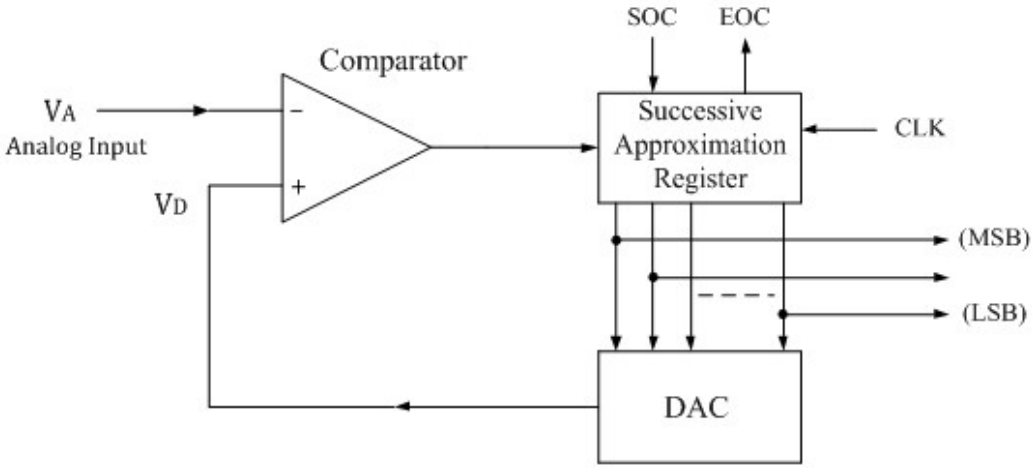
Successive Approximation type ADC is the most widely used and popular ADC method.

The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter type A/D converters.

It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC.

The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator.

The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR. When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.



The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB.

This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.
(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.
(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.
Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V.
when the conversion starts, the MSB bit is set to 1.
Now VA = 11V > VD = 8V = [1000]2
Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2),
the MSB is retained as 1 and the next MSB bit is set to 1 as follows
VD = 12V = [1100]2
Now VA = 11V < VD = 12V = [1100]2
Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as
VD = 10V = [1010]2
Now again VA = 11V > VD = 10V = [1010]2
Again as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is
VD = 11V = [1011]2
Now finally VA = VD , and the conversion stops.

Successive Approximation type ADC

- **Advantages:**
  1 Conversion time is very small.
  2 Conversion time is constant and independent of the amplitude of the analog input signal VA.
- **Disadvantages:**
  1 Circuit is complex.
  2 The conversion time is more compared to flash type ADC.