طراحی سیستم های دیجیتال
تکلیف دوم

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علیرضا نعمتی

کسری رشیدفر

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Question1

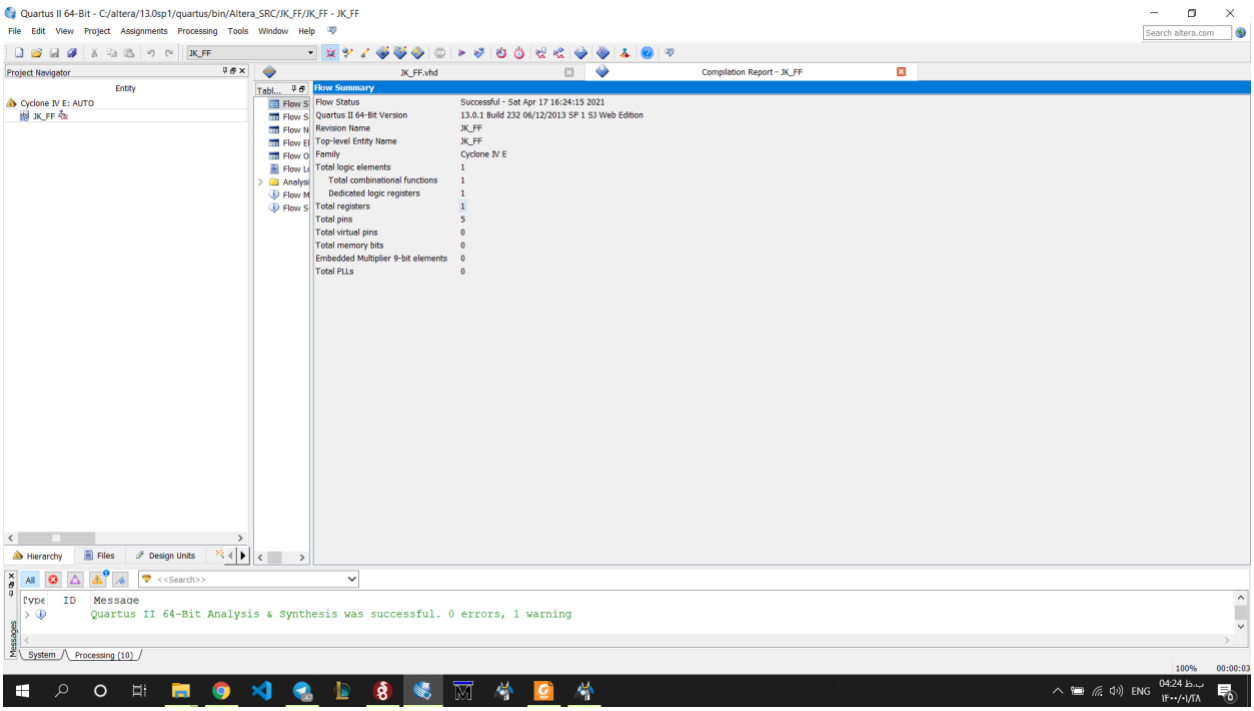
JK_FF

Code

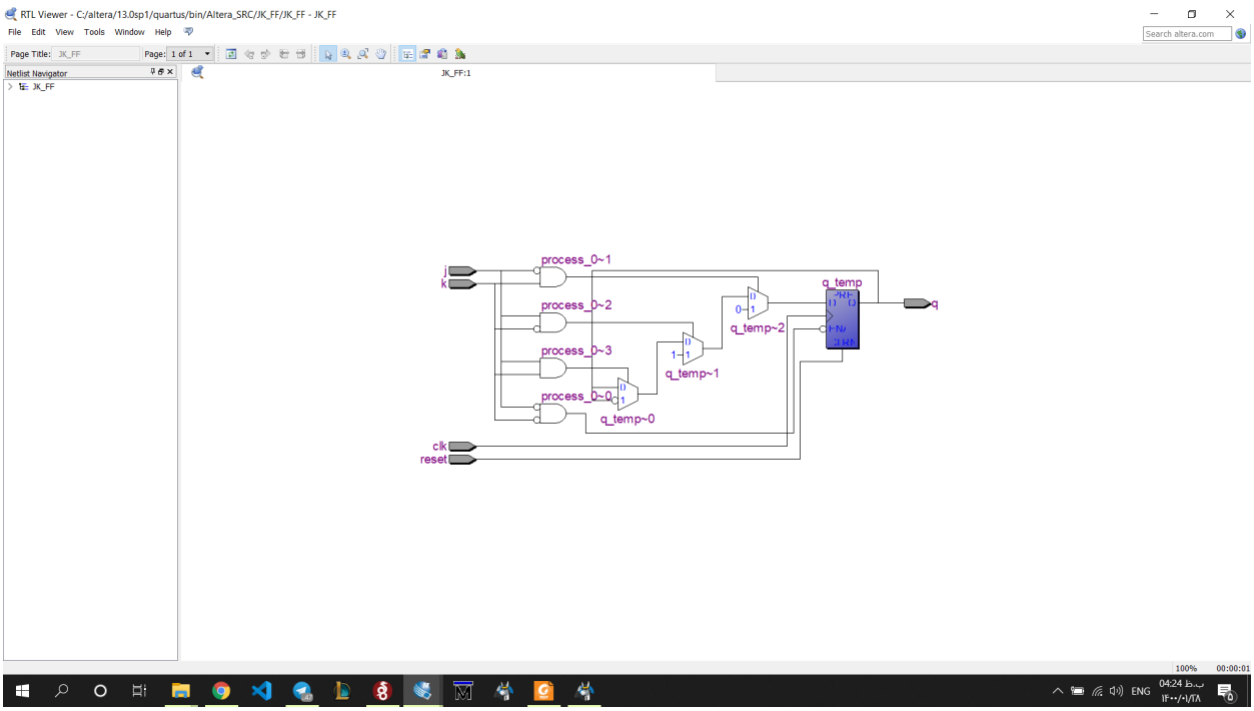
```
library ieee;
use ieee.std_logic_1164.all;

entity JK_FF is port(
    clk, reset: in std_logic;
    j, k: in std_logic;
    q: out std_logic
    );
end JK_FF;

architecture arch of JK_FF is

    signal q_temp: std_logic;

    begin
        process(clk, reset)
            begin
                if(reset = '1') then
                    q_temp <= '0';
                elsif (clk'event and clk = '1') then
                    if(j = '0' and k = '0') then
                        q_temp <= q_temp;
                    elsif(j = '0' and k = '1') then
                        q_temp <= '0';
                    elsif(j = '1' and k = '0') then
                        q_temp <= '1';
                    elsif(j = '1' and k = '1') then
```

```
                q_temp <= not (q_temp);
            end if;
        end if;
    end process;
    q <= q_temp;
end arch;
```

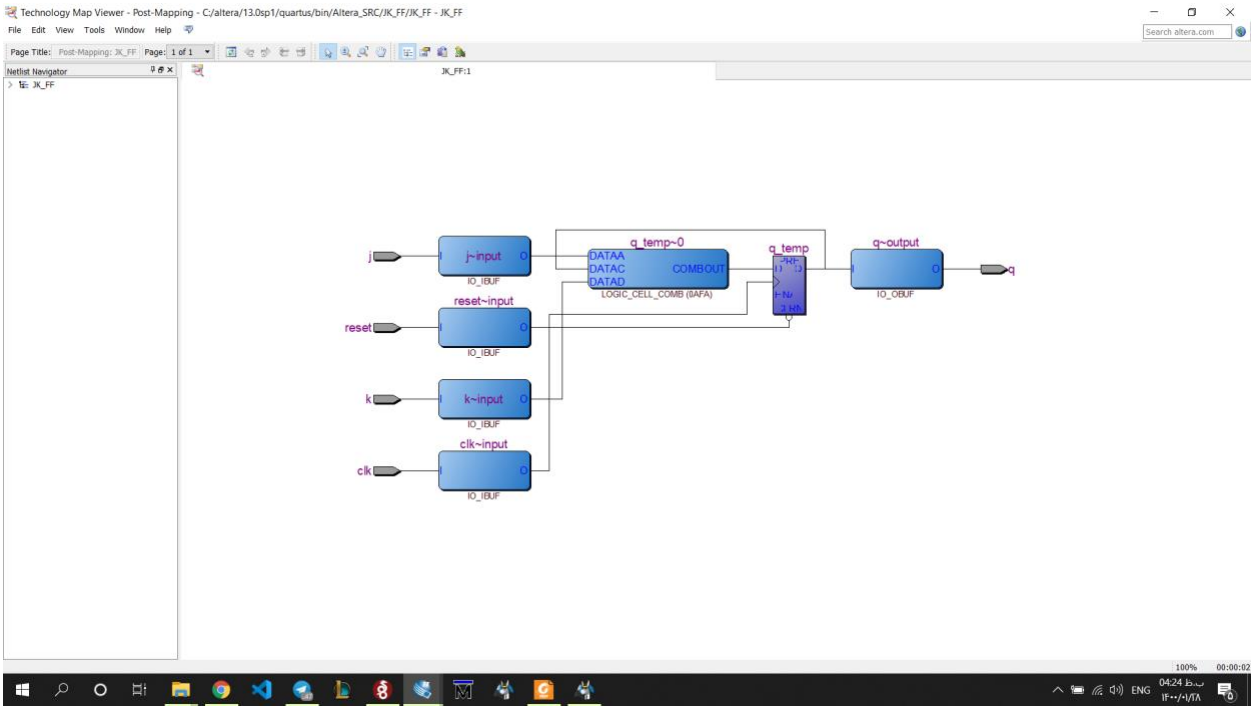
Compilation report



RTL



Post-Mapping



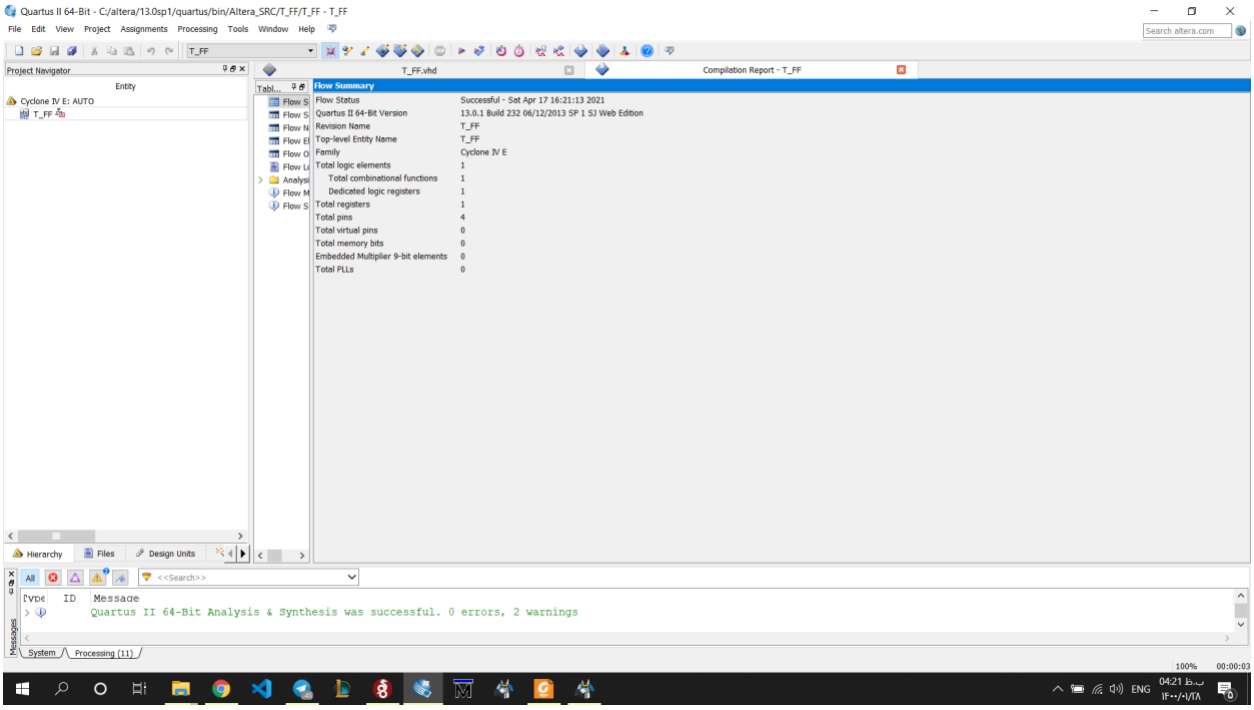
T_FF

Code

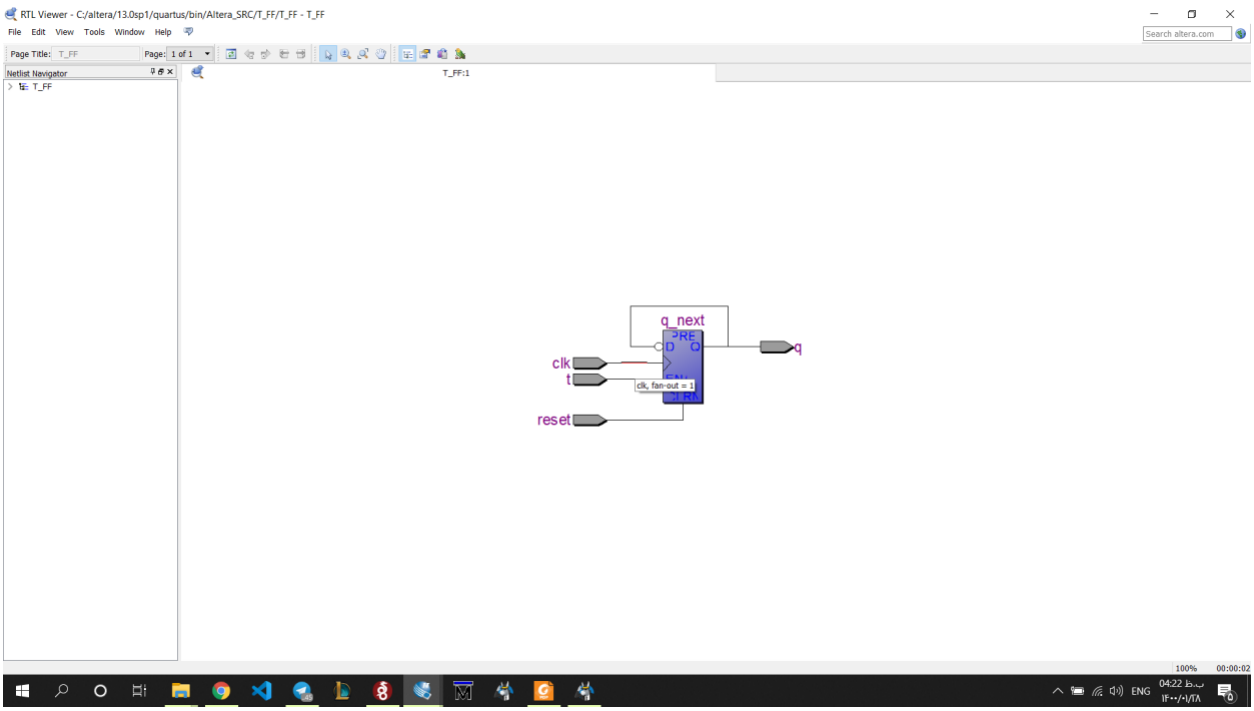
```
library ieee;
use ieee.std_logic_1164.all;

entity T_FF is
  port(
    clk: in std_logic;
    reset: in std_logic;
    t: in std_logic;
    q: out std_logic
    );
end T_FF;

architecture arch of T_FF is

  signal q_next: std_logic;

  begin
```

```
  process(clk, reset)
    begin
      if (reset = '1') then
        q_next <= '0';
      elsif (clk'event and clk = '1') then
          q_next <= (t xor q_next);
      end if;
      q <= q_next;
  end process;
end arch;
```

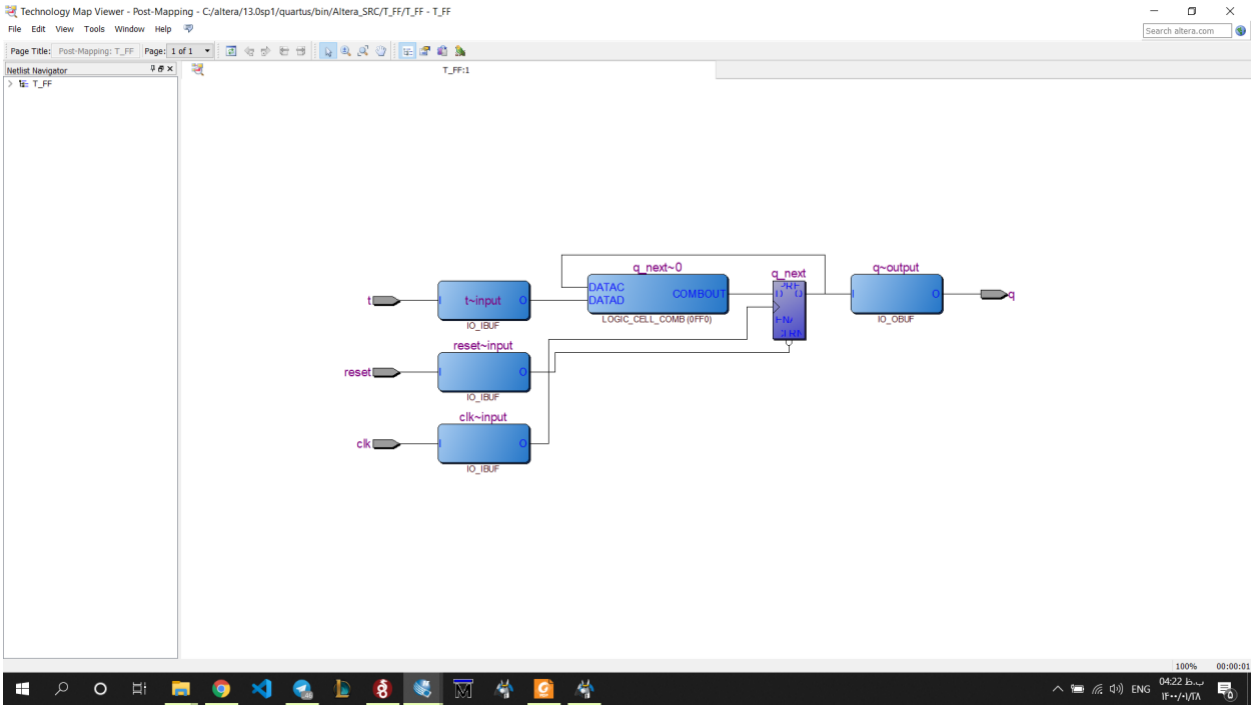
Compilation report



Rtl



Post-Mapping

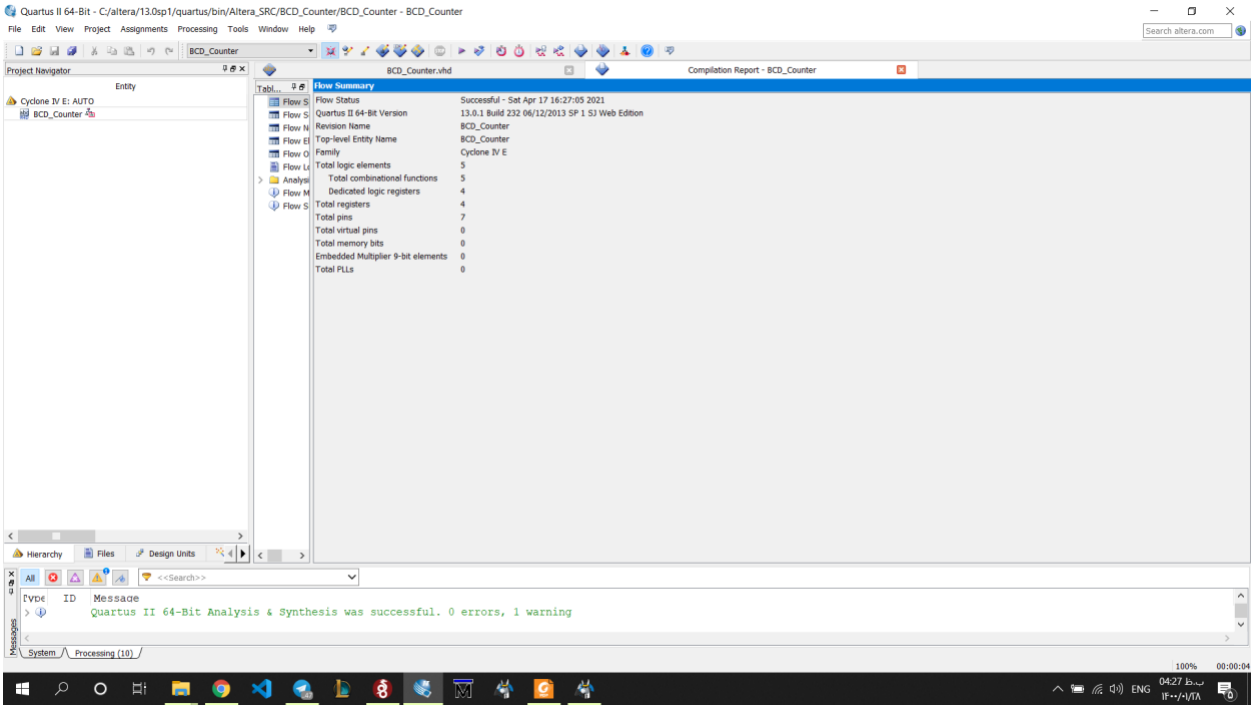


Question2

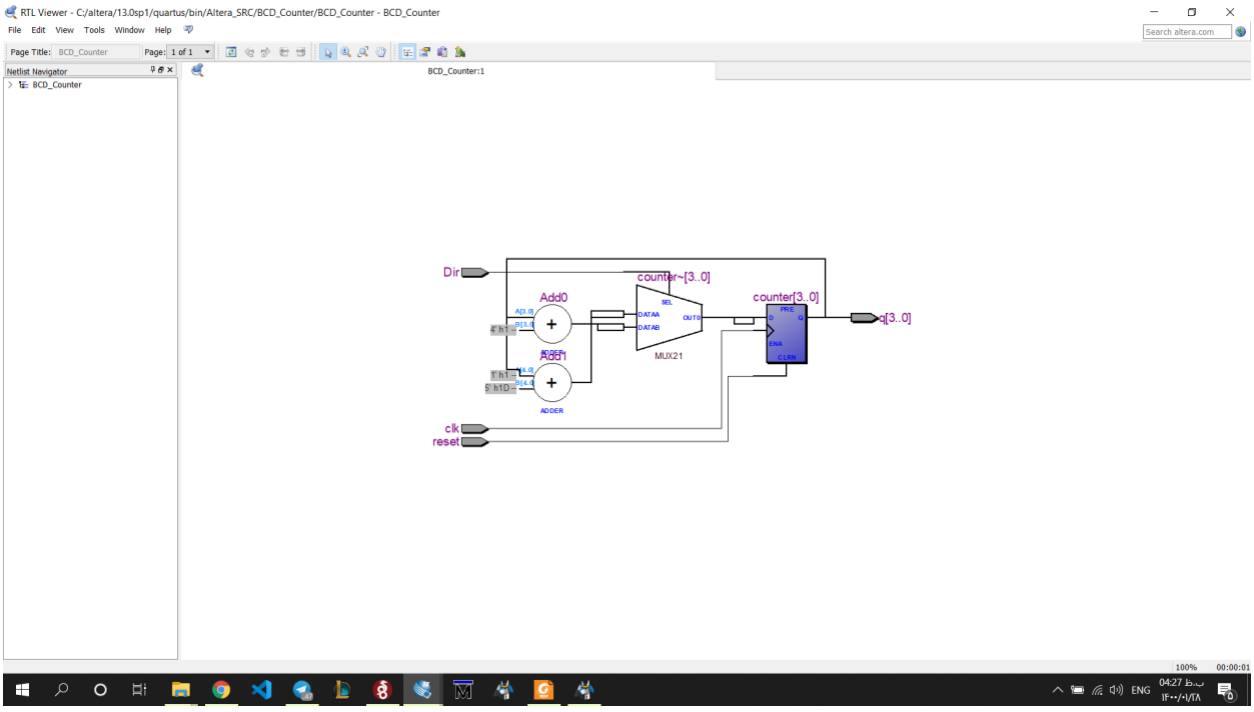
Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity BCD_Counter is port(
    clk, reset: in std_logic;
    Dir: in std_logic;
    q: out std_logic_vector(3 downto 0)
    );
end BCD_Counter;

architecture arch of BCD_Counter is
    signal counter: unsigned(3 downto 0);

    begin
        process(clk, reset)
            begin
                if (reset = '1') then
                    counter <= (others => '0');
                elsif (clk'event and clk = '1') then
                    if (Dir = '1') then
                        counter <= counter + 1;
                    elsif (Dir = '0') then
                        counter <= counter - 1;
                    end if;
                end if;
            end process;

        q <= std_logic_vector(counter);

    end arch;
```

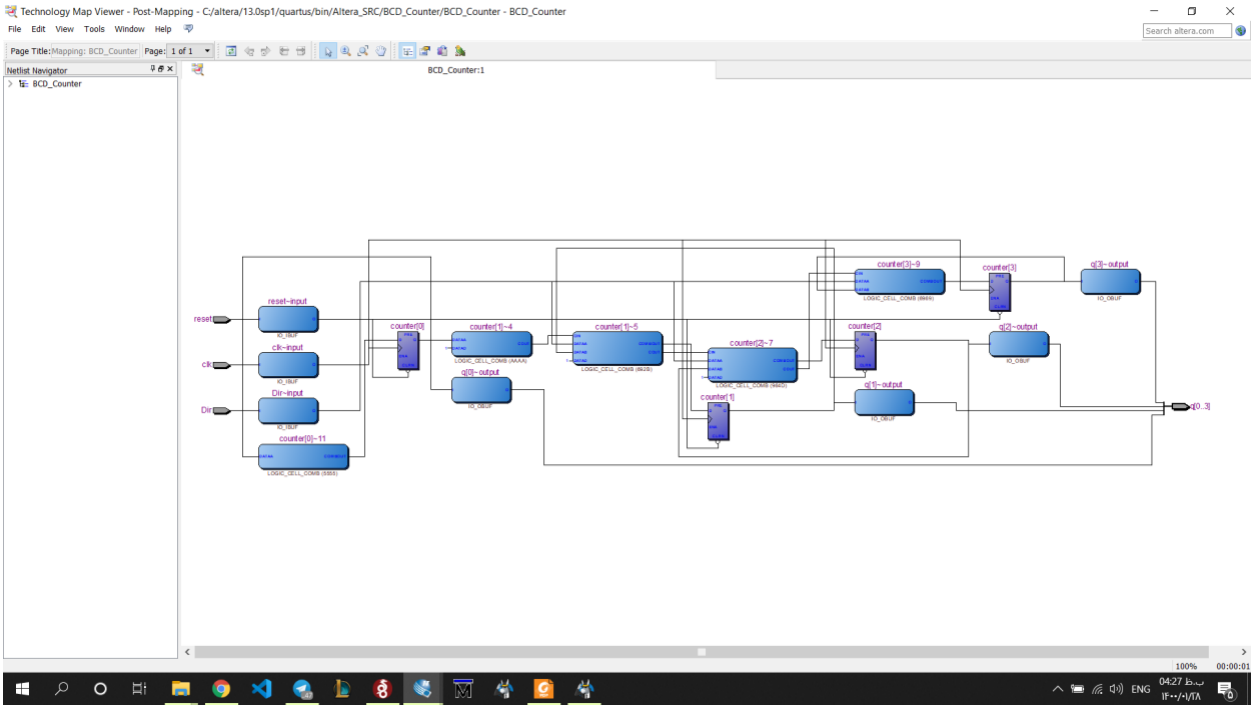
Compilation report



RTL



Post-Mapping



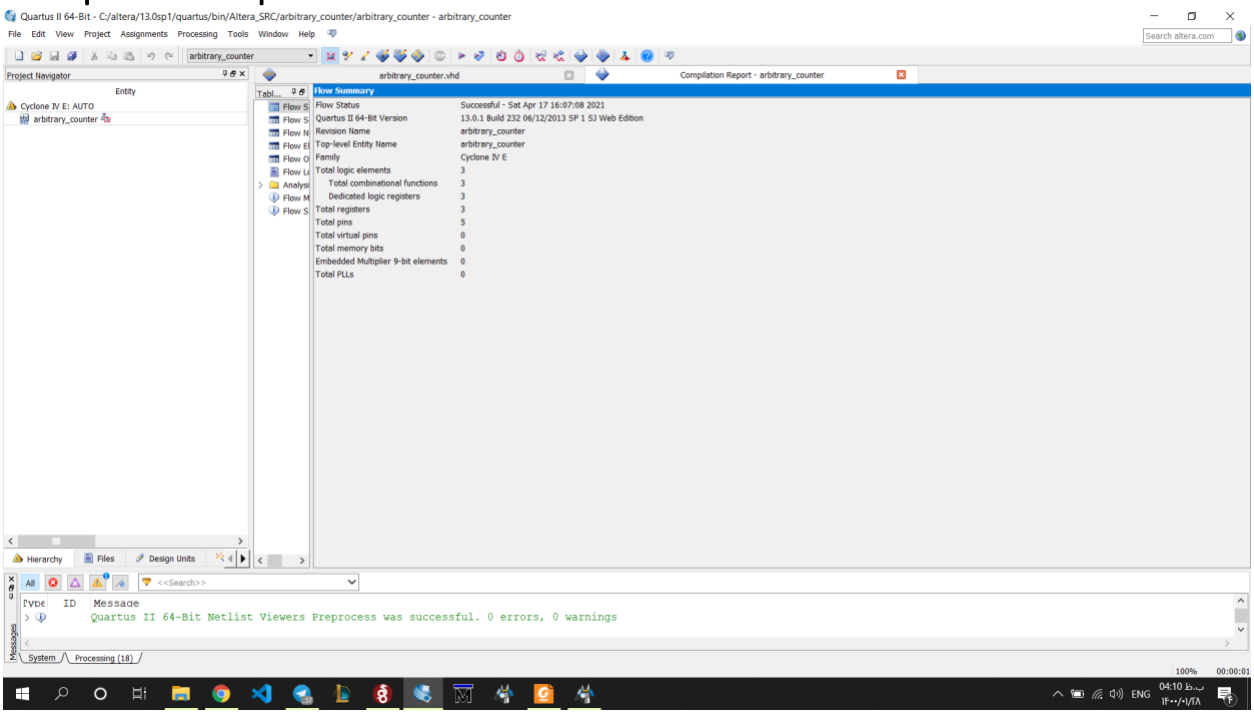
Question3

Code

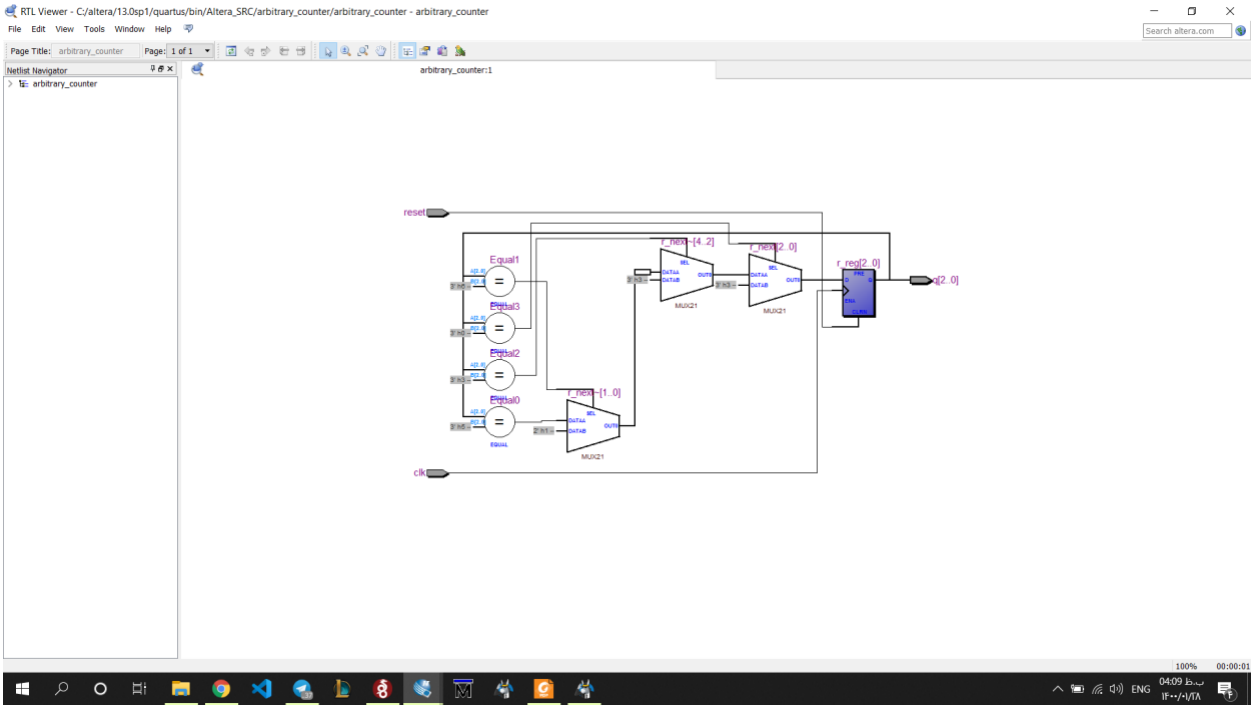
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity arbitrary_counter is
    port(
    clk, reset: in std_logic;
    q: out std_logic_vector(2 downto 0)
    );
end arbitrary_counter;

architecture arch of arbitrary_counter is
    signal r_reg: std_logic_vector(2 downto 0);
    signal r_next: std_logic_vector(2 downto 0);
```

```
  begin
      process(clk, reset)
          begin
              if (reset = '1') then
                  r_reg <= (others => '0');
              elsif (clk'event and clk = '1') then
                  r_reg <= r_next;
              end if;
          end process;

      r_next <=   "011" when r_reg="000" else
                  "110" when r_reg="011" else
                  "101" when r_reg="110" else
                  "111" when r_reg="101" else
                  "000";

      q <= r_reg;
end arch;
```

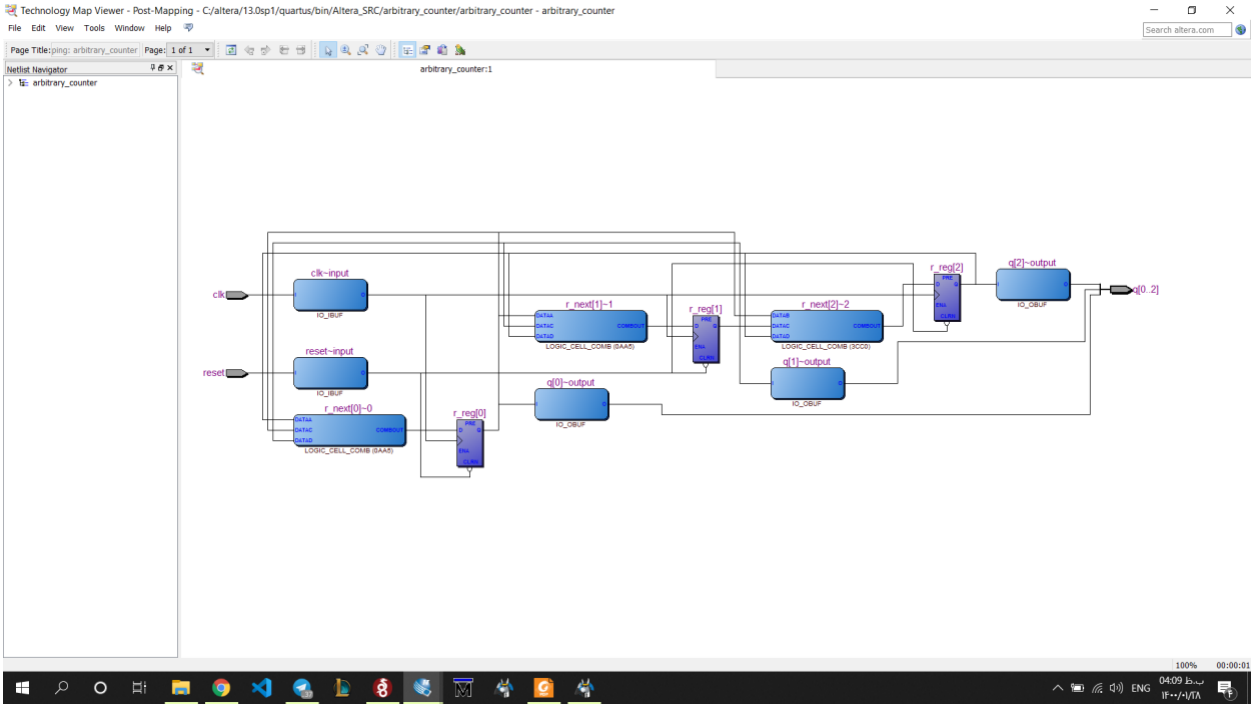
Compilation report



RTL



Post-Mapping



Question4

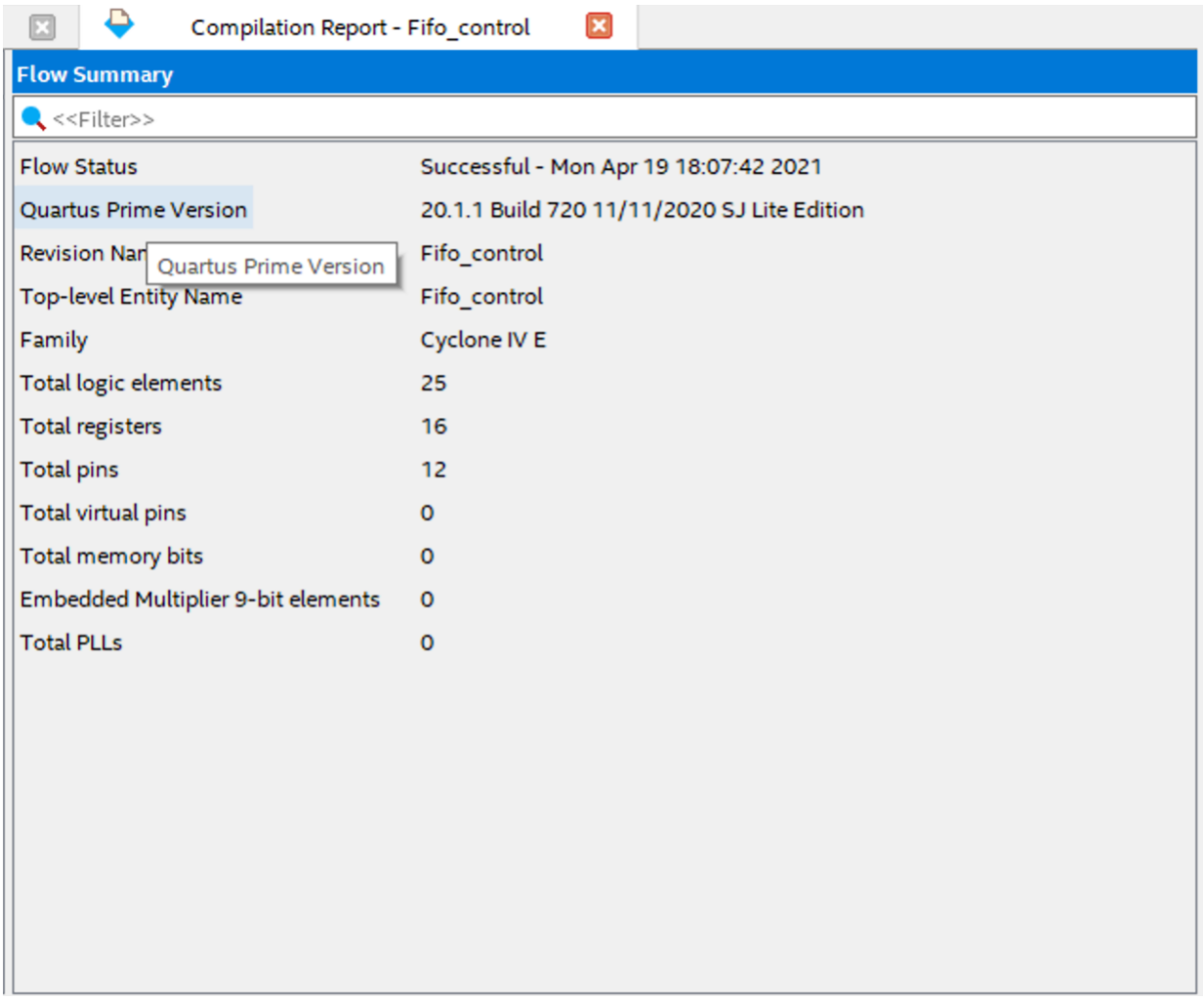
Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
-- use ieee.numeric_std.all;
-- use IEEE.STD_LOGIC_UNSIGNED.all;
entity Fifo_control is
    port (
            clk, reset : in std_logic;
            wr,rd      : in std_logic;
         full, empty    : out std_logic;
    w_address,r_address : out std_logic_vector (2 downto 0) );
end Fifo_control;

architecture arch of Fifo_control is
        signal reader_pointer : unsigned(3 downto 0) := "0000";
        signal writer_pointer : unsigned(3 downto 0) := "0000";
        -- signal reader_pointer : std_logic_vector(3 downto 0);
        -- signal writer_pointer : std_logic_vector(3 downto 0);
        signal full_fifo      : std_logic;
        signal empty_fifo     : std_logic;


    begin
      process(wr,clk,reset)
          begin
             if(reset = '1') then
                    -- reader_pointer <= "0000";
                    writer_pointer <= "0000";
                    full_fifo      <= '0';
                    -- empty_fifo     <= '0';
             elsif(clk'event and clk ='1') then
```

```
            if(wr = '1')then
                if((reader_pointer(2 downto 0) = writer_pointer(2 downto 0)) and (reader_pointer(3) /=
writer_pointer(3)))then
                    full_fifo <= '1';
                elsif(writer_pointer = "1111") then
                    writer_pointer <= "0000";
                else
                    writer_pointer <= writer_pointer + 1;
                end if;
                if(full_fifo = '1') then
                    full <= '1';
                else
                    -- i don't know what todod
                    -- maybe send w_address
                    w_address <= std_logic_vector(writer_pointer(2 downto 0));
                    -- w_address <= writer_pointer(2 downto 0);
                end if;
            end if;
        end if;
    end process;

    process(rd,clk,reset)
        begin
        if(reset = '1') then
        reader_pointer <= "0000";
        -- writer_pointer <= "0000";
        -- full_fifo      <= '0';
        empty_fifo     <= '0';
        elsif(clk'event and clk ='1') then
            if(rd = '1') then
            if(reader_pointer = writer_pointer) then
                empty_fifo <= '1';
            elsif(reader_pointer = "1111") then
                reader_pointer <= "0000";
            else
                reader_pointer <= reader_pointer + 1;
            end if;
```

```
                if(empty_fifo = '1') then
                    empty <= '1';
                else
                    -- i don't know what todod
                    -- maybe send r_address
                    r_address <= std_logic_vector(reader_pointer(2 downto 0));
                    -- r_address <= reader_pointer(2 downto 0);
                end if;
            end if;
        end if;
    end process;



end architecture;
```

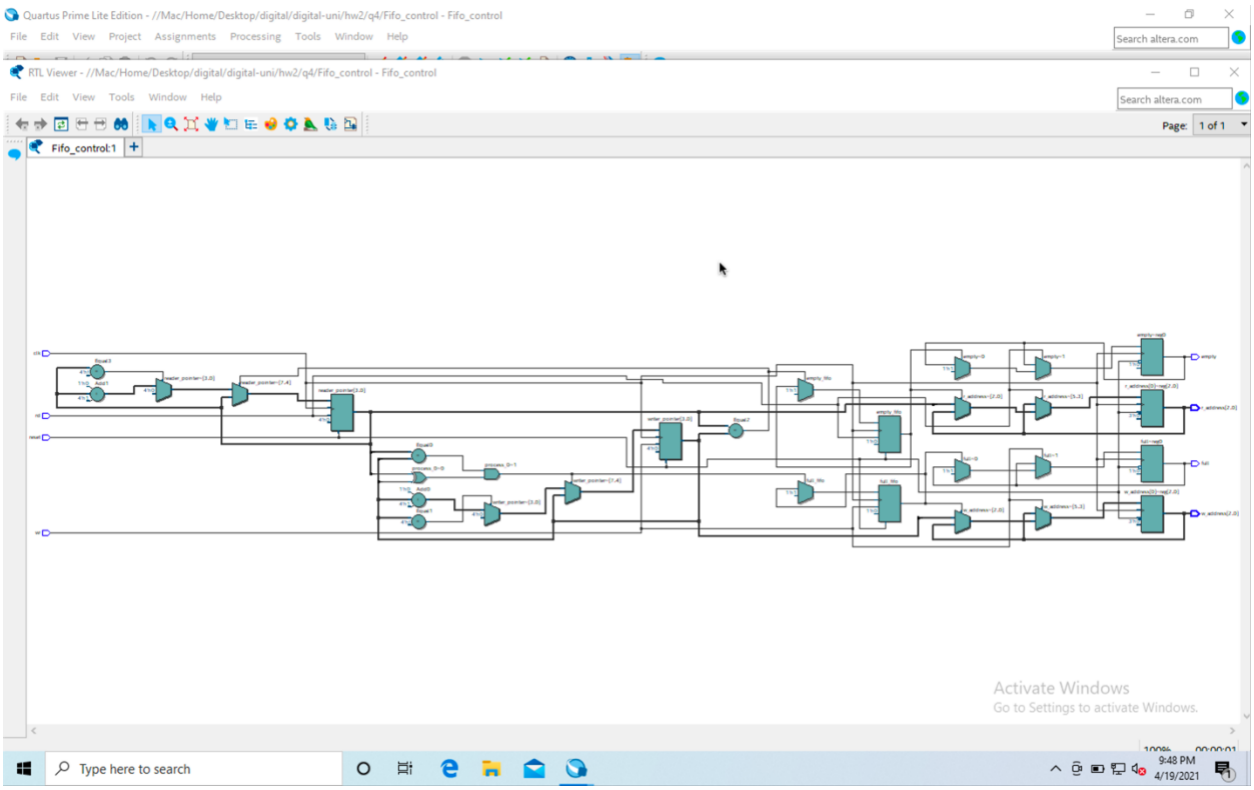
Compilation report



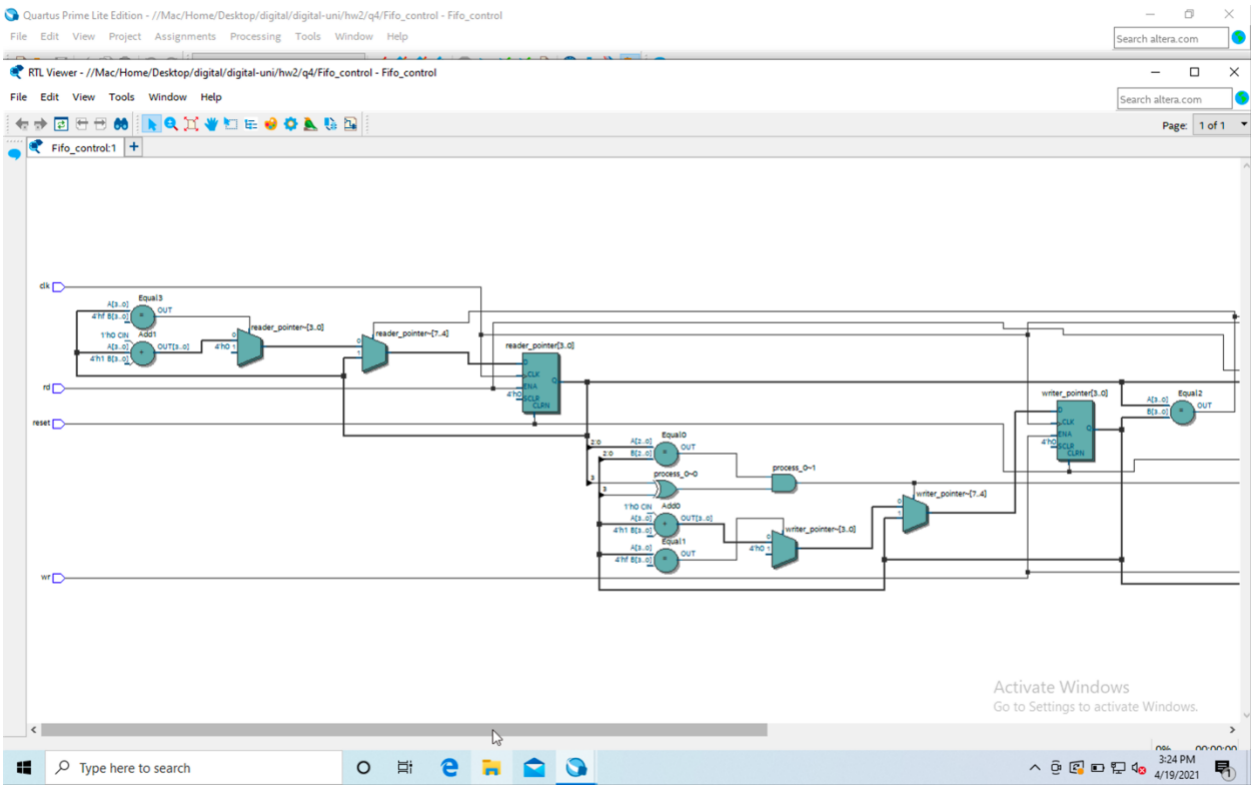
RTL

این عکس به دلیل سخت خواندن به۲ قسمت تقسیم شده اند

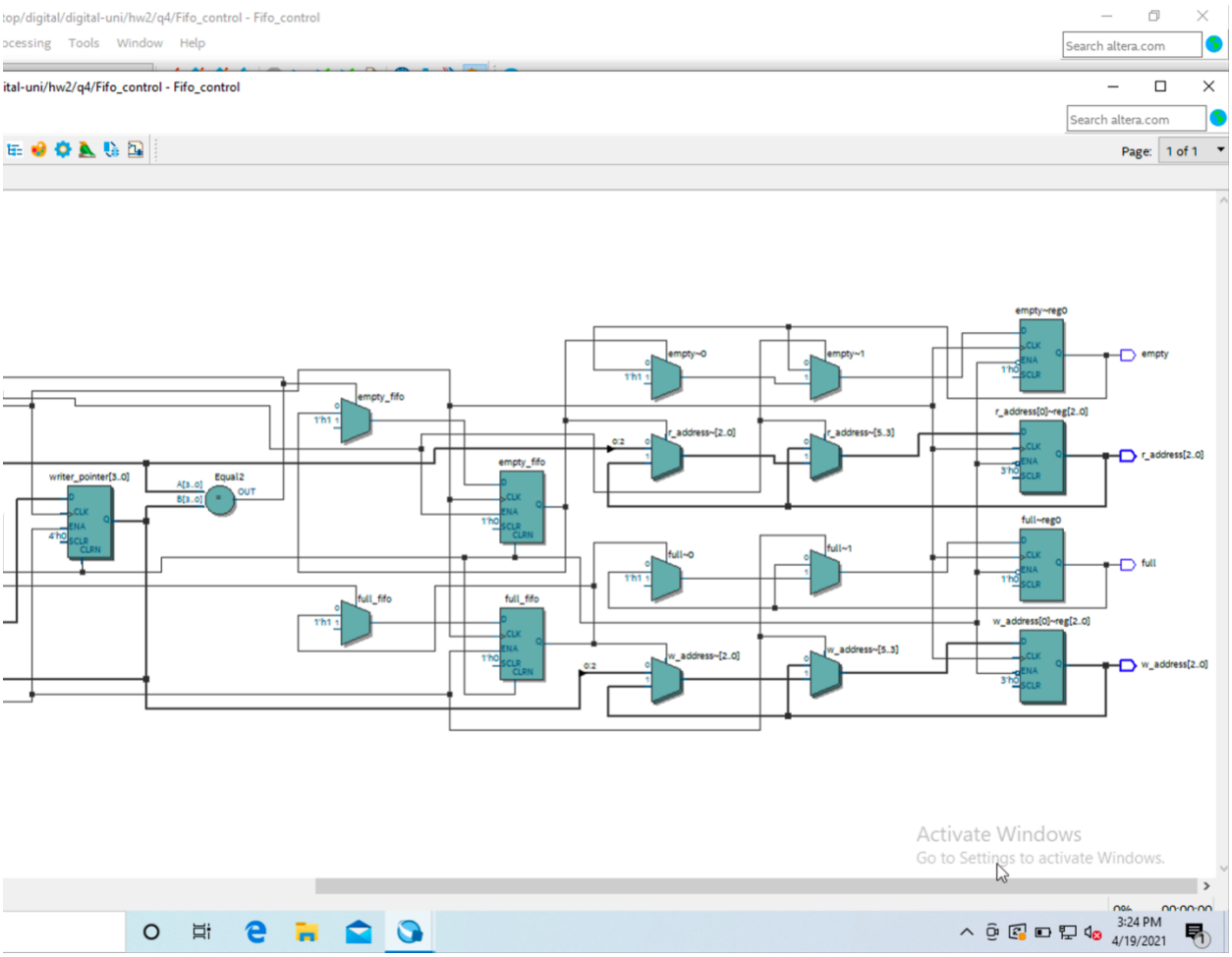
عکس اصلی


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Project Assignments Processing Tools Window Help
RTL Viewer - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Tools Window Help
Page: 1 of 1
Fifo_control:1
Activate Windows
Go to Settings to activate Windows.
Type here to search
9:48 PM
4/19/2021

عکس اول


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
RTL Viewer - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
Fifo_control:1
clk
rd
reset
wr
reader_pointer[3..0]
reader_pointer~[3..0]
reader_pointer~[7..4]
writer_pointer[3..0]
writer_pointer~[3..0]
writer_pointer~[7..4]
process_0~0
process_0~1
Equal0
Equal1
Equal2
Equal3
Add0
Add1
Activate Windows
Go to Settings to activate Windows.
Type here to search
3:24 PM
4/19/2021

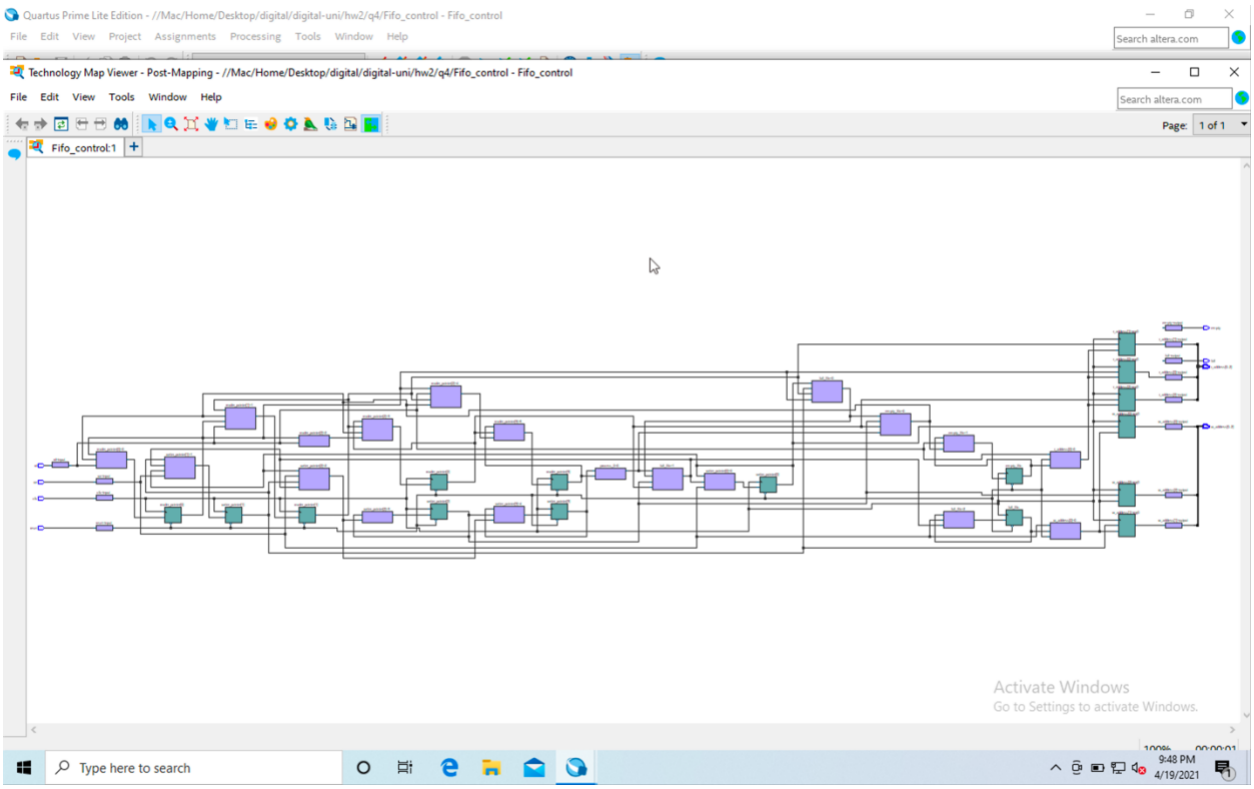
عکس دوم



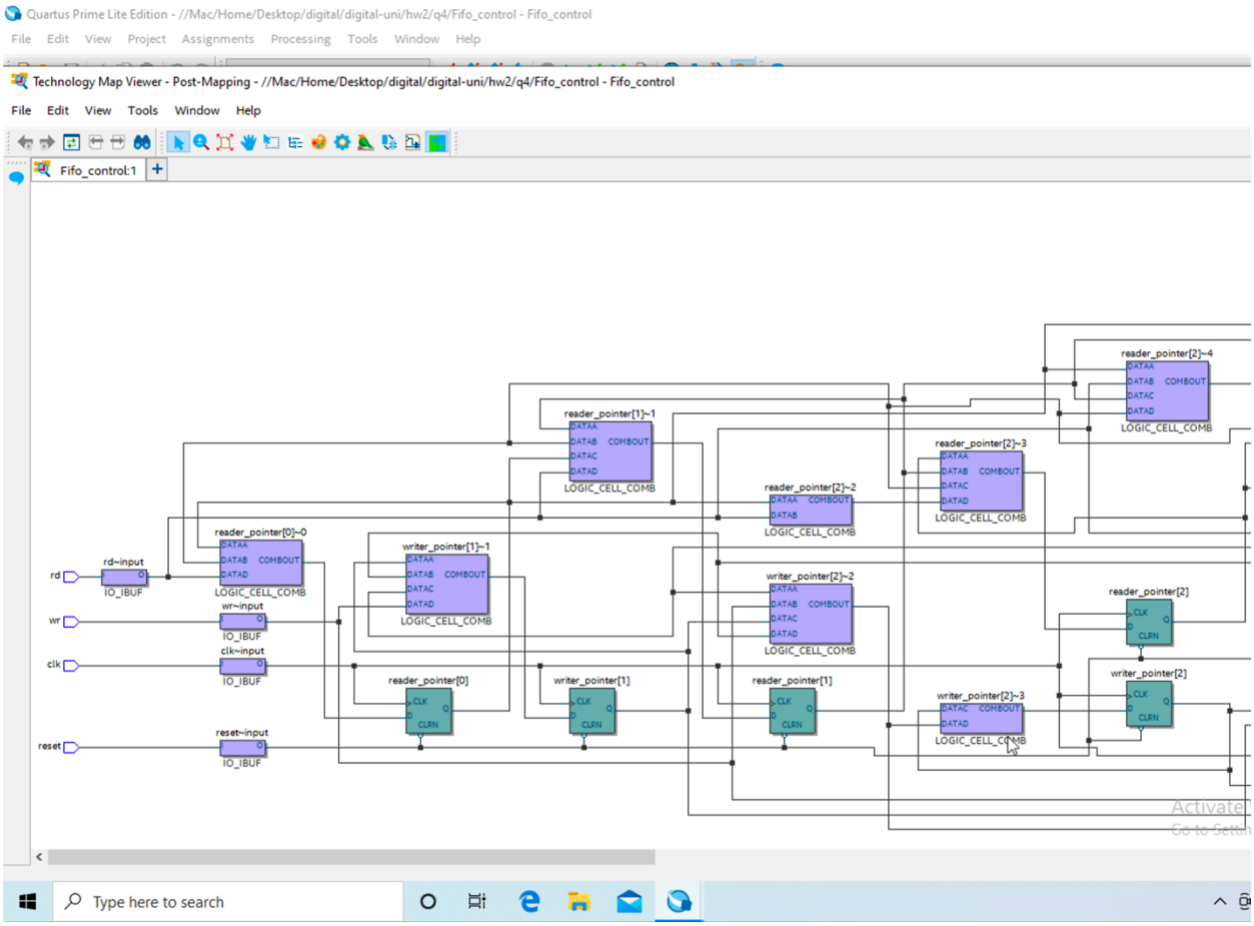
Post-mapping

این عکس به دلیل سخت خواندن به ۳ قسمت تقسیم شده اند

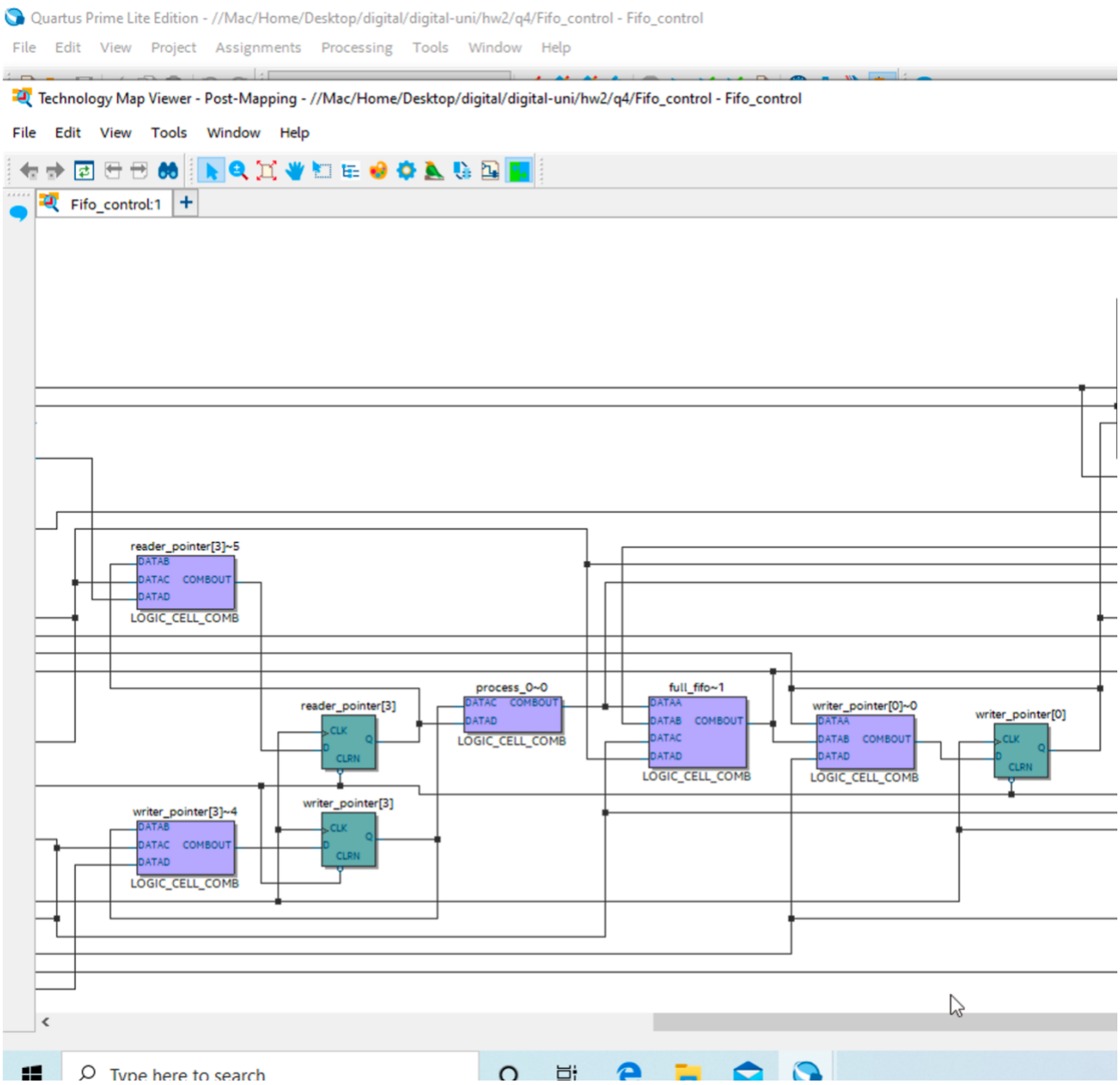
عکس اصلی


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Technology Map Viewer - Post-Mapping - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Fifo_control:1
Activate Windows
Go to Settings to activate Windows.
Type here to search
9:48 PM
4/19/2021

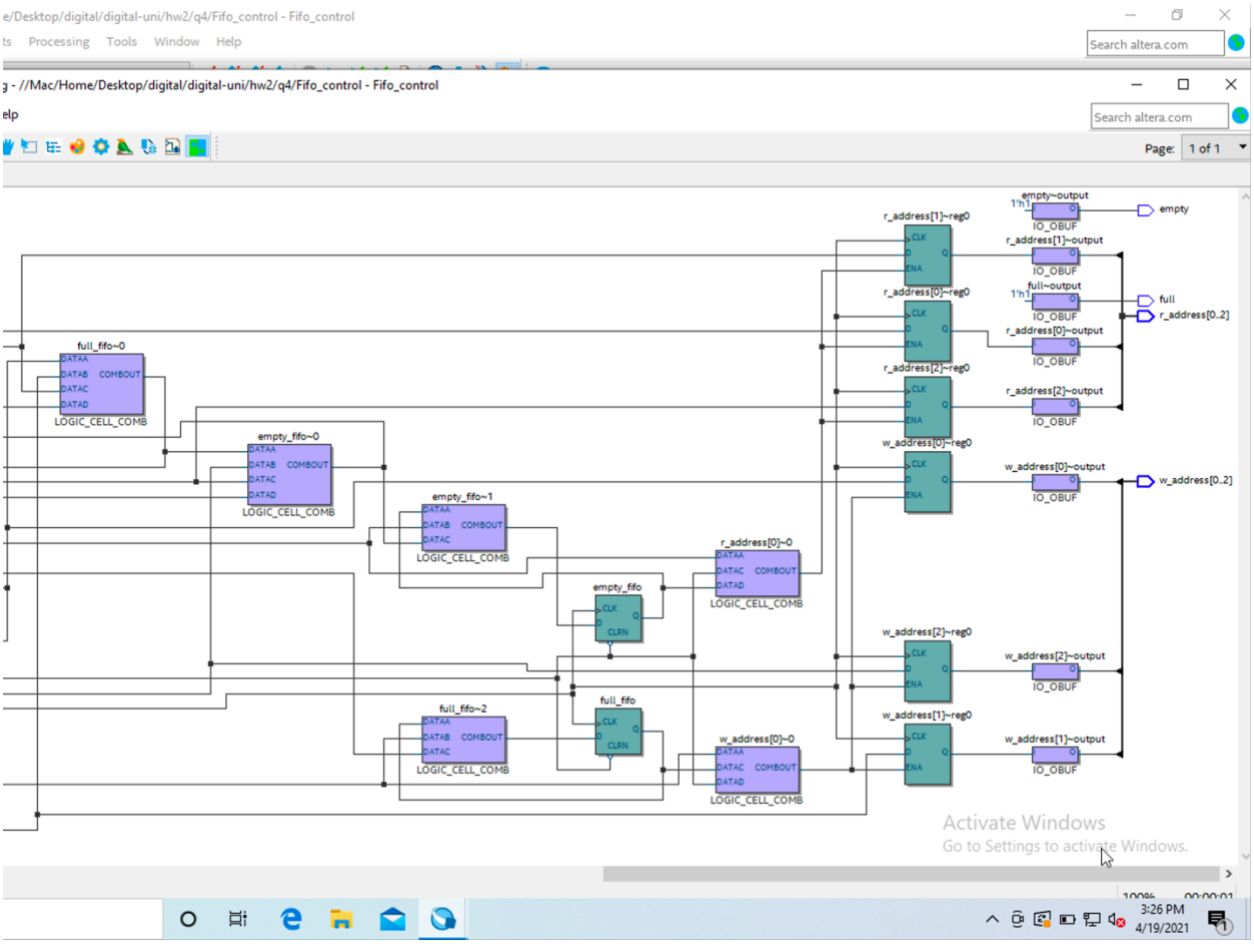
عکس اول


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Project Assignments Processing Tools Window Help
Technology Map Viewer - Post-Mapping - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Tools Window Help
Fifo_control:1
rd
wr
clk
reset
rd~input
wr~input
clk~input
reset~input
IO_IBUF
reader_pointer[0]~0
reader_pointer[1]~1
reader_pointer[2]~2
reader_pointer[2]~3
reader_pointer[2]~4
writer_pointer[1]~1
writer_pointer[2]~2
writer_pointer[2]~3
reader_pointer[0]
reader_pointer[1]
reader_pointer[2]
writer_pointer[1]
writer_pointer[2]
LOGIC_CELL_COMB
Type here to search

عکس دوم


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Project Assignments Processing Tools Window Help
Technology Map Viewer - Post-Mapping - //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
File Edit View Tools Window Help
Fifo_control:1
reader_pointer[3]~5
DATAB
DATAC COMBOUT
DATAD
LOGIC_CELL_COMB
reader_pointer[3]
CLK Q
D
CLRN
process_0~0
DATAC COMBOUT
DATAD
LOGIC_CELL_COMB
full_fifo~1
DATAA
DATAB COMBOUT
DATAC
DATAD
LOGIC_CELL_COMB
writer_pointer[0]~0
DATAA
DATAB COMBOUT
DATAD
LOGIC_CELL_COMB
writer_pointer[0]
CLK Q
D
CLRN
writer_pointer[3]~4
DATAB
DATAC COMBOUT
DATAD
LOGIC_CELL_COMB
writer_pointer[3]
CLK Q
D
CLRN
Type here to search

عکس سوم


e/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
Processing Tools Window Help
Search altera.com
- //Mac/Home/Desktop/digital/digital-uni/hw2/q4/Fifo_control - Fifo_control
elp
Search altera.com
Page: 1 of 1
full_fifo~0
LOGIC_CELL_COMB
empty_fifo~0
LOGIC_CELL_COMB
empty_fifo~1
LOGIC_CELL_COMB
empty_fifo
full_fifo~2
LOGIC_CELL_COMB
full_fifo
r_address[0]~0
LOGIC_CELL_COMB
w_address[0]~0
LOGIC_CELL_COMB
r_address[1]~reg0
r_address[0]~reg0
r_address[2]~reg0
w_address[0]~reg0
w_address[2]~reg0
w_address[1]~reg0
empty~output
IO_OBUF
empty
r_address[1]~output
full~output
full
r_address[0..2]
r_address[0]~output
r_address[2]~output
w_address[0]~output
w_address[0..2]
w_address[2]~output
w_address[1]~output
Activate Windows
Go to Settings to activate Windows.
3:26 PM
4/19/2021