طراحی سیستم های دیجیتال
تکلیف اول

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کسری رشیدفر

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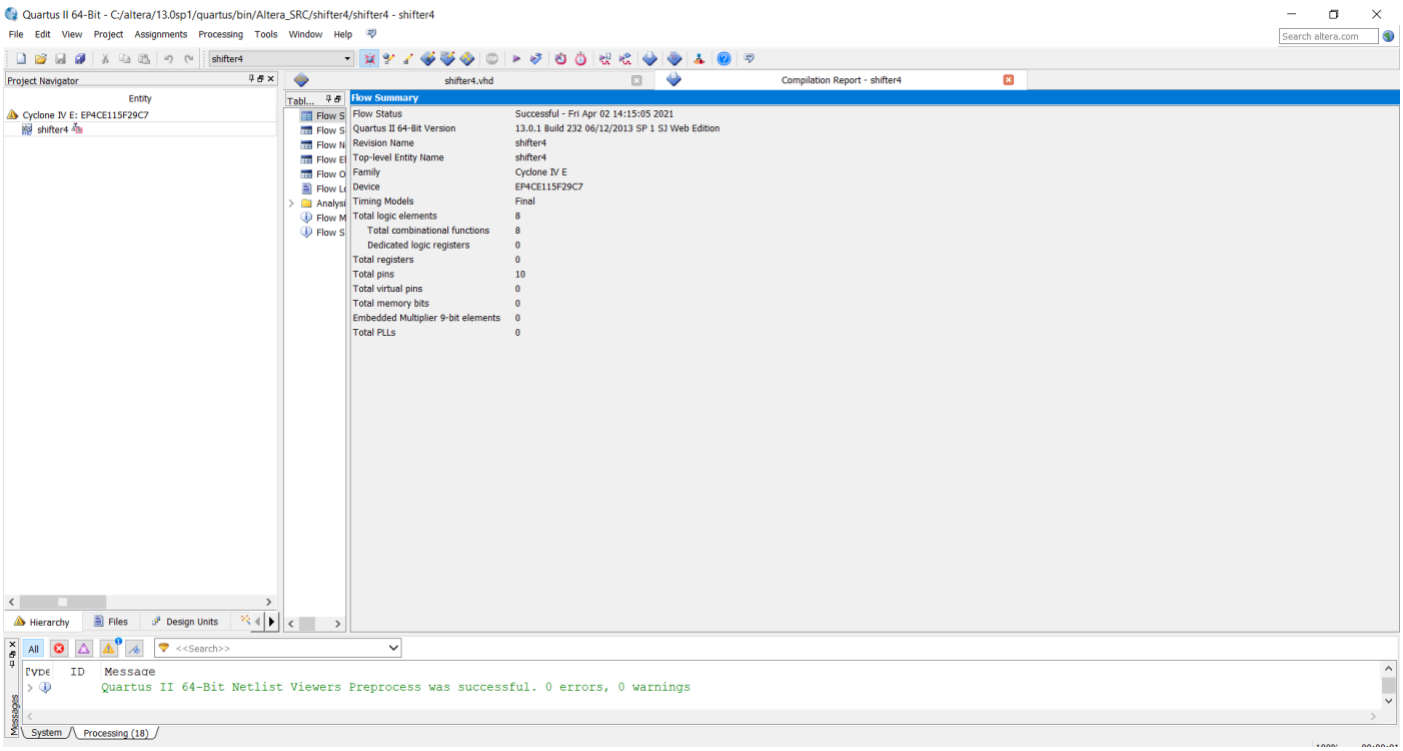
Question1

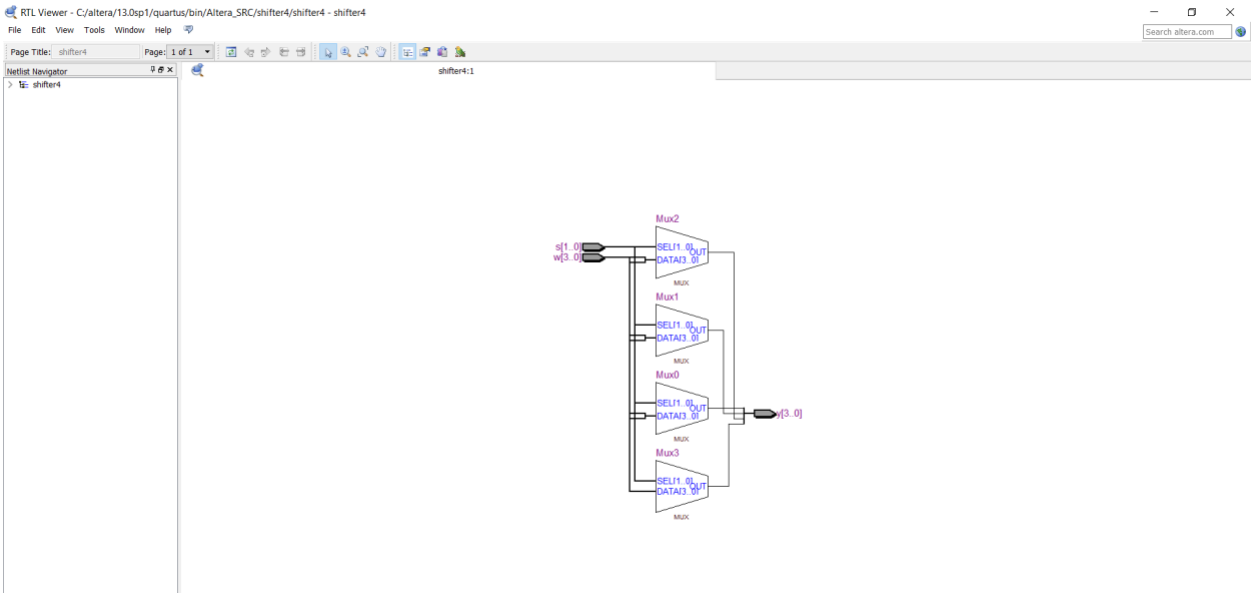
Code

```
library ieee;
use ieee.std_logic_1164.all;

entity shifter4 is
  port(
    s: in  std_logic_vector(1 downto 0);
    w: in  std_logic_vector(3 downto 0);
    y: out std_logic_vector(3 downto 0)
  );
end shifter4;

architecture sel_shift of shifter4 is
begin
  with s select
    y <= (w(3) & w(2) & w(1) & w(0)) when "00",
      (w(0) & w(3) & w(2) & w(1)) when "01",
      (w(1) & w(0) & w(3) & w(2)) when "10",
      (w(2) & w(1) & w(0) & w(3)) when others;
end sel_shift;
```

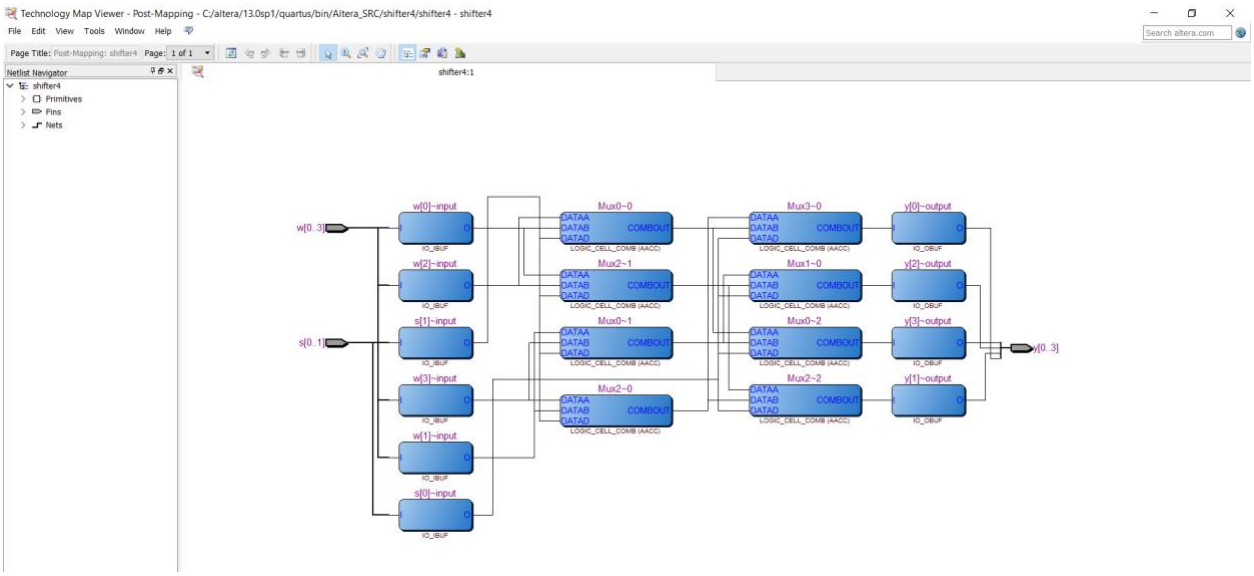
Compilation report



RTL



Post-Mapping



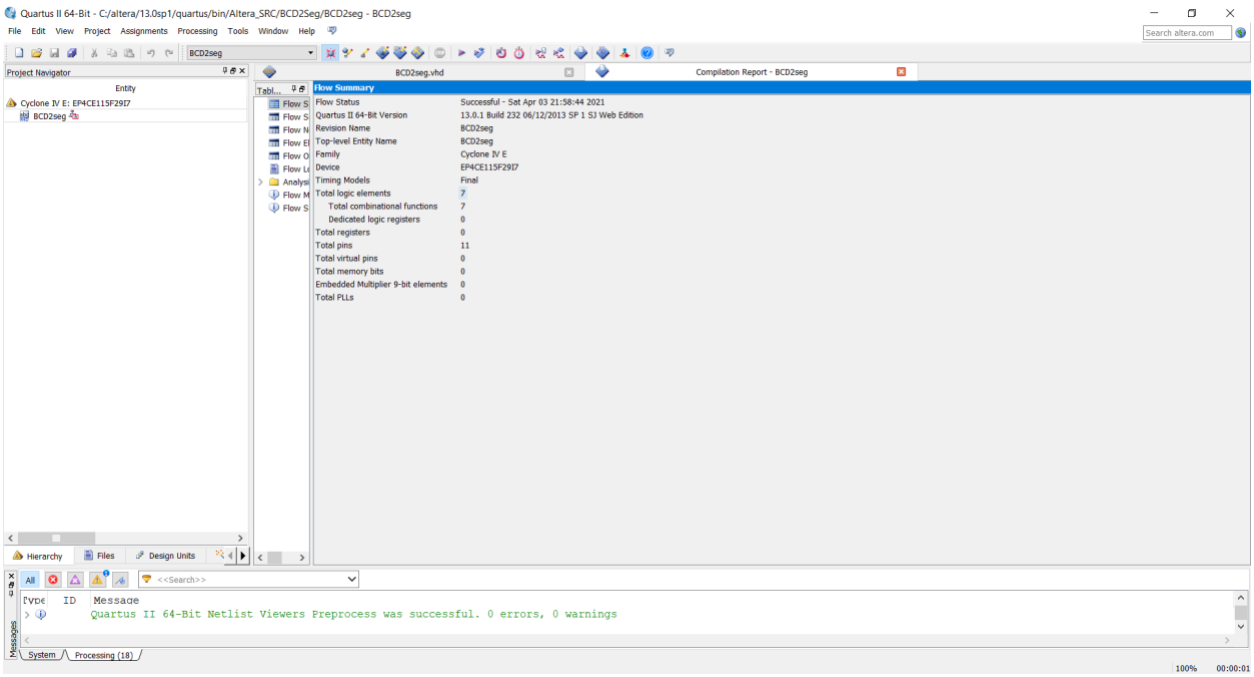
Question2

Code

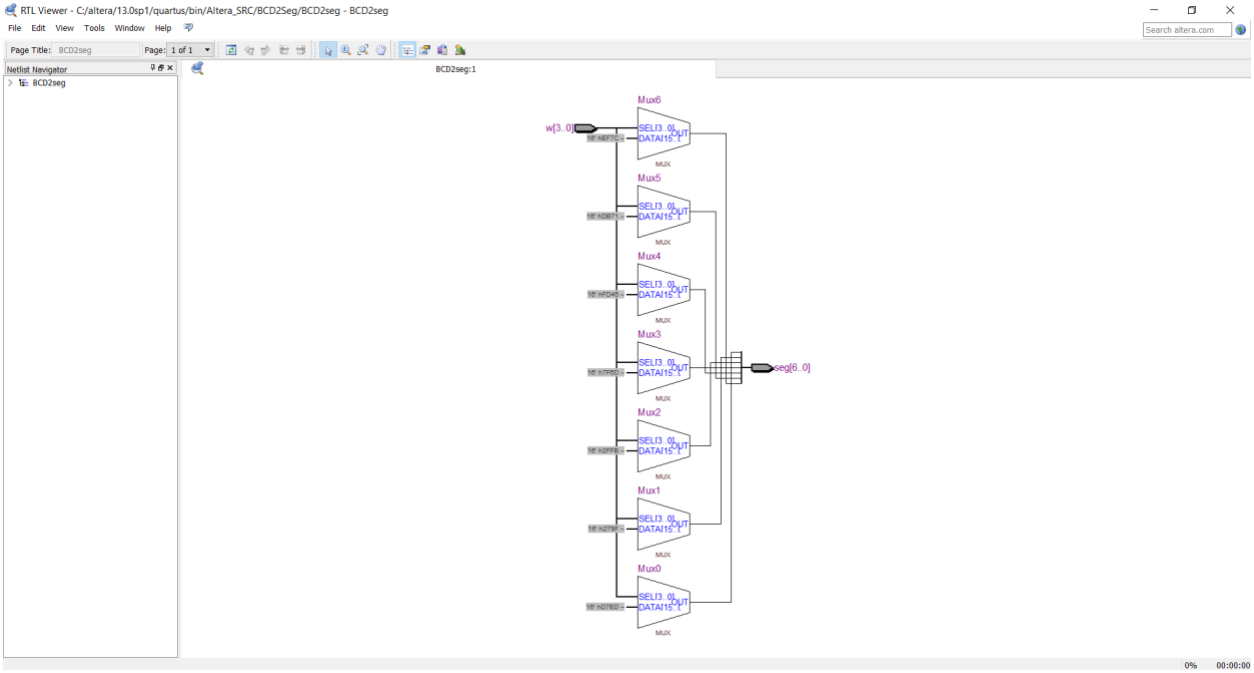
```
library ieee;
use ieee.std_logic_1164.all;

entity BCD2seg is
    port(
        w: in std_logic_vector(3 downto 0);
        seg: out std_logic_vector(6 downto 0));
    end BCD2seg;

architecture decoder_arch of BCD2seg is
    begin
        process(w)
        begin
        case w is
            when "0000" =>
                seg <= "1111110";
            when "0001" =>
                seg <= "0110000";
```

```
        when "0010" =>
            seg <= "1101101";
        when "0011" =>
            seg <= "1111001";
        when "0100" =>
            seg <= "0110011";
        when "0101" =>
            seg <= "1011011";
        when "0110" =>
            seg <= "1011111";
        when "0111" =>
            seg <= "1110000";
        when "1000" =>
            seg <= "1111111";
        when "1001" =>
            seg <= "1111011";
        when "1010" =>
            seg <= "1111101";
        when "1011" =>
            seg <= "0011111";
        when "1100" =>
            seg <= "1001110";
        when "1101" =>
            seg <= "0111101";
        when "1110" =>
            seg <= "1001111";
        when others =>
            seg <= "1000111";
    end case;
    end process;
end decoder_arch;
```

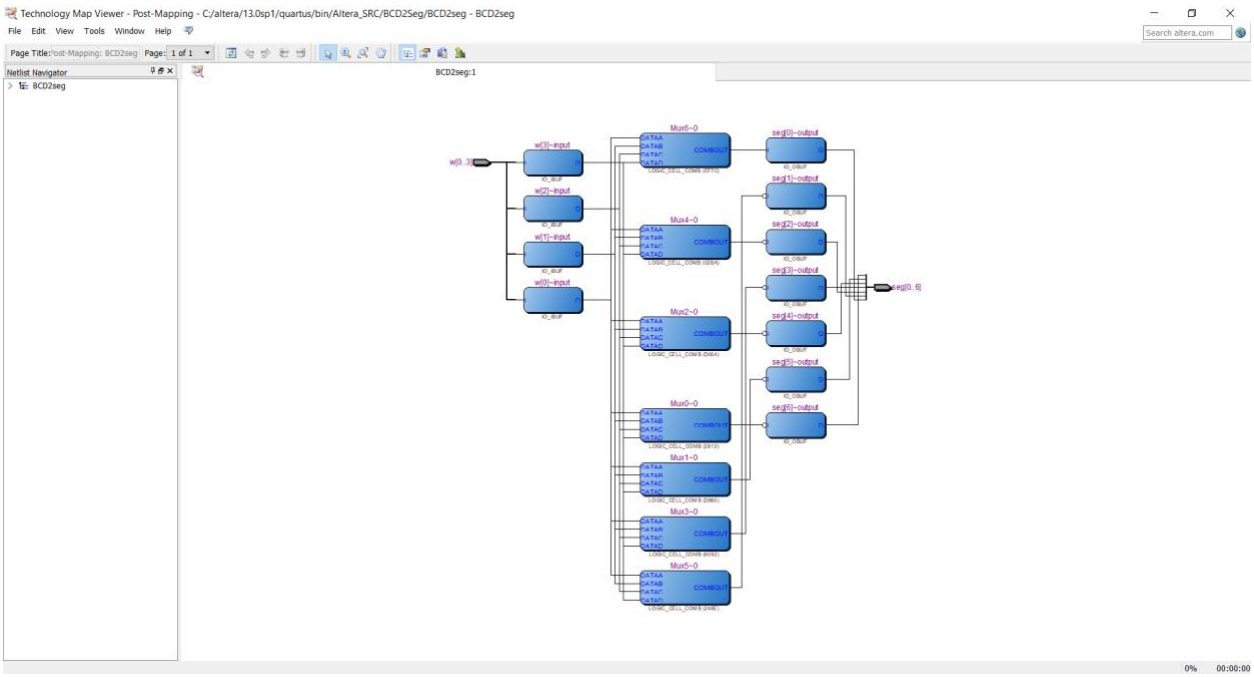
Compilation report



RTL



Post-Mapping

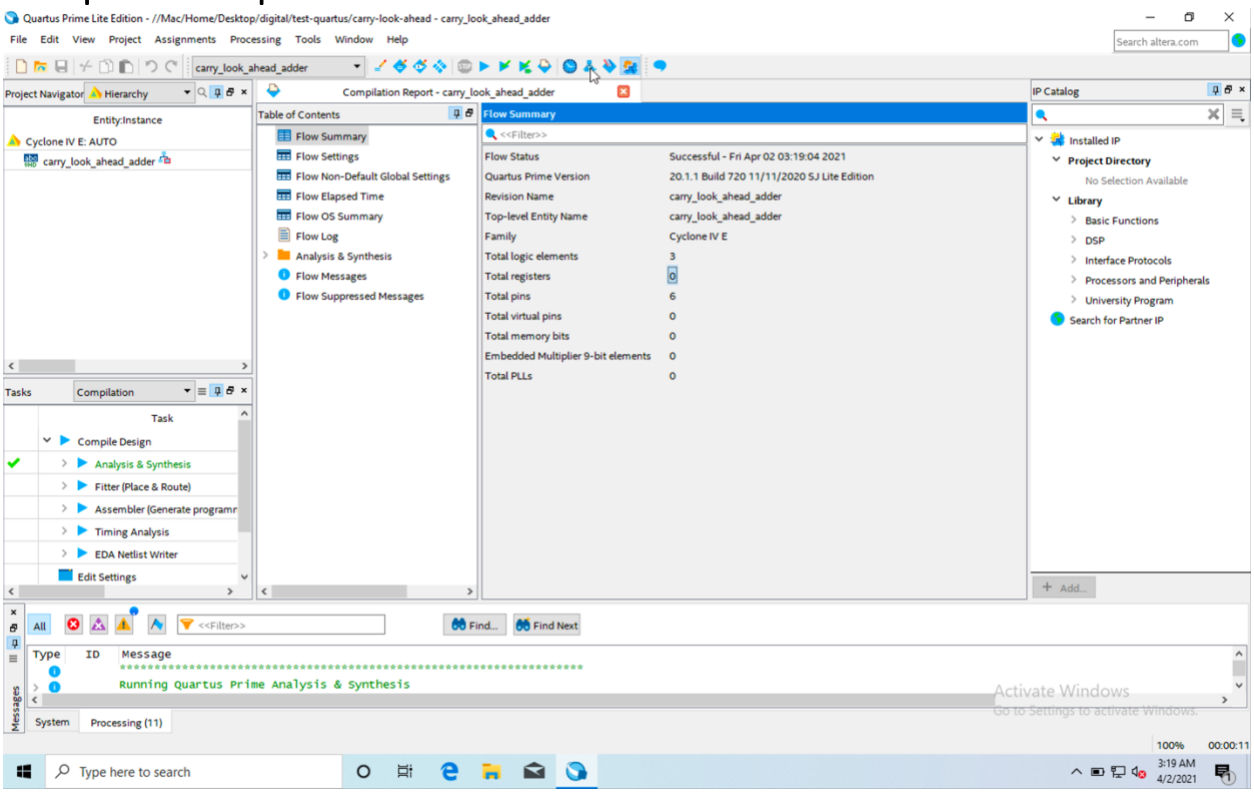


Question3

Code

```
library ieee;
use ieee.std_logic_1164.all;


entity carry_look_ahead_adder is
port(
   input1,input2,carryIn : in bit;
   sum,gen,propagate : out bit);
end entity;

architecture struct of carry_look_ahead_adder is

begin
    sum <= (input1 xor input2) xor carryIn;
    propagate <= input1 xor input2;
    gen <= input1 and input2;
end architecture;
```

Compilation report



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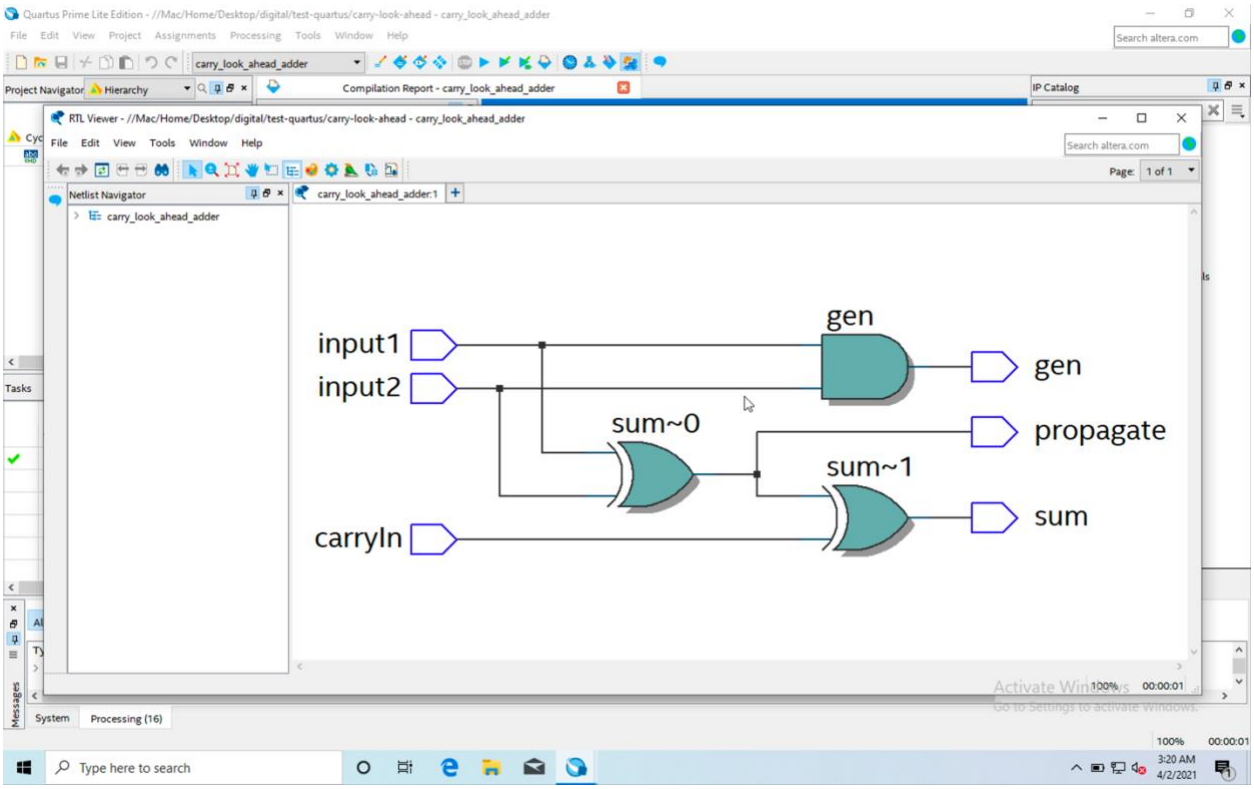
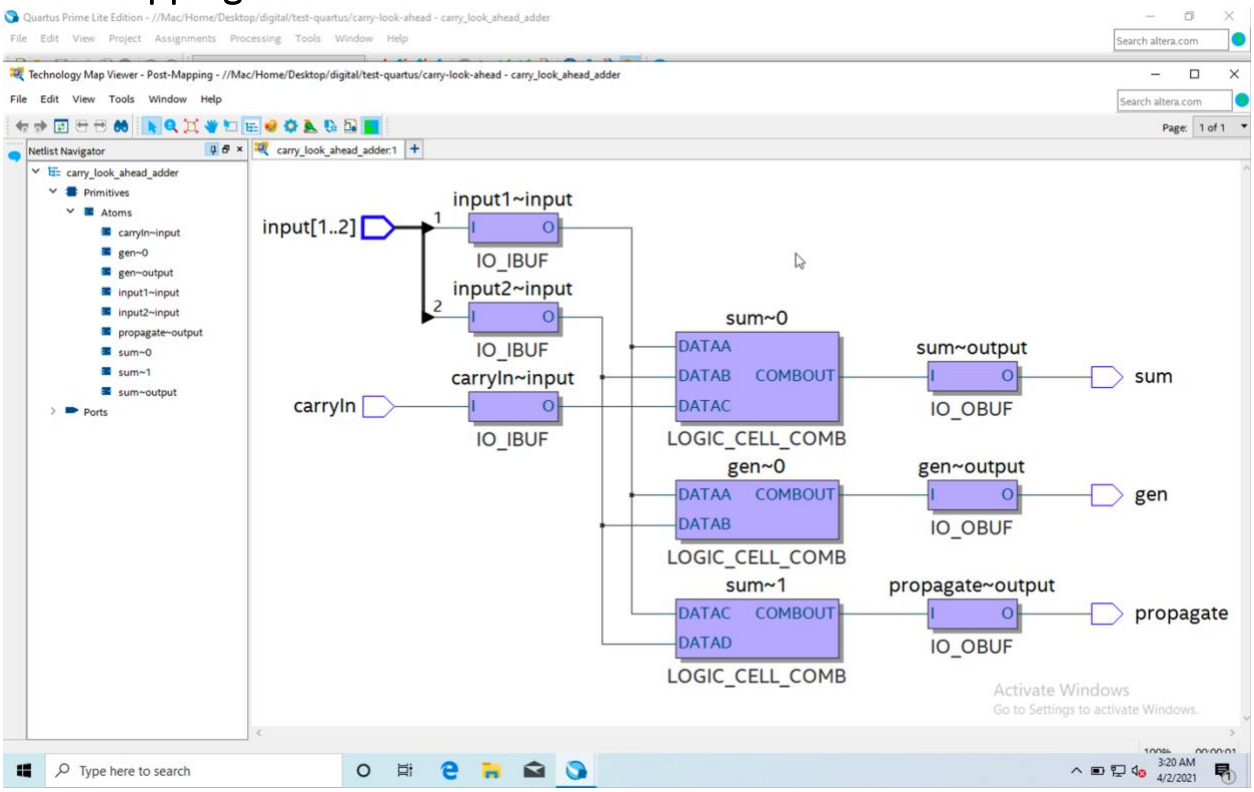
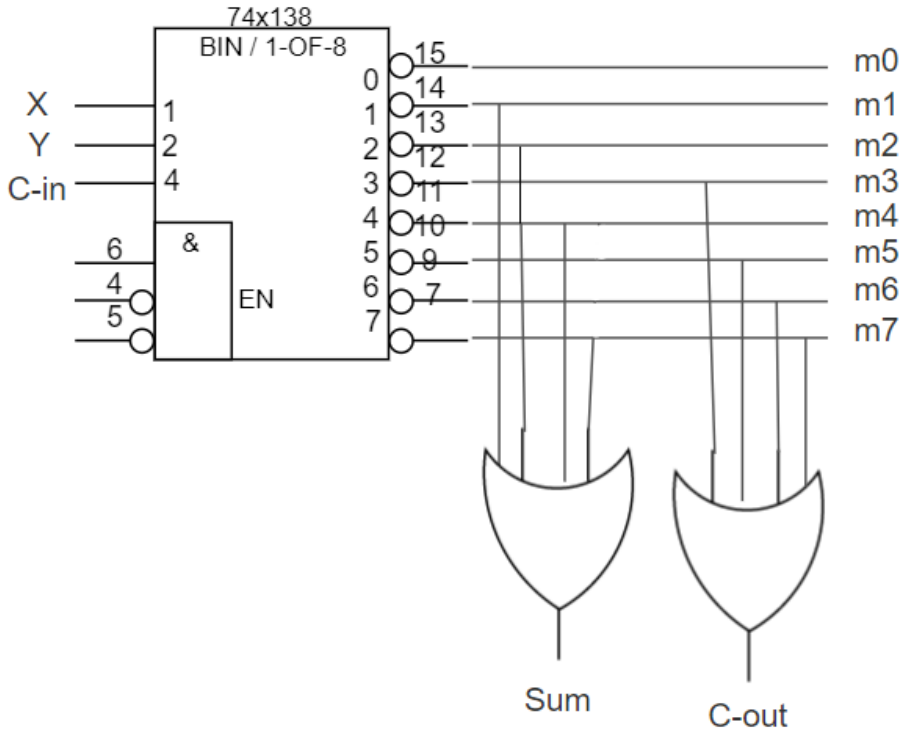


Post-Mapping



Question4

A


74x138
BIN / 1-OF-8
X
Y
C-in
1
2
4
6
4
5
&
EN
0
1
2
3
4
5
6
7
15
14
13
12
11
10
9
7
m0
m1
m2
m3
m4
m5
m6
m7
Sum
C-out

B

Code

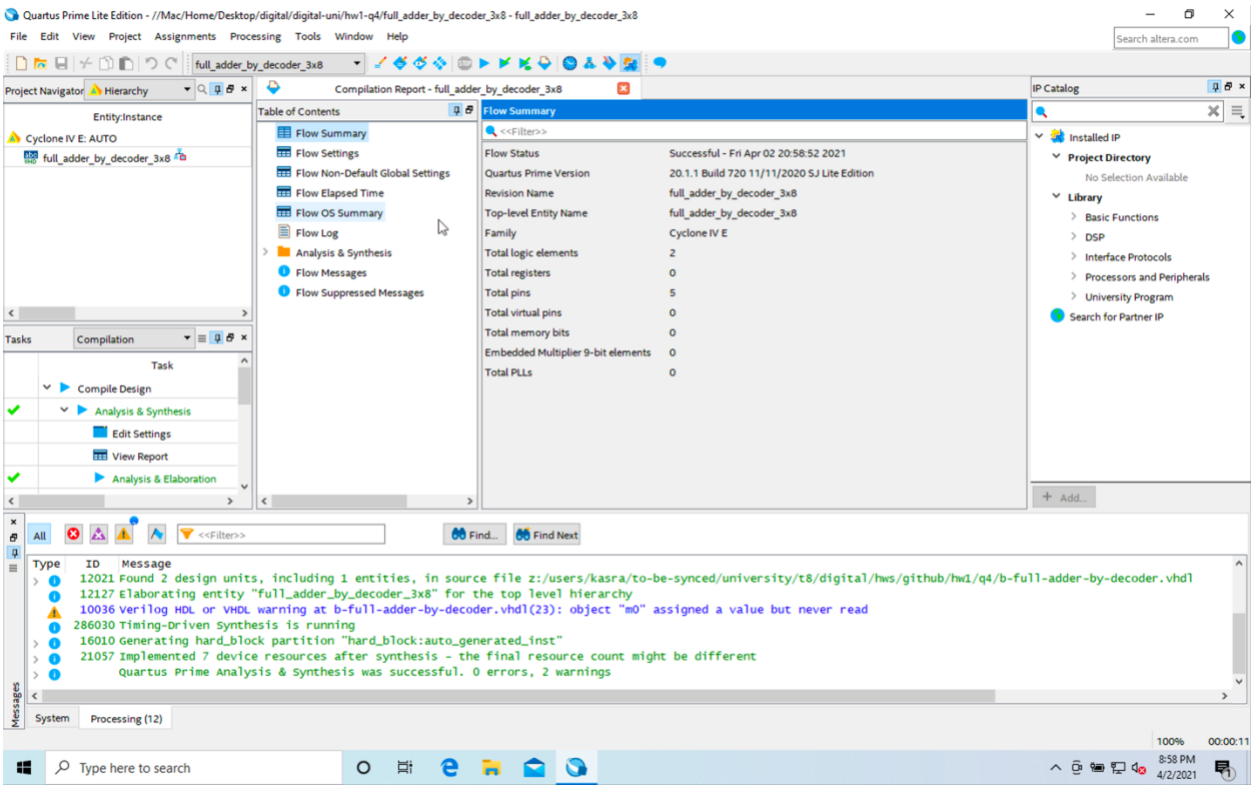
```
library ieee;
use ieee.std_logic_1164.all;
entity full_adder_by_decoder_3x8 is
port(
  inputDecoder    : in STD_LOGIC_VECTOR(2 downto 0);
  sum      : out std_logic;
  carryOut : out std_logic);
end entity;

architecture struct of full_adder_by_decoder_3x8 is
   signal outPutDecoder : STD_LOGIC_VECTOR(7 downto 0);
begin
   -- to see where  m1,m2,m3,... come from, pleas pay attention to  answer of  section a
   outPutDecoder <=("10000000") when (inputDecoder="000") else
                   ("01000000") when (inputDecoder="001") else
                   ("00100000") when (inputDecoder="010") else
                   ("00010000") when (inputDecoder="011") else
                   ("00001000") when (inputDecoder="100") else
                   ("00000100") when (inputDecoder="101") else
                   ("00000010") when (inputDecoder="110") else
                   ("00000001");
   process(outPutDecoder) is
   variable m0,m1,m2,m3,m4,m5,m6,m7 : STD_LOGIC;
   begin
      m0 :='0';
      m1 :='0';
      m2 :='0';
      m3 :='0';
      m4 :='0';
      m5 :='0';
      m6 :='0';
      m7 :='0';
      case outPutDecoder is
```

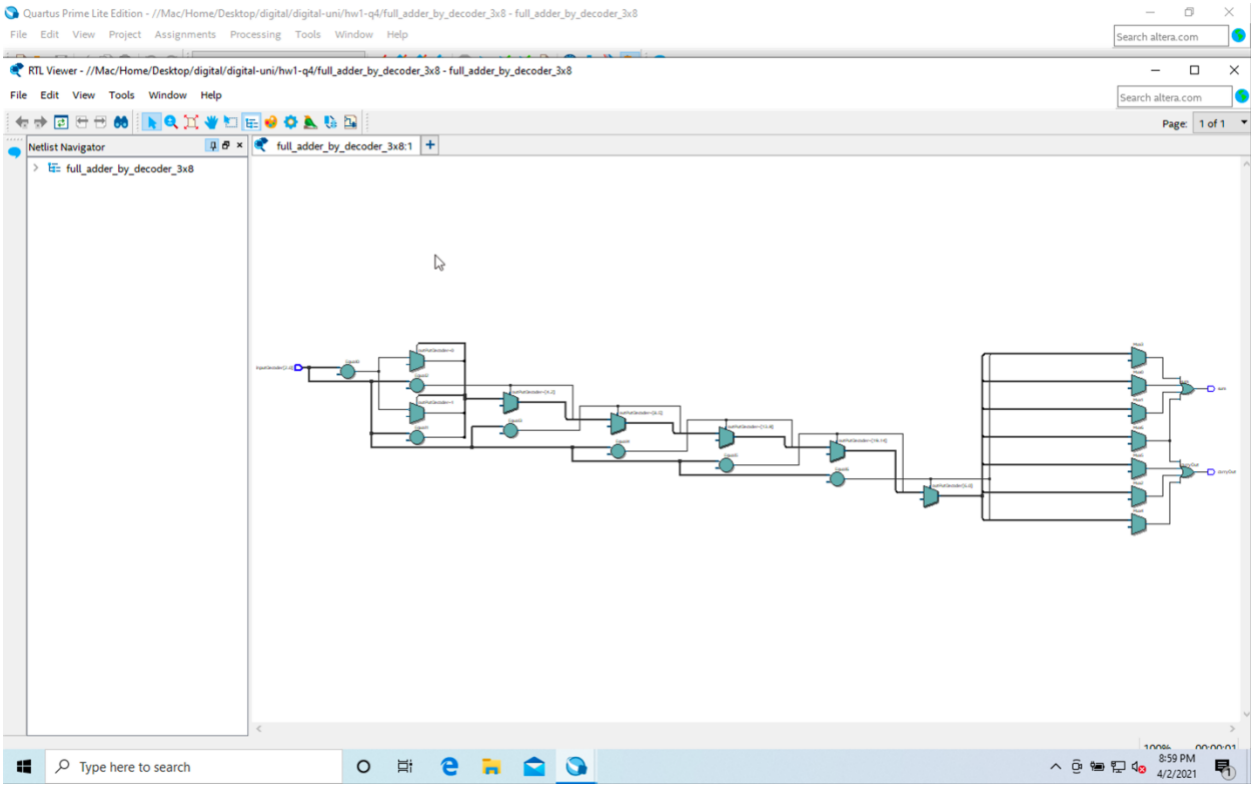
```
        when "10000000" =>
            m0 := '1';
        when "01000000" =>
            m1 := '1';
        when "00100000" =>
            m2 := '1';
        when "00010000" =>
            m3 := '1';
        when "00001000" =>
            m4 := '1';
        when "00000100" =>
            m5 := '1';
        when "00000010" =>
            m6 := '1';
        when others =>
            m7 := '1';
      end case;


    sum      <= m1 OR m2 OR m4 OR m7;
    carryOut <= m3 OR m5 OR m6 Or m7;
  end process;
end architecture;
```

Compilation report


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw1-q4/full_adder_by_decoder_3x8 - full_adder_by_decoder_3x8
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
full_adder_by_decoder_3x8
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: AUTO
full_adder_by_decoder_3x8
Compilation Report - full_adder_by_decoder_3x8
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Flow Messages
Flow Suppressed Messages
Flow Summary
<<Filter>>
Flow Status Successful - Fri Apr 02 20:58:52 2021
Quartus Prime Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name full_adder_by_decoder_3x8
Top-level Entity Name full_adder_by_decoder_3x8
Family Cyclone IV E
Total logic elements 2
Total registers 0
Total pins 5
Total virtual pins 0
Total memory bits 0
Embedded Multiplier 9-bit elements 0
Total PLLs 0
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
All
<<Filter>>
Find... Find Next
Type ID Message
12021 Found 2 design units, including 1 entities, in source file z:/users/kasra/to-be-synced/university/t8/digital/hws/github/hw1/q4/b-full-adder-by-decoder.vhdl
12127 Elaborating entity "full_adder_by_decoder_3x8" for the top level hierarchy
10036 Verilog HDL or VHDL warning at b-full-adder-by-decoder.vhdl(23): object "m0" assigned a value but never read
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 7 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings
Messages
System
Processing (12)
100%
00:00:11
Type here to search
8:58 PM
4/2/2021

RTL


Quartus Prime Lite Edition - //Mac/Home/Desktop/digital/digital-uni/hw1-q4/full_adder_by_decoder_3x8 - full_adder_by_decoder_3x8
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
RTL Viewer - //Mac/Home/Desktop/digital/digital-uni/hw1-q4/full_adder_by_decoder_3x8 - full_adder_by_decoder_3x8
File Edit View Tools Window Help
Search altera.com
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Netlist Navigator
full_adder_by_decoder_3x8
full_adder_by_decoder_3x8:1
Type here to search
8:59 PM
4/2/2021

Post-mapping