**Question1**

**Code**

library ieee;

use ieee.std\_logic\_1164.all;

entity shifter4 is

port(

s: in std\_logic\_vector(1 downto 0);

w: in std\_logic\_vector(3 downto 0);

y: out std\_logic\_vector(3 downto 0)

);

end shifter4;

architecture sel\_shift of shifter4 is

begin

with s select

y <= (w(3) & w(2) & w(1) & w(0)) when "00",

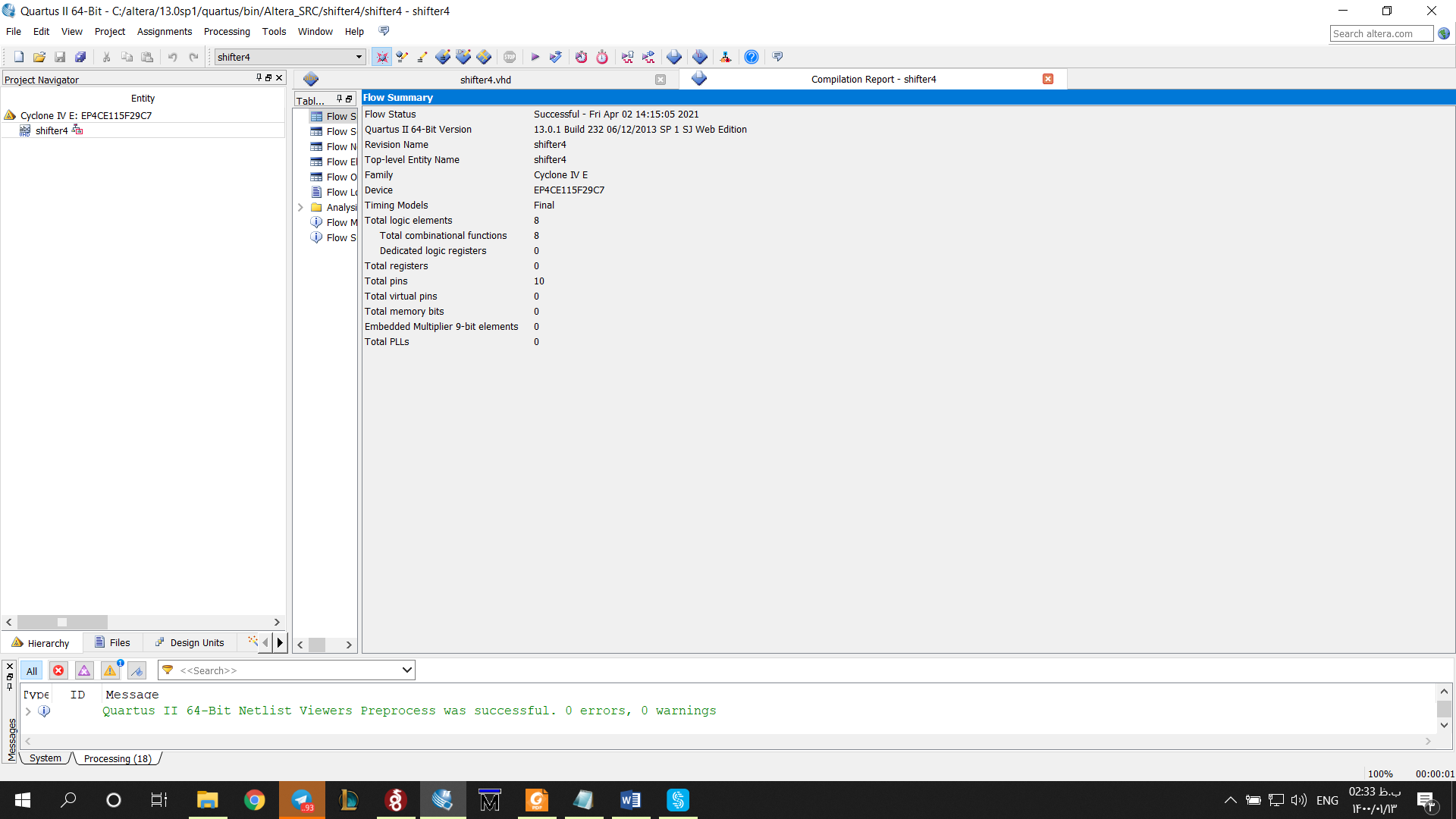
(w(0) & w(3) & w(2) & w(1)) when "01",

(w(1) & w(0) & w(3) & w(2)) when "10",

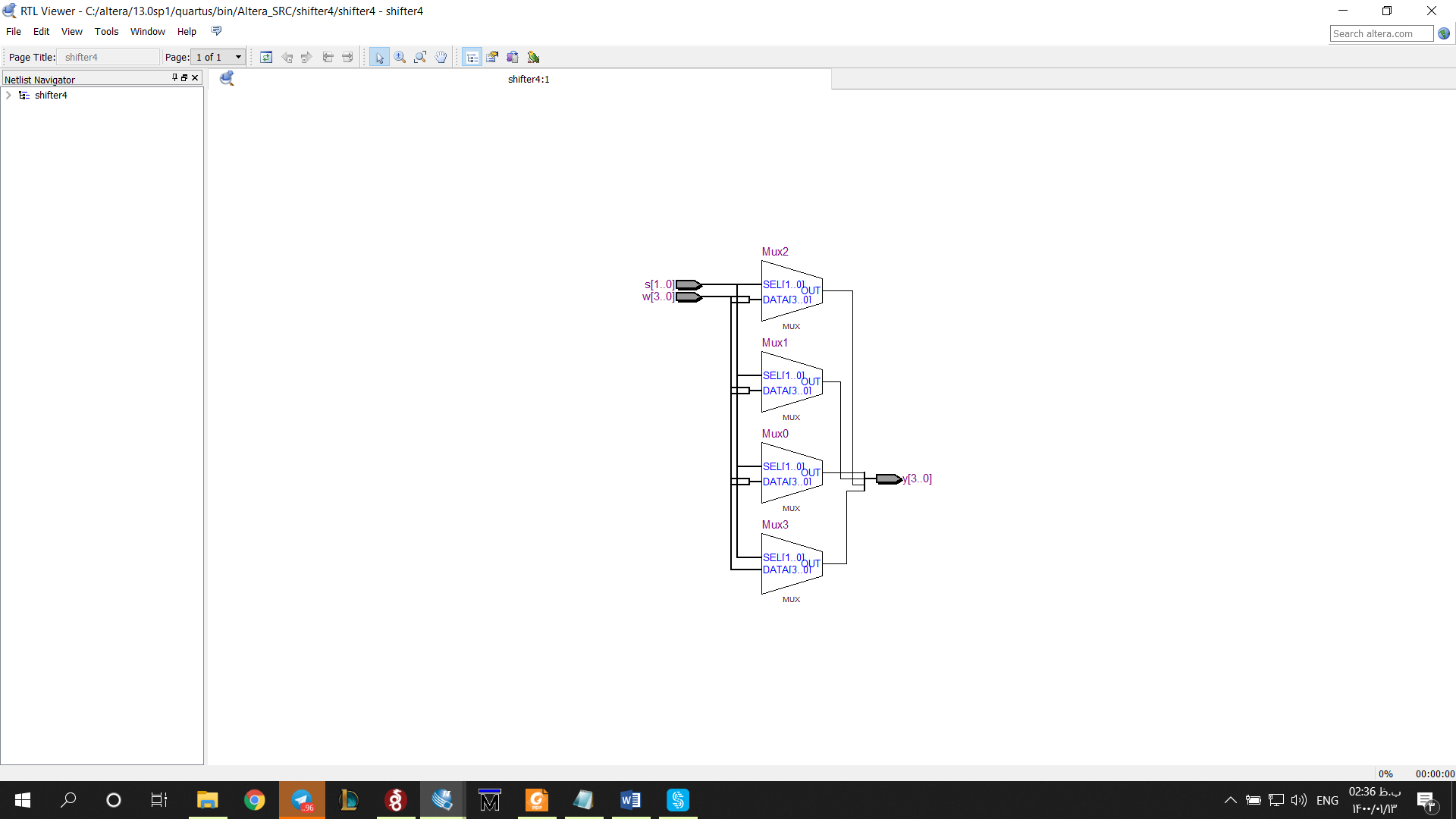
(w(2) & w(1) & w(0) & w(3)) when others;

end sel\_shift;

**Compilation report**



**RTL**



**Post-Mapping**

