**Question3**

**Code**

library ieee;

use ieee.std\_logic\_1164.all;

entity carry\_look\_ahead\_adder is

port(

input1,input2,carryIn : in bit;

sum,gen,propagate : out bit);

end entity;

architecture struct of carry\_look\_ahead\_adder is

begin

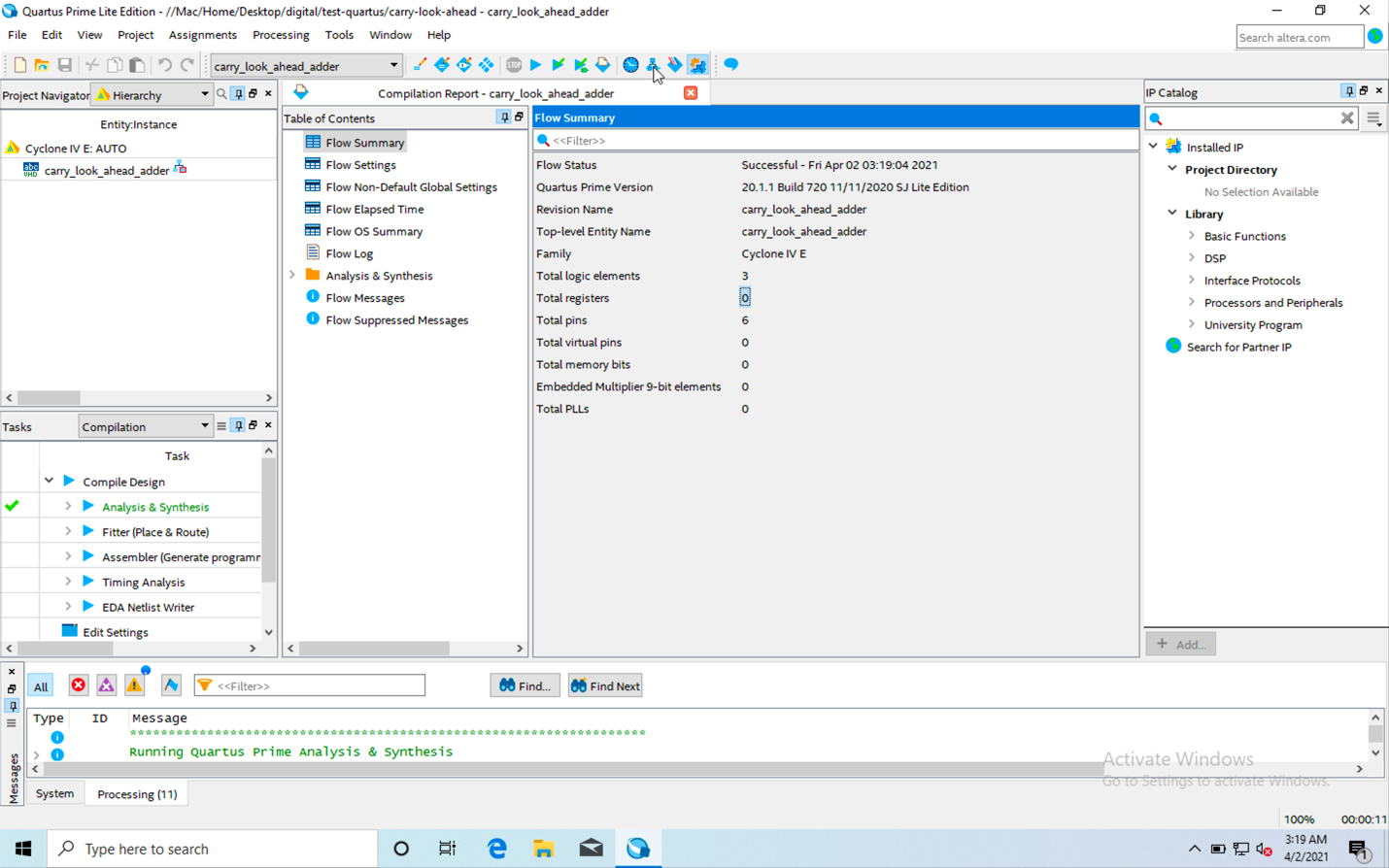
sum <= (input1 xor input2) xor carryIn;

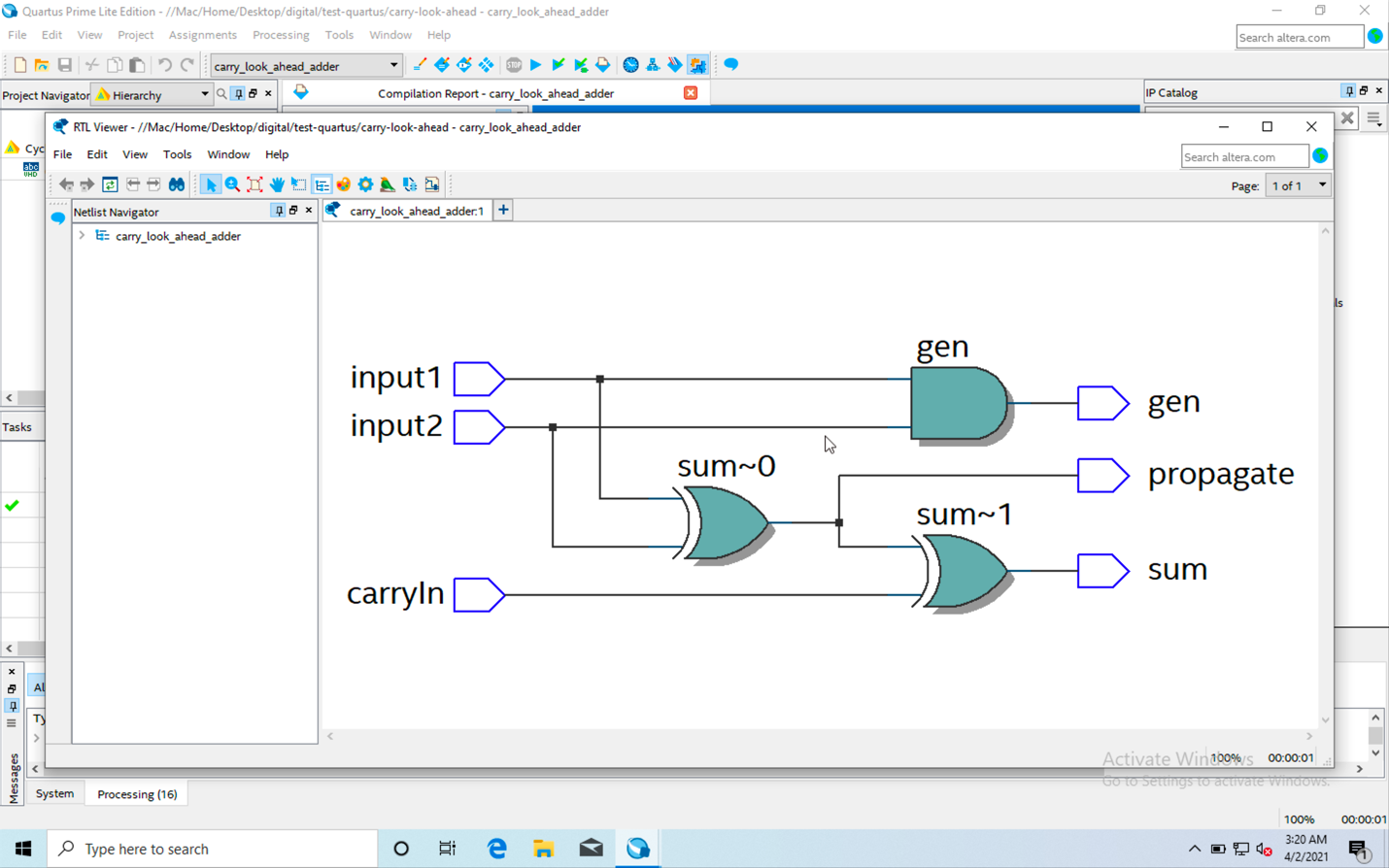
propagate <= input1 xor input2;

gen <= input1 and input2;

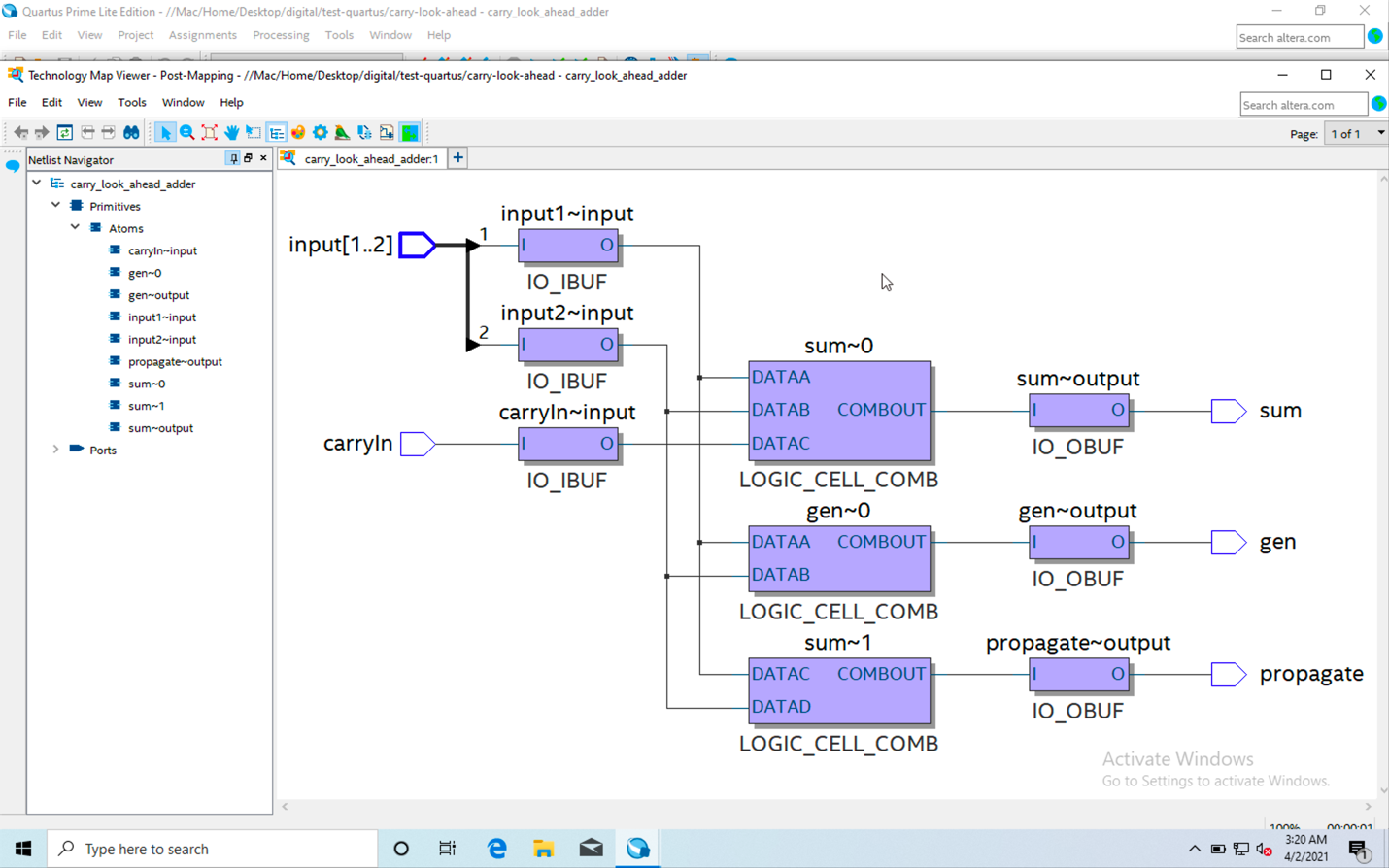
end architecture;

**compilation report**

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**RTL**

**Post-mapping**

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