

Hardware Specification

Product Name: RK3328 Core Board

Product Model: DSOM-010R

Revision History

Specification		Sect.	Update Description	By
Rev.	Date			
1.0	2023-01-17		New version release	Fu huayuan
1.1	2023-04-17		Update Footer and Header	Hubert

Approvals

Organization	Name	Title	Date

Contents

1. Product Description	3
1.1. Product Overview and Scope.....	3
1.2. Features	3
1.3. Application.....	4
2. System Block Diagram.....	5
2.1. Main Chip Block Diagram.....	5
2.2. Core Board Block Diagram.....	5
3. Basic Parameters and Interfaces	6
4. Pin Definition	7
5. Electrical Parameters.....	13
5.1. Absolute Electrical Parameters	13
5.2. Normal working parameters	14
6. Hardware Design Guidelines	14
6.1. SDIO/SDMMC.....	14
6.2. Wi-Fi/BT	17
6.3. Ethernet.....	18
6.4. USB	25
6.5. Audio	28
6.6. Recovery	32
6.7. Debug Circuit.....	33
7. Product Dimensions.....	34
8. The Methods of Coreboard Thermal Control.....	34
8.1. Thermal Control Strategy	34
8.2. Thermal Control Configure	35
9. Production Guide	36
9.1. SMT process	36
9.2. Module storage conditions:.....	36
9.3. Baking is required when:	36
9.4. ESD	37
9.5. Conformity.....	37
9.6. Recommended Furnace Temperature Profile	37
9.7. Storage.....	39
9.8. Order Information	39

1. Product Description

1.1. Product Overview and Scope

The RK3328 Core board uses the ROCKCHIP RK3328 Cortex-A53 quad-core processor and runs Android/Linux+QT/Ubuntu OS with a high-performance frequency of 1.5GHz. It features the Mali-450MP2 GPU, supporting 4K video encoding and H.264 hardware decoding. RK3328 core board has rich interfaces, with all function pins available for external device expansion, making it an ideal choice for human-computer interaction and industrial automation projects.

The RK3328 core board is a versatile Android-based intelligent Coreboard, widely used in products such as facial recognition devices, smart display terminals, video terminals, and industrial automation terminals, including advertising machines, digital signboards, smart self-service terminals, smart retail terminals, smart homes, O2O smart devices, industrial control hosts, and robot devices, among others.

The DSOM-010R Core Board offers a wide range of development documents and software resources that are both free and open-source. This convenience enables developers to enhance their efficiency and shorten the development cycle.

1.2. Features

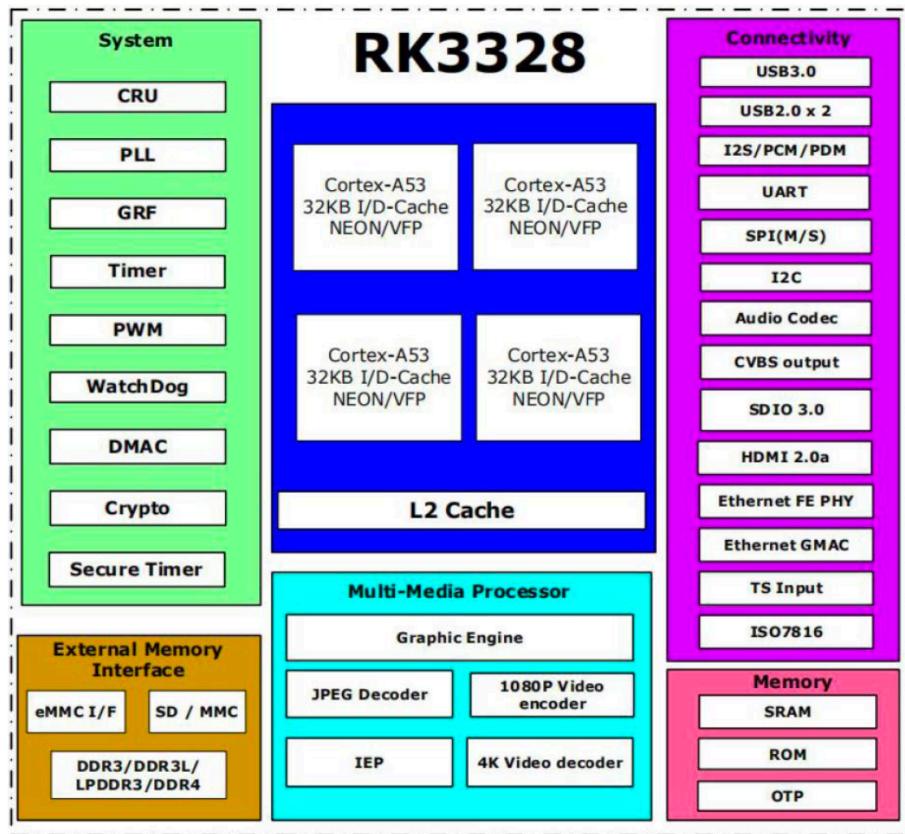
- Featuring a compact form factor and sufficient GPIO interfaces
- Size 44mm*44mm
- Utilizes RK805 PMU ensuring stable and reliable operation
- eMMC up to 32GB
- RAM up to 2GB
- Stamp hole soldering core board, with built-in CVBS and HDMI
- Supports customization of Android/Linux+QT system, providing system call interface API reference code and enabling perfect support for customer upper-level application APP development and SDK
- Supports 100M/1000M Ethernet;
- Leads out 132 PIN pins, including all CPU pins.
- Size 44mm*44mm
- RoHS certified

1.3. Application

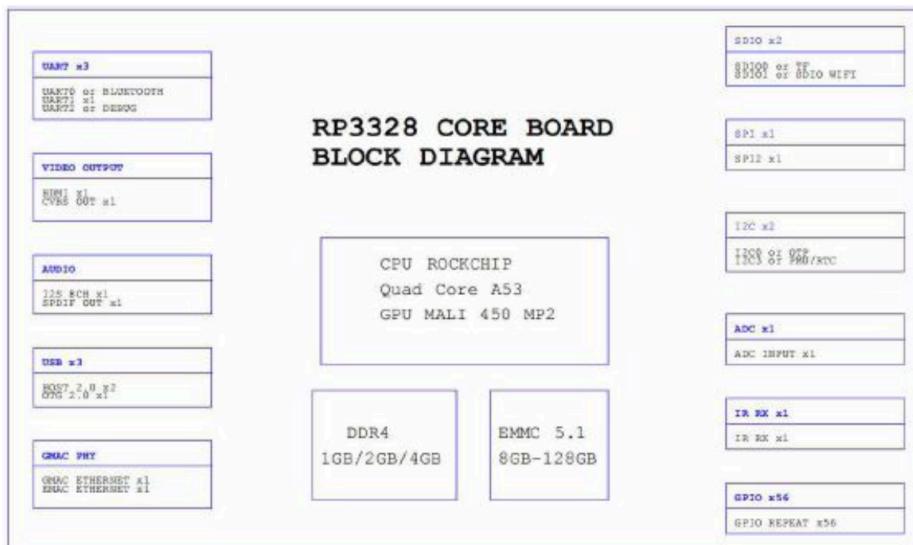
- IoT gateways
- Robotics
- Facial recognition devices
- Smart display terminals
- Video terminals

2. System Block Diagram

2.1. Main Chip Block Diagram



2.2. Core Board Block Diagram



3. Basic Parameters and Interfaces

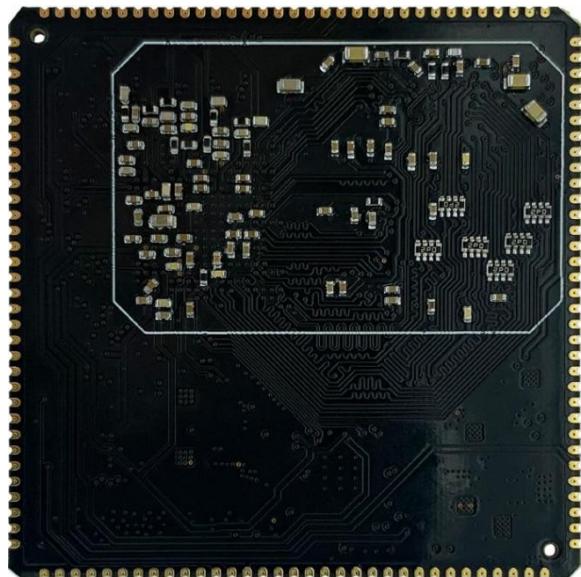
Item	Parameter
CPU	Quad-Core ARM® Cortex-A53 64-bit processor, Frequency up to 1.5GHz
GPU	ARM Mali-450 MP2 Quad-Core GPU Support OpenGL ES1.1/2.0, OpenVG1.1 Frequency up to 500 MHz
VPU	Support 4K VP9 and 4K 10bits H265 / H264 video decoding, up to 60fps 1080P multi-format video decoding(WMV, MPEG-1/2/4, VP9, H.264, H.265) 1080P video coding, support H.264/H.265 Video postprocessor: de-interlacing, denoising, edge/detail/color optimization
RAM	2GB (1GB optional)
Storage	eMMC 32 GB (8GB / 16GB / 32GB / 64G / 128G eMMC optional)
Power Management	RK805-1
Operating Voltage	Typical voltage 5V/2A
OS	andAndroDebian
Temperature	Operating Temperature: 0 °C ~80 °C Storage Temperature: -40 °C ~85 °C
Humidity	10~95%(Non-condensing)
Barometric Pressure	76Kpa ~106Kpa
Size	44mm×44mm x 3.5mm

Item	Parameter
Ethernet	Integrated GMAC Ethernet controller extended 2×RJ45 (1000Mbps)
HDMI	support maximum 4K/1080P display
CVBS	Support CVBS output
UART	3-way serial port, one of which is for debugging
I2C	2-way I2C
I2S	1 X I2S with 8 channel
SDIO	1 X SDIO for Wi-Fi AP6212
SPI	1 X SPI
USB 2.0	2 X USB2.0, one of which is for OTG
USB 3.0	1 X USB3.0
Ethernet	the main chip integrates 100M Ethernet chip
TF	1 X TF
GPIO	Defined features
ADC	1 X ADC
Upgrade	supports local firmware upgrades via USB interface

4. Pin Definition



Top Side Coreboard



Bottom Side Coreboard

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
1	USB30_TXP	O	O				USB30_TXP
2	USB30_TXN	O	O				USB30_TXN
3	USB30_RXP	I	I				USB30_RXP
4	USB30_RXN	I	I				USB30_RXN
5	USB30_DP	I/O	I				USB30_DP
6	USB30_DM	I/O	I				USB30_DM
7	GND	P			0		GND
8	AOL	O	O				AOL
9	AOR	O	O				AOR
10	GND	P			0		Ground
11	VDAC_OUT	O	O				VDAC_OUT
12	GND	P			0		GND
13	GPIO0_A2	I/O	I	down	4	3.3	GPIO0_A2/CLKOUT_GMAC_M0/SPDIF_TX_M2_d
14	MUTE_CTL	O	O			3.3	GPIO_MUTE_d
15	GPIO0_A0	I/O	I	down	4	3.3	GPIO0_A0/CLKOUT_WIFI_M0_d

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
16	SDMMC0_P_WREN	I/O	I	down	4	3.3	GPIO0_D6/FEPHY_LED_SPEED_10/SDMMC0_PWREN_M1
17	SPDIF_TX_M0	I/O	I	down	4	3.3	GPIO0_D3/SPDIF_TX_M0_d
18	HDMI_HPD	I/O	I	down	4	3.3	GPIO0_A4/HDMI_HPD_d
19	HDMI_SDA	I/O	I			3.3	I2C3_SDA/HDMI_SDA_od
20	HDMI_SCL	O	O			3.3	I2C3_SCL/HDMI_SCL_od
21	HDMI_CEC	I/O	I			3.3	HDMI_CEC
22	GND	P				0	GND
23	HDMI_TX_C-	O	O				HDMI_TX_C-
24	HDMI_TX_C+	O	O				HDMI_TX_C+
25	GND	P				0	GND
26	HDMI_TX_D0-	O	O				HDMI_TX_D0-
27	HDMI_TX_D1+	O	O				HDMI_TX_D0+
28	GND	P				0	GND
29	HDMI_TX_D1-	O	O				HDMI_TX_D1-
30	HDMI_TX_D2+	O	O				HDMI_TX_D1+
31	GND	P				0	GND
32	HDMI_TX_D2-	O	O				HDMI_TX_D2-
33	HDMI_TX_D2+	O	O				HDMI_TX_D2+
34	OTG20_DM	I/O	I				OTG20_DM
35	OTG20_DP	I/O	I				OTG20_DP
36	GND	P				0	GND
37	USB1_DM	I/O	I				USB1_DM
38	USB1_DP	I/O	I				USB1_DP
39	GND	P				0	GND
40	TD+	I/O	O				TD+
41	TD-	I/O	O				TD-

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
42	GND	P				0	GND
43	RD+	I/O	I				RD+
44	RD-	I/O	I				RD-
45	GND	P				0	GND
46	SDMMC0_D _{ET}	I/O	I	up	4	3.3	GPIO1_A5/SDMMC0_DETN_u
47	SDMMC0_D ₁	I/O	I	up	8	3.3	GPIO1_A1/SDMMC0_D1/UAR T2_RX_M0_u
48	SDMMC0_D ₀	I/O	I	up	8	3.3	GPIO1_A0/SDMMC0_D0/UAR T2_TX_M0_u
49	GND	P				0	GND
50	SDMMC0_C_LK	I/O	I	down	8	3.3	GPIO1_A6/SDMMC0_CLK/TEST_CLK0_d
51	GND	P				0	GND
52	SDMMC0_C_MD	O	I	up	8	3.3	GPIO1_A4/SDMMC0_CMD_u
53	SDMMC0_D ₃	I/O	I	up	8	3.3	GPIO1_A3/SDMMC0_D3/JTAG_TMS_u
54	SDMMC0_D ₂	I/O	I	up	8	3.3	GPIO1_A2/SDMMC0_D2/JTAG_TCK_u
55	UART0_RTS_N	I/O	I	down	4	1.8/3.3	GPIO1_B2/UART0_RTSN/GMAC_C_RXD1_M1_d
56	UART0_TX	I/O	I	up	4	1.8/3.3	GPIO1_B1/UART0_TX/GMAC_TXD0_M1_u
57	UART0_RX	I/O	I	up	4	1.8/3.3	GPIO1_B0/UART0_RX/GMAC_TXD1_M1_u
58	UART0_CTS_N	I/O	I	down	4	1.8/3.3	GPIO1_B3/UART0_CTSN/GMAC_C_RXD0_M1_d
59	GND	P				0	GND
60	PCM_SYNC	I/O	I	down	4	1.8/3.3	GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDIO_M1_d
61	PCM_TX	I/O	I	down	4	1.8/3.3	GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDII_M1_d
62	PCM_CLK	I/O	I	down	2	1.8/3.3	GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
							1_u
63	PCM_RX	I/O	I	down	2	1.8/3.3	GPIO1_D0/I2S2_SDI_M0/GM AC_RXER_M1/PDM_SDI1_M1_d
64	GND	P				0	GND
65	32K_OUT	O	I	up	2	1.8/3.3	GPIO1_D4/CLK32KOUT_M1_d
66	GND	P				0	GND
67	SDMMC1_D1	I/O	I	down	4	1.8/3.3	GPIO1_B7/SDMMC1_D1/GMA_C_RXD2_M1_u
68	SDMMC1_D0	I/O	I	down	4	1.8/3.3	GPIO1_B6/SDMMC1_D0/GMA_C_RXD3_M1_u
69	GND	P				0	GND
70	SDMMC1_CLK	I/O	I	down	4	1.8/3.3	GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1_d
71	GND	P				0	GND
72	SDMMC1_CMD	I/O	I	up	8	1.8/3.3	GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1_u
73	SDMMC1_D3	I/O	I	up	8	1.8/3.3	GPIO1_C1/SDMMC1_D3/GMA_C_TXD2_M1_u
74	SDMMC1_D2	I/O	I	up	8	1.8/3.3	GPIO1_C0/SDMMC1_D2/GMA_C_TXD3_M1_u
75	GND	P				0	GND
76	WIFI_WAKE_HOST	I/O	I	up	4	1.8/3.3	GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1_u
77	WIFI_REG_ON	I/O	I	down	4	1.8/3.3	GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1_d
78	BT_WAKE_HOST	I/O	I	down	4	1.8/3.3	GPIO1_D2/I2S2_LRCK_RX_M0/CLKOUT_GMAC_M2/PDM_SD13_M1_d
79	BT_REG_ON	I/O	I	down	4	1.8/3.3	GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1_d
80	GND	P				0	GND
81	EMMC_KEY	I	I			3.3	UPDATE KEY
82	GND	P				0	GND
83	SARADC_IN1	I	I			1.8	SARADC_IN1

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
84	RECOVER	I	I			1.8	SARADC_IN0
85	GND	P				0	GND
86	RESET	I	I			3.3	RESET
87	GND	P				0	GND
88	UART2_TX	I/O	I	down	4	3.3	GPIO2_A0/UART2_TX_M1/PO WERSTATE0_d
89	UART2_RX	I/O	I	up	4	3.3	GPIO2_A1/UART2_RX_M1/PO WERSTATE1_u
90	IR_RX	I/O	I	up	4	3.3	GPIO2_A2/IR_RX/POWERSTA TE2_u
91	GND	P				0	GND
92	I2C1_SCL_P MIC	I/O	I	up	4	3.3	GPIO2_A5/PWM1/I2C1_SCL_u
93	I2C1_SDA_P MIC	I/O	I	up	4	3.3	GPIO2_A4/PWM0/I2C1_SDA_u
94	PMIC_SLEEP	I	I	down	4	3.3	GPIO2_D2/USB20_DRV_d
95	GPIO2_A3	I/O				3.3	GPIO2_A3/EFUSE_PWREN/P OWERSTATE3_u
96	PWR_KEY	I	I	down		3.3	PWR_KEY
97	RK805_32K OUT	O	OD			3.3	RK805_32KOUT
98	GND	P				0	GND
99	GND	P				0	GND
100	VCC_SYS	P	I			5.0	Power supply 5V
101	VCC_SYS	P	I			5.0	Power supply 5V
102	PMU_EN	I	I	down		3.3	The power-on self-startup setting switch: 0 = Power off on startup, 1 = Power on on startup
103	GND	P				0	GND
104	GND	P				0	GND
105	VCCIO_WL	I	I			1.8/3.3	IO Voltage Input 1.8V/3.3V
106	GND	P				0	GND
107	VCC_18	P	O			1.8	POWER OUT 1V8 100mA
108	GND	P				0	GND
109	VCC_IO	O				3.3	POWER OUT 3V3 300mA

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
110	GND	P				0	GND
111	I2S1_SDI	I/O	I	up	4	3.3	GPIO2_C3/I2S1_SDI/PDM_SDI0_M0/CARD_CLK_M1_u
112	I2S1_SDIO3	I/O	I	up	4	3.3	GPIO2_C6/I2S1_SDIO3/PDM_SDID3_M0/CARD_IO_M1_u
113	I2S1_SDIO2	I/O	I	up	4	3.3	GPIO2_C5/I2S1_SDIO2/PDM_SDID2_M0/CARD_DET_M1_u
114	I2S1_SDIO1	I/O	I	up	4	3.3	GPIO2_C4/I2S1_SDIO1/PDM_SDID1_M0/CARD_RST_M1_u
115	I2S1_SDO	I/O	I	up	4	3.3	GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0_u
116	I2S1_LRCK_RX	I/O	I	up	4	3.3	GPIO2_C0/I2S1_LRCK_RX/TSP_D5_M1/CIF_D5_M1_u
117	I2S1_LRCK_TX	I/O	I	up	4	3.3	GPIO2_C1/I2S1_LRCK_TX/SPDI_F_TX_M1/TSP_D6_M1/CIF_D6_M1_u
118	I2S1_SCLK	I/O	I	down	4	3.3	GPIO2_C2/I2S1_SCLK/PDMCLK_M0/TSP_D7_M1/CIF_D7_M1_d
119	I2S1_MCLK	I/O	I	down	4	3.3	GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1_d
120	GND	P				0	GND
121	I2C0_SCL	I/O	I	up	4	3.3	GPIO2_D0/I2C0_SCL/FEPHYLED_LINK_M1_u
122	I2C0_SDA	I/O	I	up	4	3.3	GPIO2_D1/I2C0_SDA/FEPHYLED_DATA_M1_u
123	GND	P				0	GND
124	UART1_TX	I/O	I	up	4	3.3	GPIO3_A4/TSP_D0/CIF_D0/SDMMC0EXT_D0/UART1_TX/USB3PHY_DEBUG4_u
125	USB20_HOST_DRV	I/O	I	up	4	3.3	GPIO3_A5/TSP_D1/CIF_D1/SDMMC0EXT_D1/UART1_RTSN/USB3PHY_DEBUG5_u
126	UART1_RX	I/O	I	up	4	3.3	GPIO3_A6/TSP_D2/CIF_D2/SDMMC0EXT_D2/UART1_RX/USB3PHY_DEBUG6_u

Pin	Name	I/O Type	I/O Def	I/O Voltage (High/Low)	I/O Driver (Unit: mA)	I/O Voltage (Unit: V)	Feature
127	USB30_HOST_DRV	I/O	I	up	4	3.3	GPIO3_A7/TSP_D3/CIF_D3/S DMMC0EXT_D3/UART1_CTS N/USB3PHY_DEBUG7_u
128	GND	P				0	GND
129	SPI2_CS0	I/O	I	down	4	3.3	GPIO3_B0/TSP_D4/CIF_D4/S PI_CSNO_M2/I2S2_LRCK_TX_ M1/USB3PHY_DEBUG8/I2S2_L RCK_RX_M1_d
130	SPI2_TXD	I/O	I	up	4	3.3	GPIO3_A1/TSP_FAIL/CIF_HR EF/SDMMC0EXT_DET/SPI_TX D_M2/USB3PHY_DEBUG2/I2S 2_SDO_M1_u
131	SPI2_RXD	I/O	I	down	4	3.3	GPIO3_A2/TSP_CLK/CIF_CLK IN/SDMMC0EXT_CLK/SPI_RX D_M2/USB3PHY_DEBUG3/I2S 2_SDI_M1_d
132	SPI2_CLK	I/O	I	up	4	3.3	GPIO3_A0/TSP_VALID/CIF_V SYNC/SDMMC0EXT_CMD/SP I_CLK_M2/USB3PHY_DEBUG1/ I2S2_SCLK_M1_u

NOTE:

I/O types: I = digital-input, O = digital-output, I/O = digital input/output (bidirectional),

A=Analog IO. Def default IO direction for digital IO.

All GPIO pins support interrupts. P = power supply.

5. Electrical Parameters

5.1. Absolute Electrical Parameters

Parameter	Description	Min	Typ	Max	Unit
VCC_SYS	Input Voltage	-0.3		6.5	V
Ta	Operating temperature range	0		80	°C
Ts	Store temperature range	-40		85	°C

Note: Exposure to conditions beyond the absolute maximum ratings may cause permanent damage and affect the reliability and safety of the device and its systems. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

5.2. Normal working parameters

Parameter	Description	Min	Typ	Max	Unit
VCC_SYS	Input Voltage	4.75	5	5.25	V
Ta	Operating temperature range	-20	25	60	°C
Ts	Store temperature range	-20	25	70	°C
Current (Without any other peripherals connected)	Startup current	370	576	1023	mA
	Static current		360		mA

6. Hardware Design Guidelines

6.1. SDIO/SDMMC

The RK3328 provides two SDMMC interface controllers supporting the SDMMC 3.0 protocol. However, the current core board is not designed for 1.8V/3.3V power switching, so it only supports the SDMMC 2.0 protocol.

- SDMMC0 is multiplexed with UART2 and JTAG functions.
- The SDMMC0EXT controller also supports the SDMMC 3.0 protocol, but due to power design limitations, it only supports SDIO 2.0. It can be used to connect to TF cards or SDIO WIFI.

The recommended pull-up/down and matching design for the SDMMC interface are as follows:

Signal	Internal pull/pull-upn	Connection method	Description
SDMMC_DQ[3:0]	Pull-up	Series with 22ohm resistor	SD data transmission/reception
SDMMC_CLK	Pull-down	Series with 22ohm resistor	SD clock transmission
SDMMC_CMD	Pull-up	Series with 22ohm resistor	SD command transmission/reception

In order to meet the requirements of ESD protection, it is necessary to consider designing protection circuits on the SDMMC circuit in circuit design. To avoid the impact of protection devices on SDMMC signals and achieve good protection effect, the following principles are recommended for PCB design:

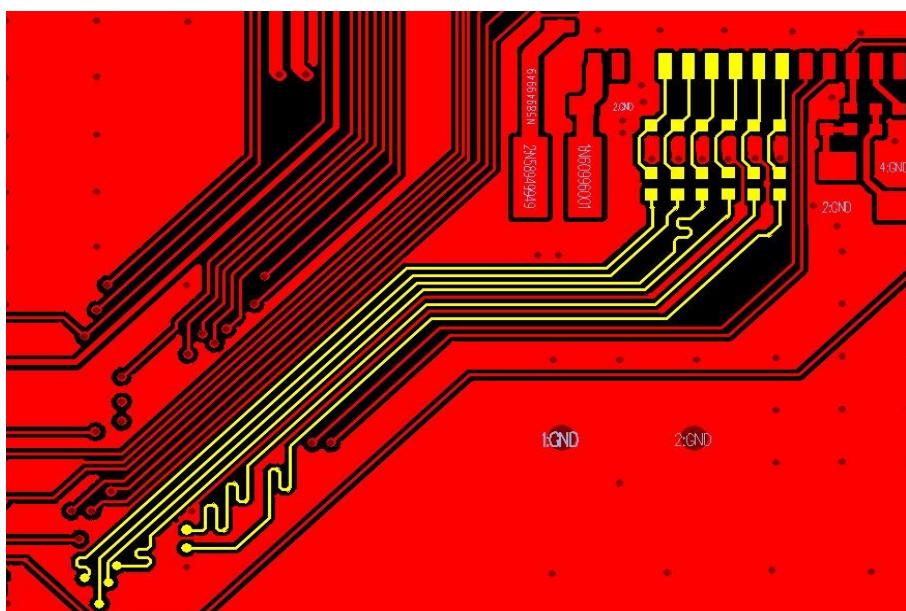
- The protection device is recommended to be placed close to the SDMMC connector port.
- It is recommended that the parasitic capacitance of the protection device be less than 10pF.

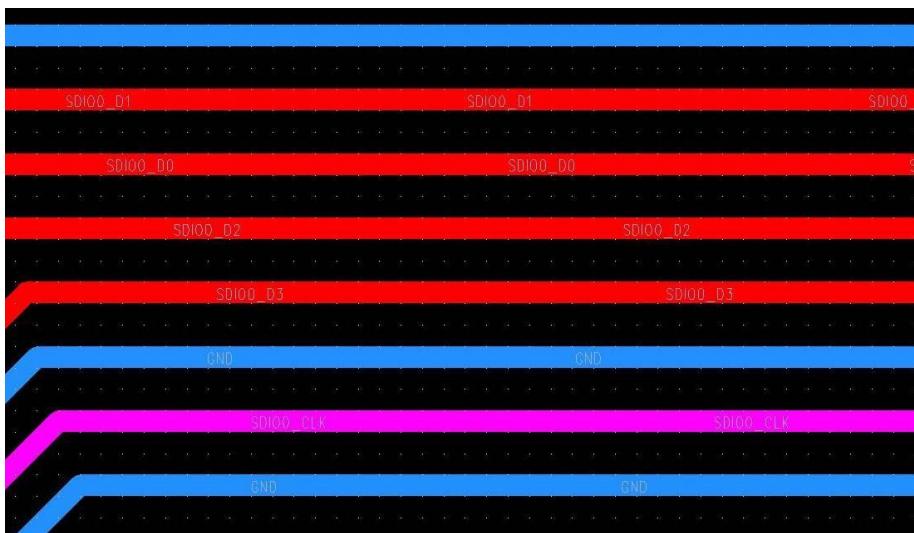
SDIO/SDMMC PCB design routing should pay attention to the following:

- CLK should be routed separately and have ground shielding
- DATA lines should follow the 3W rule for spacing
- TF card only supports up to SDMMC2.0 and has no separate power supply, while Wi-Fi supports up to SDIO3.0 and a clock frequency of up to 180MHz.

Therefore, SDIO_D0/1/2/3, SDIO_CLK, and SDIO_CMD should be routed carefully on the PCB layout to avoid interference and ensure consistency.

The highlighted yellow part in the diagram below is the SDIO routing, and the PCB routing should maintain the integrity of the reference layer (adjacent layers should maintain the same plane) to avoid interference from other signals, such as power lines on the same layer should be isolated with GND.





- Due to the long length of the tracks, the spacing between them is recommended to be 8mil.
- The load capacitance consists of two parts: the SD card load's capacitance and the PCB load's capacitance. The load capacitance for the SD card should be less than 10pF according to the protocol requirements.

Parameters	Requirement
3.0V Operation	50 MHz with 40 pF
1.8V Operation	208 MHz with 21 pF

SDMMC Capacitance requirements

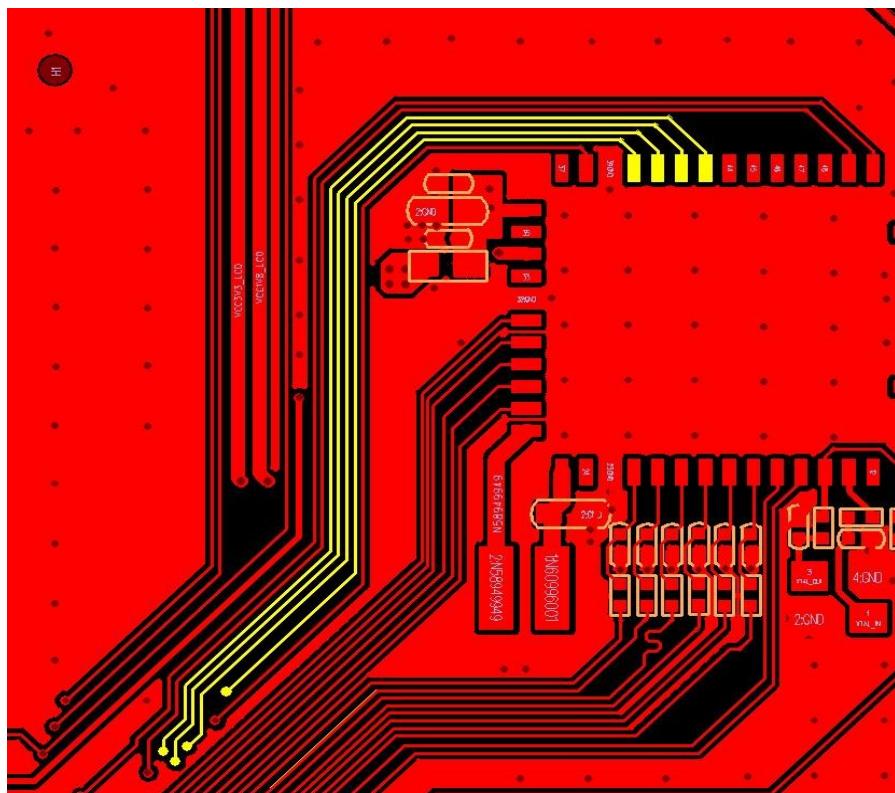
Capacitance	Min	Max	Units	Notes
$C_{CARD} (C_{DIE} + C_{PKG})$	5	10	pF	---

Card Capacitance Range

The requirements for routing of SDIO/SDMMC are shown in the following table:

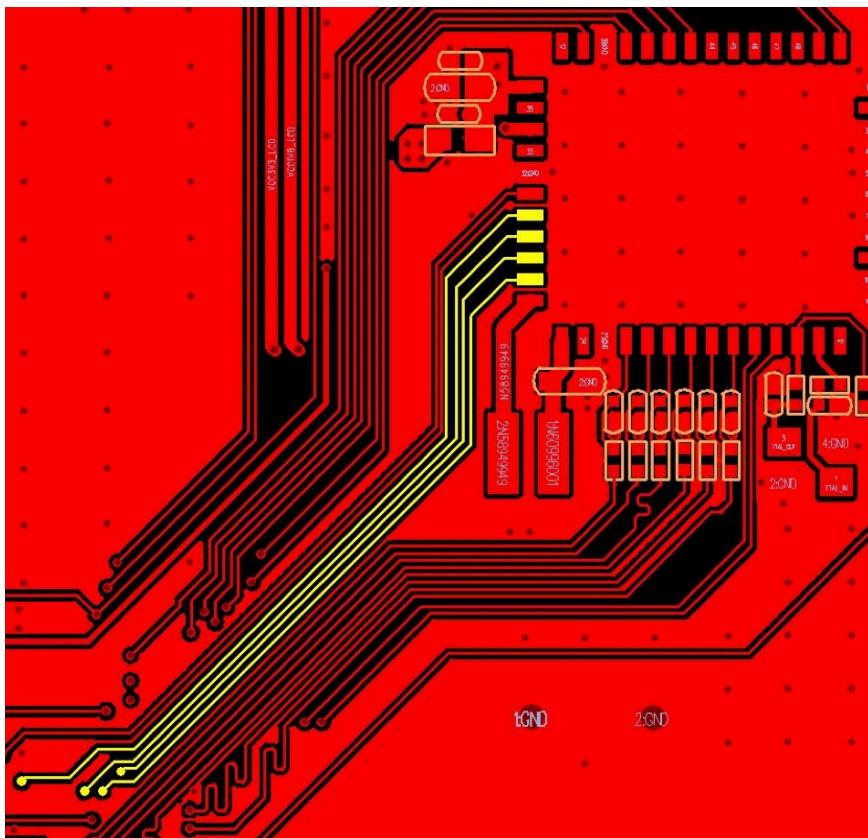
Parameters	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Max skew between data signal and clock	<20ps
Max trace length	<3.93 英寸

6.2. Wi-Fi/BT



WIFI communicates with the RK3328 chip through either SDIO or USB, while BT communicates with the RK3328 chip through UART or PCM interface. For SDIO PCB design, please refer to the design considerations for SDIO in section 3.3.1. BT communicates with the RK3328 chip through UART (up to 4Mbps), and the PCB layout for UART should also maintain the integrity of the reference layer as much as possible.

For the PCB layout of I2S/PCM, the adjacent reference layers should be kept intact (the adjacent layers should be in the same plane) to avoid interference from other signals, such as power, and the lines should be isolated from GND on the same layer.



6.3. Ethernet

The RK3328 integrates a Gigabit Ethernet MAC and a 100Mbps Ethernet PHY internally and can be used with an external Gigabit Ethernet PHY to achieve Gigabit network functionality. It can also use the integrated 100Mbps Ethernet PHY to achieve 100Mbps network functionality. Simultaneously using both can achieve dual-port (Gigabit + 100Mbps) functionality. For specific design information regarding Gigabit Ethernet, please refer to the design documentation provided by the PHY manufacturer. The working clock for the PHY can be selected from an external crystal or provided by the MAC_CLK output of the RK3328 chip.

1000M MAC

The RK3328 supports 10/100/1000M MAC. The design and precautions for the 1000M GMAC are described below.

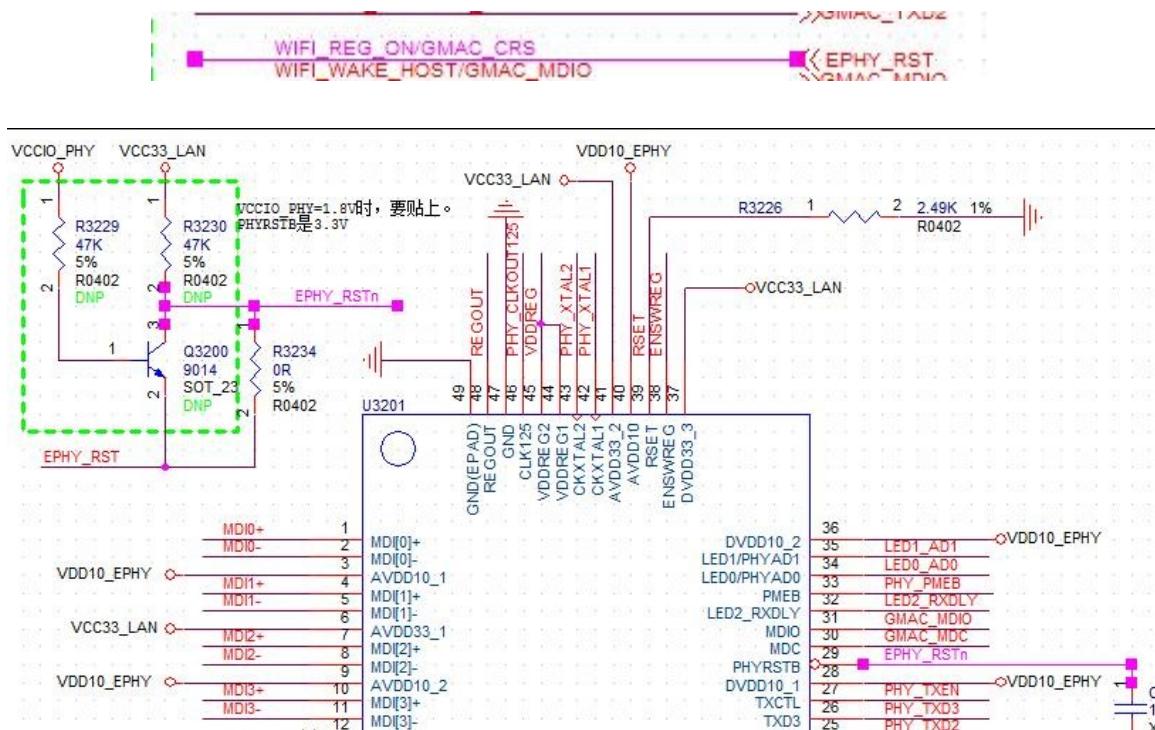
Signal	Internal Pull-up/Down	Connection method	Description
MAC_TXCLK	Pull-down	Series 22 ohm resistor	Reference clock for data transmission
MAC_RXCLK	Pull-down	Series 22 ohm resistor	Reference clock for data reception
MAC_TXD[3:0]	Pull-down	Series 22 ohm resistor	Data transmission
MAC_RXD[3:0]	Pull-down	Series 22 ohm resistor	Data reception
MAC_TXEN	Pull-down	Series 22 ohm resistor	Enable data transmission
MAC_RXDV	Pull-down	Direct connection	Data reception valid indicator
MAC_MDC	Pull-down	Direct connection	Configure interface clock
MAC_MDIO	Pull-down	Direct connection	Configure interface I/O
MAC_CLK	Pull-down	Series 22 ohm resistor	MAC master clock output

Power supply: The RK3328 GMAC IO voltage is 3.3V/1.8V (selected via Pin 105 on the core board), and the Ethernet PHY IO voltage needs to be consistent with the GMAC IO level.

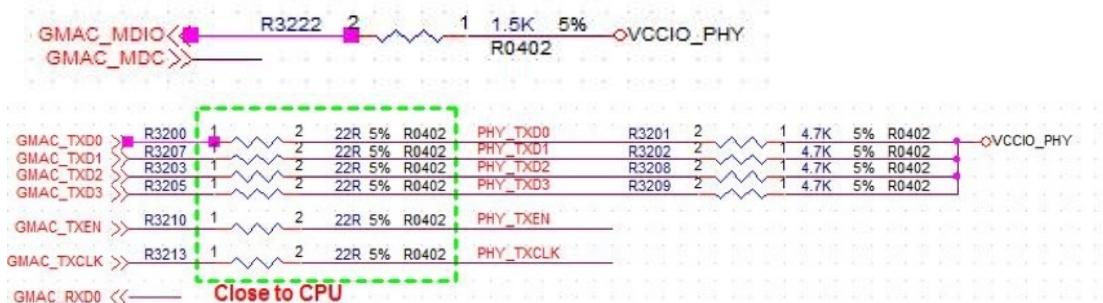
On the **RGMII** interface transmission and reception signal lines, TX_CLK and RX_CLK are 125MHz. In order to achieve a transmission rate of 1000Mb, the TXD and RXD signal lines are sampled on both edges of the clock, and the data enable signals (MAC_TXEN, MAC_RXDV) must be enabled before the data is sent.

Reset: The MAC controls the reset of the PHY through GPIO, but if the IO of the PHY is 1.8V, the following circuit needs to be added.

GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1_u	AA19 SDMMC1_D2/GMAC_TXD3
GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1_u	Y19 SDMMC1_D3/GMAC_TXD2
GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1_d	W20 WIFI_REG_ON/GMAC_CRS
GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1_u	Y21 WIFI_WAKE_HOST/GMAC_MDIO
GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1_d	W15 BT_REG_ON/GMAC_CLK
GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1_u	W16 GMAC_RXDV/PCM_CLK
GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDIO_M1_d	W17 GMAC_MDC/PCM_SYNC
	V12 BT_WAKE_HOST/CLKOUT_GMAC



The control and status information transfer between the MAC layer and PHY is carried out through the MDIO interface, using the clock signal MDC and the data signal MDIO. It is important to note that the MDIO signal requires a pull-up resistor, and the TX signal also requires an additional pull-up resistor, as shown in the diagram below:

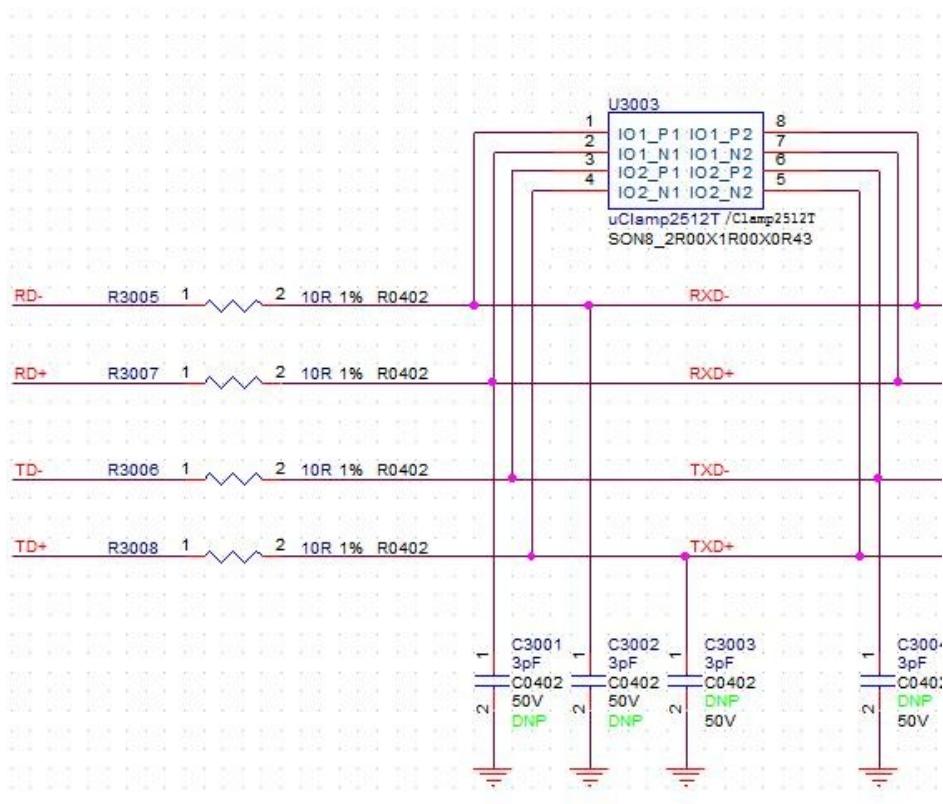


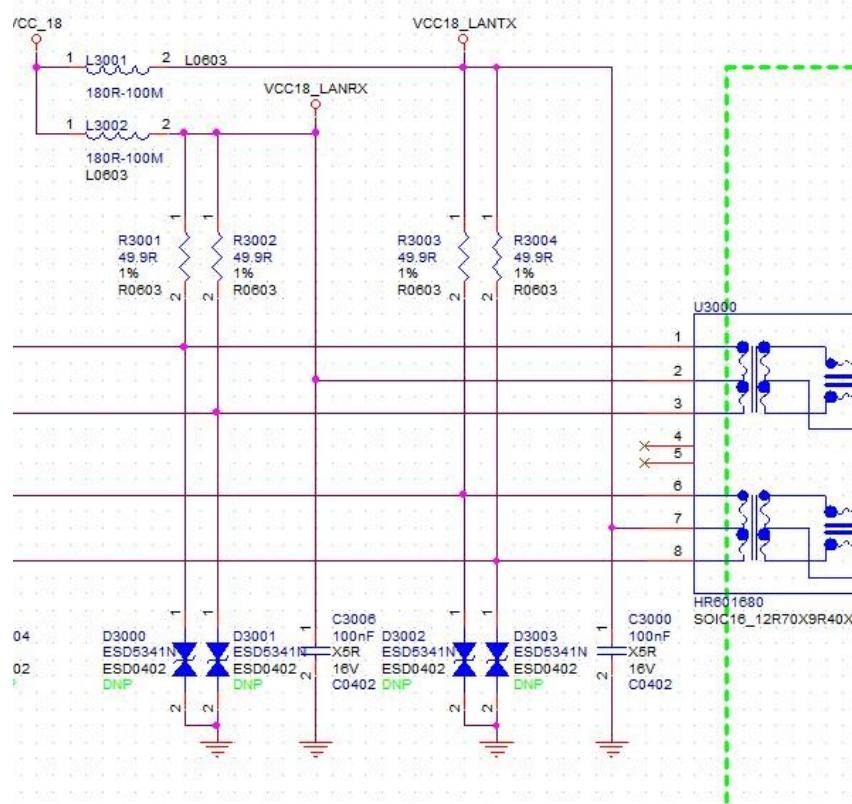
100M PHY

RK3328 supports built-in integration of 10/100 PHY. The PHY interface design of RK3328 includes the following:

Signal	Internal Pull-up/down	Connection method	Description
FEPHY_TXP	NA	Connect a 10 ohm resistor in series with a network transformer.	Differential signaling for data transmission
FEPHY_TXP	NA	Connect a 10 ohm resistor in series with a network transformer.	
FEPHY_TXP	NA	Connect a 10 ohm resistor in series with a network transformer.	Differential signaling for data reception
FEPHY_TXP	NA	Connect a 10 ohm resistor in series with a network transformer.	

When using internal 100Mbps, it is essential to note that the 10ohm resistor connected in series with the signal cannot be removed or its parameters changed. The pull-up resistor for the differential signal should be connected to the network transformer rather than the chip.

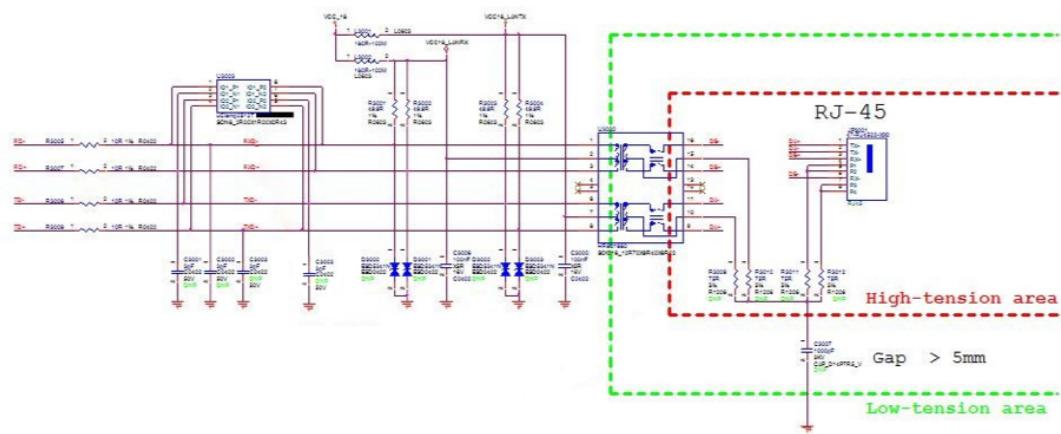




Surge and lightning protection

To meet the requirements of ESD protection and surge protection, it is necessary to add protection circuits in circuit design. In order to avoid the impact of protection devices on PHY wiring signals and achieve good protection effects, the following principles must be followed in PCB design:

It is recommended to place the protection device on the inside of the transformer, between the transformer and the PHY, close to the transformer. Differential mode and ESD can be solved by using components. TVS tubes with a breakdown voltage of 8kV and a response time of less than 1ns are recommended for protection devices



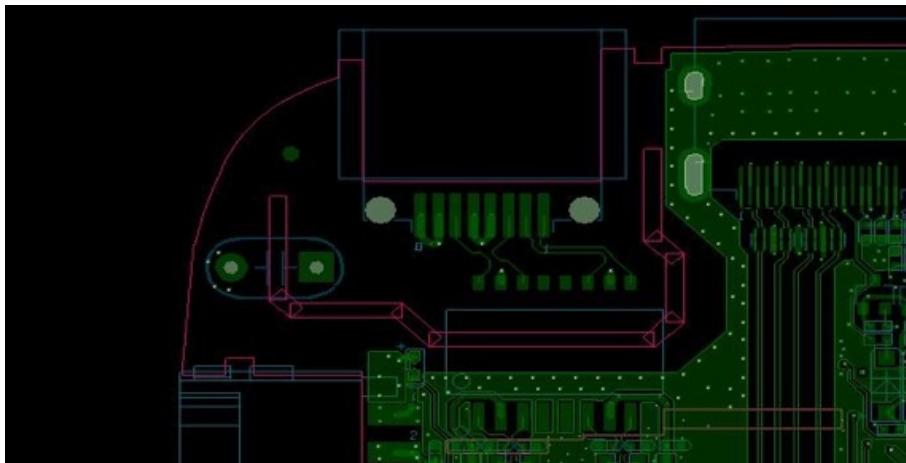
The cost of an integrated differential mode surge protection device may be higher compared to using individual ESD components. However, ESD components with specifications reaching the following levels can be selected instead.

PROTECTION PRODUCTS

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	100	Watts
Maximum Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	10	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 30 +/- 30	kV
Operating Temperature	T_j	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

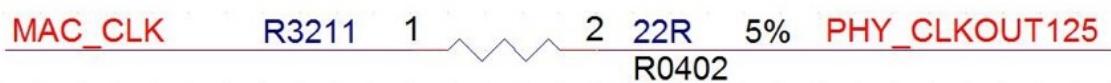
Common mode protection can be achieved through isolation spacing and AC isolation voltage provided by a network transformer. In order to meet the surge design requirements, the PCB design must ensure sufficient isolation spacing and include isolation slots. For example, if the common mode standard requires 4KV, the wires and components connected to the RJ45 connector must ensure an isolation spacing of 120 mils or more with respect to GND and the secondary of the transformer. The AC isolation voltage of the transformer itself must be in the range of 2.5-3KV or higher. If the common mode standard requires 6KV, the wires and components connected to the RJ45 connector must ensure an isolation spacing of 220 mils or more with respect to GND and the secondary of the transformer. The AC isolation voltage of the transformer itself must be in the range of 5KV or higher.



PCB Design Considerations:

- The closer the gigabit PHY is to RK3328, the better the effect will be. The RGMII routing should be kept below 15cm to achieve better EMI performance.
- MAC_RXCLK should be grounded.
- The series resistor of MAC_RX should be placed closer to the PHY.
- The routing of RXD[0:3], RXCLK, and RXDV should be equal in length, with a difference of less than 100mil throughout the entire length, and the routing should be as short as possible, with the entire length less than 15cm.
- There must be a complete reference plane, and other signal lines should not be routed parallel to it.
- The series-matching resistor of PHYTX should be placed close to RK3328, and PHY_TXCLK should be grounded.
- The routing of TXD[0:3], TXCLK, and TXEN should be equal in length, with a difference of less than 100mil throughout the entire length, and the routing should be as short as possible, with the entire length less than 15cm.

There must be a complete reference plane, and other signal lines should not be routed parallel to it. **R3211 in the figure below** should be placed closer to the PHY, grounded, and the routing should be as short as possible with a complete reference plane



6.4. USB

The RK3328 has 2 USB 2.0 interfaces and 1 USB 3.0 interface. The recommended pull-up/pull-down and matching designs for the USB 2.0 interfaces are shown in the table below.

Signal	Connection method	Description
USB0_DP/DM	Series 2.2 ohm resistor	USB2.0 HOST0&OTG Input/Output
USB1_DP/DM	Series 2.2 ohm resistor	USB2.0 HOST1 Input/Output

The recommended pull-up/pull-down and matching designs for the USB 3.0 interfaces are shown in the table below.

Signal	Connection method	Description
USB30_TXP/TXN	Series 0 ohm resistor	USB 3.0 Output
USB30_RXP/RXN	Series 0 ohm resistor	USB 3.0 Input
USB30_DP/DM	Series 2.2 ohm resistor	Compatible with USB 2.0, USB 2.0 HOST input/output

Please NOTE the following during use:

USB0 serves as the system firmware burning port and cannot be adjusted arbitrarily; OTG and HOST ports can be used independently.

VBUS serves as the USB OTG insertion detection, and the input detection voltage must be less than 3.3V, and there must be a high level for the computer to recognize it, so it cannot be left unconnected.

The USB controller reference resistor should be selected with 1% accuracy, as this resistor affects the USB amplitude and eye diagram quality.

To suppress electromagnetic radiation, consider reserving a common-mode inductor (common-mode choke) on the signal line. During debugging, choose to use a resistor or a common-mode inductor based on actual conditions.

ESD:

To meet ESD protection level requirements, protection circuits need to be designed in the USB circuit during circuit design. To avoid the impact of protection devices on USB wiring signals and achieve good protection effects, it is recommended to follow these principles during PCB design:

ESD protection devices should be placed close to the USB connector port.

ESD protection devices should be selected with an air discharge of 15kV, a contact discharge of 8kV, and a response time of less than 1ns.

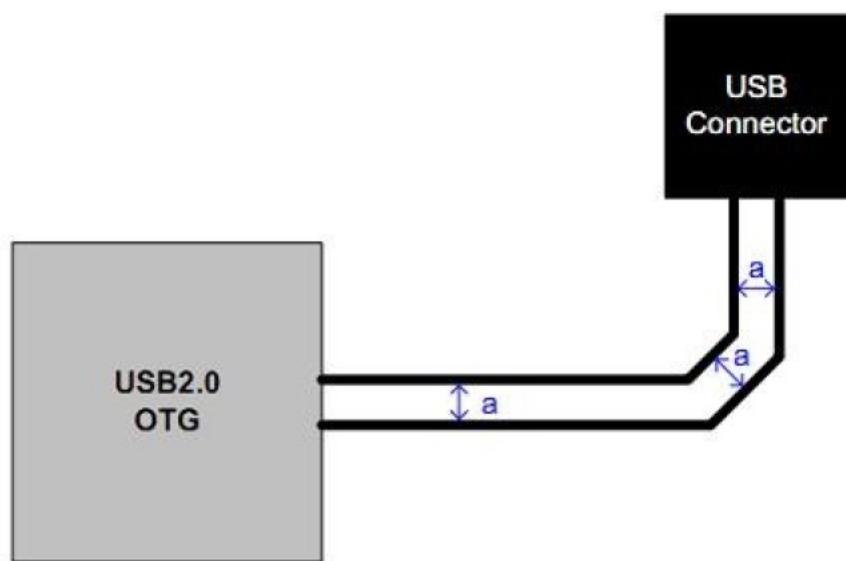
USB 2.0 has a transmission speed of 480Mbps, so differential signals are very sensitive to parasitic capacitance on the line. Therefore, ESD protection devices with low parasitic capacitance should be selected, and the capacitance should be less than 1pF.

USB 3.0 has a transmission speed of 5Gbps, so differential signals are very sensitive to parasitic capacitance on the line. Therefore, ESD protection devices with low parasitic capacitance should be selected, and the capacitance should be less than 0.4pF.

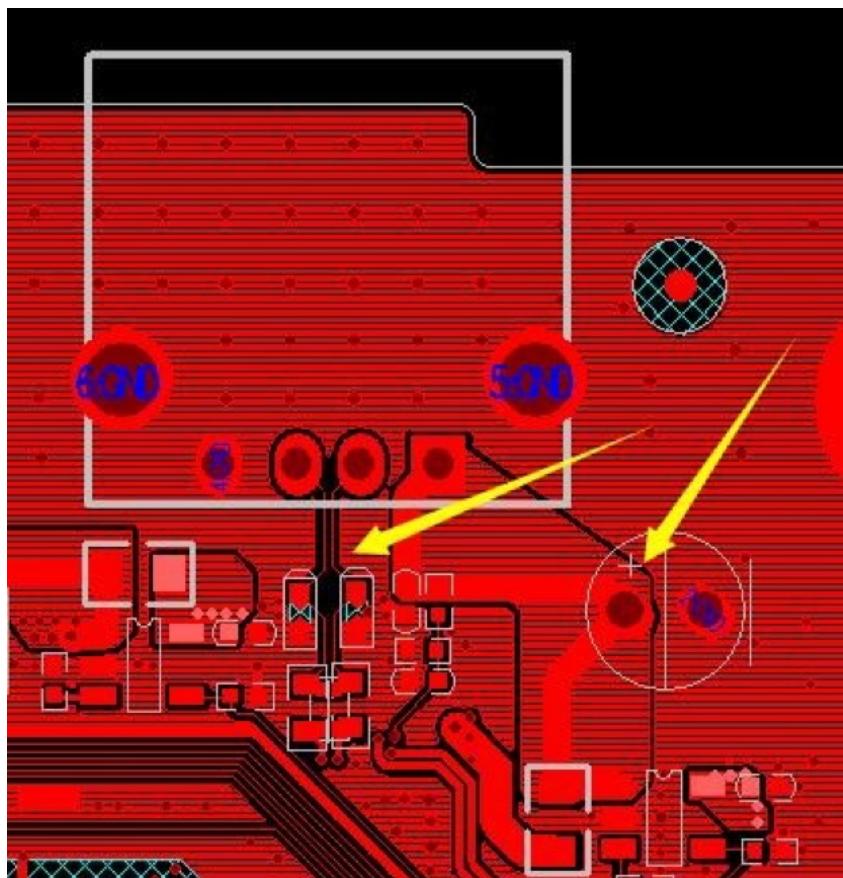
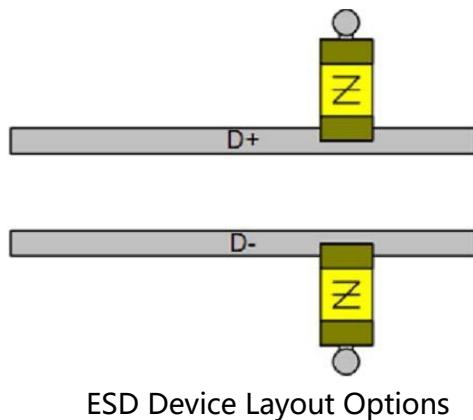
The 2.2ohm resistor in series with the USB signal cannot have its parameters modified or omitted.

USB PCB layout considerations are as follows:

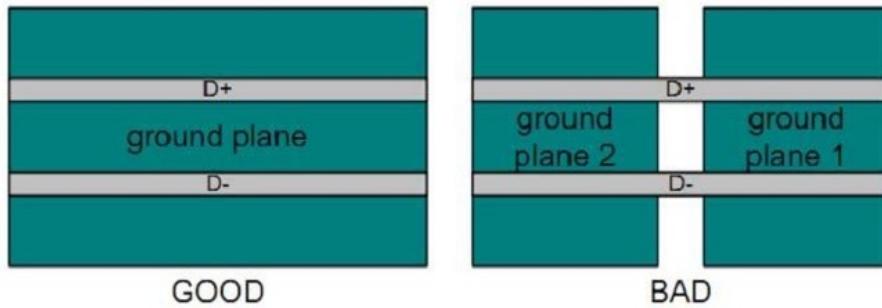
USB differential signals must be strictly routed according to differential requirements, corners cannot be right angles or sharp angles, and impedance requirements must be $Z = 90 \pm 10\text{ohm}$



The current defined by the USB 2.0 specification is 500mA, but the VBUS trace should preferably be able to withstand a current of 1A to prevent overcurrent and reduce line loss caused by PCB layout. The USB 3.0 specification defines a current of 900mA, but the VBUS trace should preferably be able to withstand a current of 1.5A to prevent overcurrent and reduce line loss caused by PCB layout. ESD protection devices, standard mode chokes, and large capacitors should be placed as close as possible to the USB interface, current limiting switch input, and output pins. Using multiple holes to reduce trace impedance and meet overload capacity is recommended if there are holes for changing layers. Also, ensure that the ground pins of the current limiting switch have a good grounding, and place at least four 0402-type through-holes on nearby pins, as shown in the figure below:



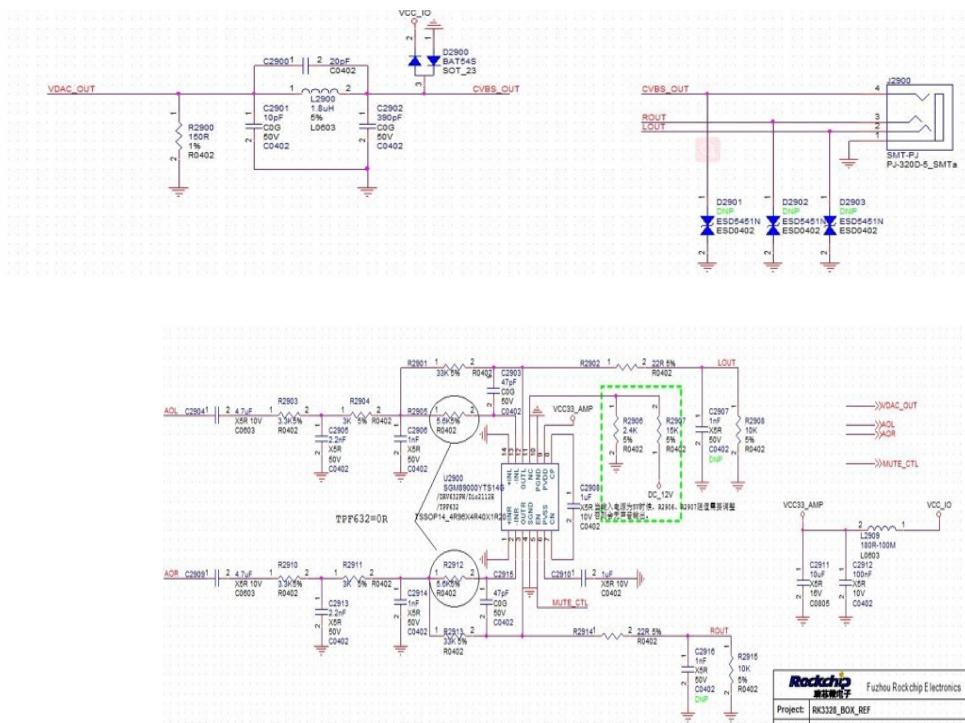
In DM/DP routing, it is advisable to minimize the use of vias, as vias can cause impedance discontinuity in the signal path. If vias must be used for layer changes, add a ground via at the center of the differential pair to provide a short signal return path. For USB routing, it is recommended to use surface routing and ensure that the routing reference plane is a continuous and uninterrupted plane, as shown in the diagram below:



6.5. Audio

Simulating Audio/Video Circuit

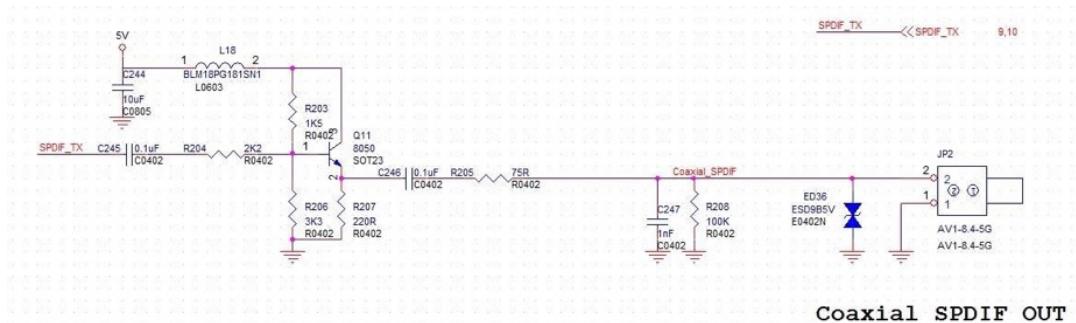
To meet standard requirements for audio, an audio amplifier IC needs to be added. The VDAC_OUT network has a lower resistance of 150 ohms, which cannot be changed, as shown in the diagram below:



PCB Layout Suggestions:

For CVBS video signals, a 75-ohm impedance control should be implemented, and PCB wiring should be kept as short as possible while avoiding interference signals such as PWM and DC-DC power inductors, especially the 12V to 5V DC-DC inductor, with a distance of at least 5mm. Additionally, the system power supply should not be used as a reference layer; the GND layer should be used instead. The ground-to-ground spacing within the same layer should be at least 2W to avoid affecting chroma and luminance gain unevenly.

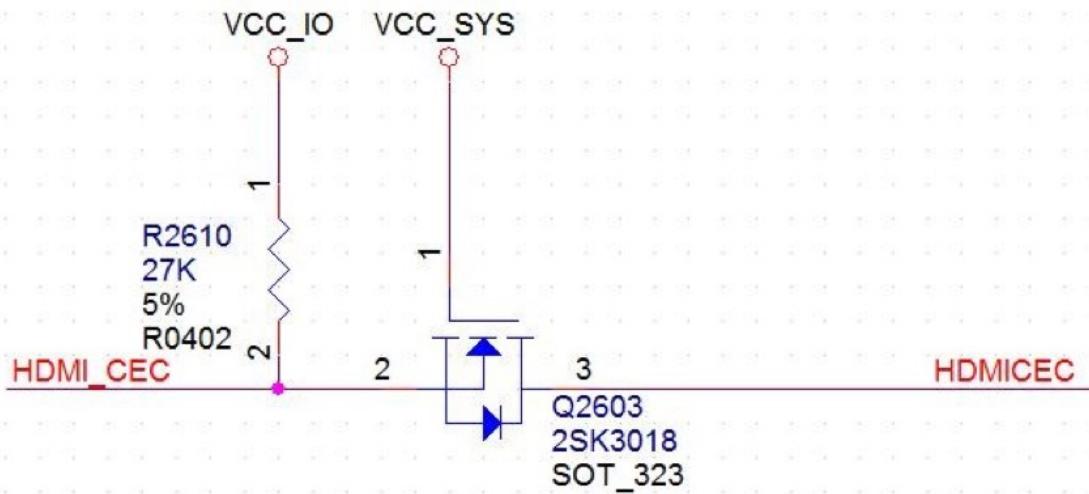
For analog audio signals, the left and right channels should be grounded appropriately, and ground vias should be placed strategically to avoid strong interference from power supplies, clocks, and other signals. It is essential to avoid interference sources for digital audio signals such as SPDIF. If using coaxial cables, isolation circuits should be added to prevent equipment levels from mismatching and damaging the SPDIF IO output port. The coaxial circuit is shown in the figure below.



HDMI OUT

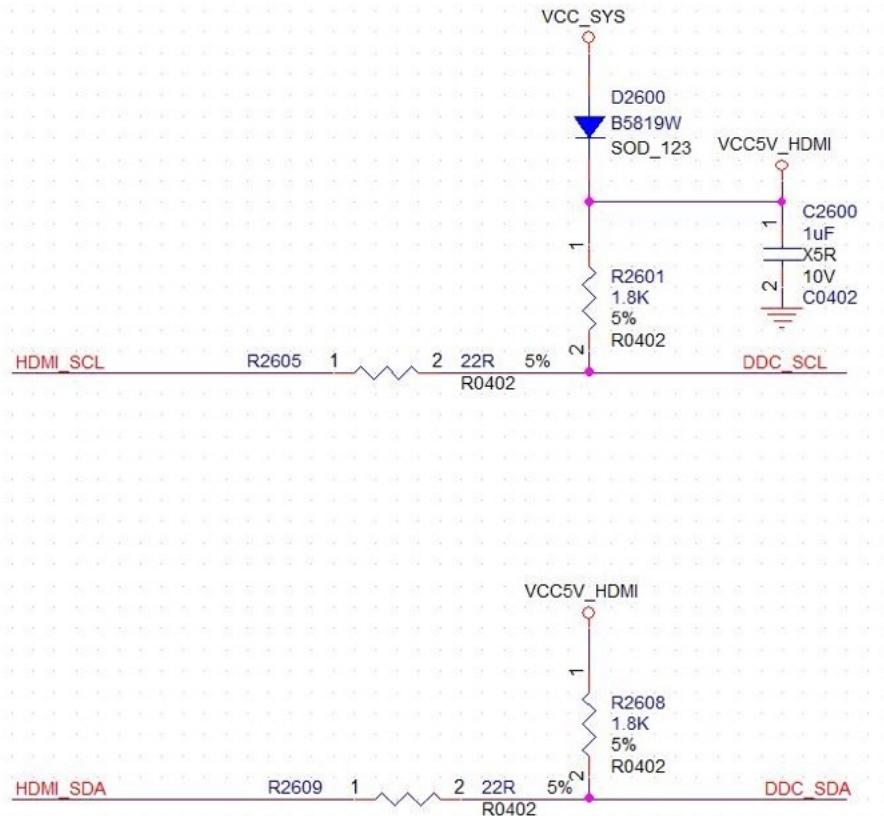
The RK3328 provides an HDMI interface that supports the HDMI 2.0a protocol.

When designing the HDMI interface circuit, it is essential to prevent reverse current flow. Refer to the diagram below for the design:

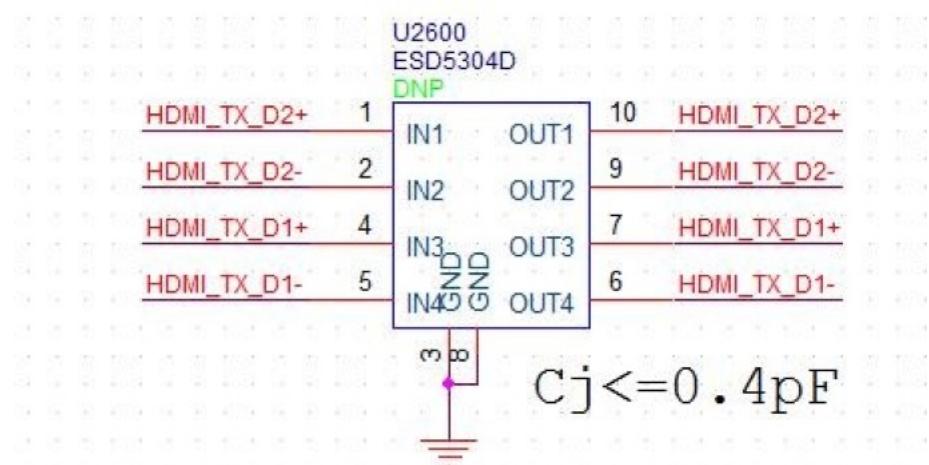


I2C Bus Circuit for RK3328

Refer to the diagram below for the design of the I2C bus circuit for the RK3328:

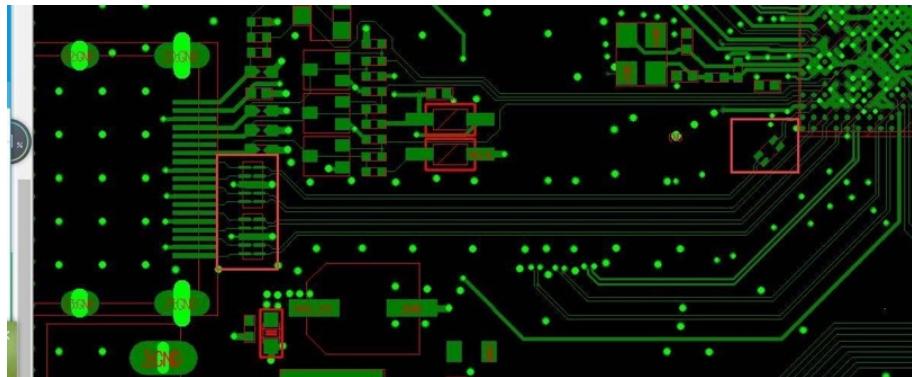


ESD protection is required for the four differential signals in HDMI. The ESD protection devices should be placed near the HDMI interface, and the recommended maximum capacitance is 0.4pF. Refer to the diagram below for the design:



PCB Layout Suggestions:

ESD protection devices should be placed near the HDMI socket. The standard mode of TMDS_CLK should be placed near the chip end to improve signal reflection and prevent excessive eye diagram jitter. Refer to the diagram below:



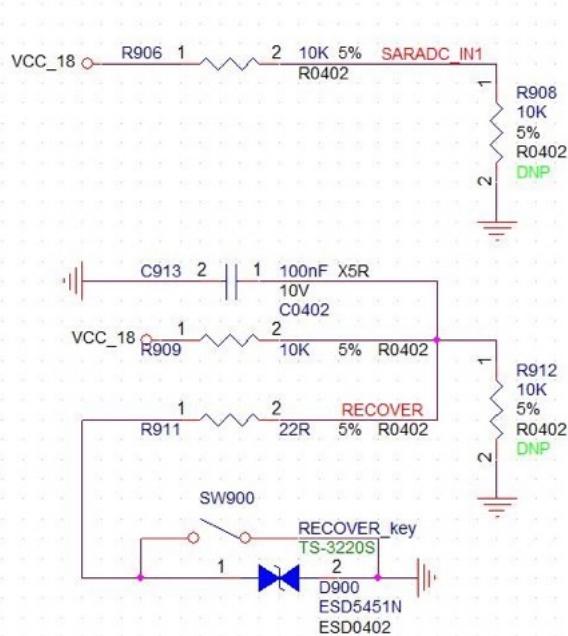
- The differential signals of HDMI must strictly follow the differential requirements for wiring, and the number of layer changes should be minimized to maintain the integrity of the reference plane. The impedance requirement is $Z=100\pm10\text{ohm}$.
- The HDMI signal of RK3328 can be directly fanned out to the HDMI connector in sequence. The number of via changes should be minimized to avoid the discontinuity of the line impedance. If layer changes cannot be avoided due to mold structure, it is recommended to control the impedance change of the layer change within 10% and arrange a nearby GND near signal return at each differential pair adjacent to the layer change.

The requirements for HDMI wiring are shown in the table below:

Parameter	Requirement
Trace Impedance	Differential impedance: $100\Omega \pm 10\%$
Max intra-pair skew	<4ps
Max trace length skew between clock and data pairs	<80ps
Max trace length on carrier board	9.8inches
Minimumpair-to-pairpaircing	3 times the width of the trace. Try to increase/ Spacing between pairs whenever it is possible.
The minimum spacing between HDMI and other Signals	At least 3 times the width of HDMI trace
Maximum allowed via	4

6.6. Recovery

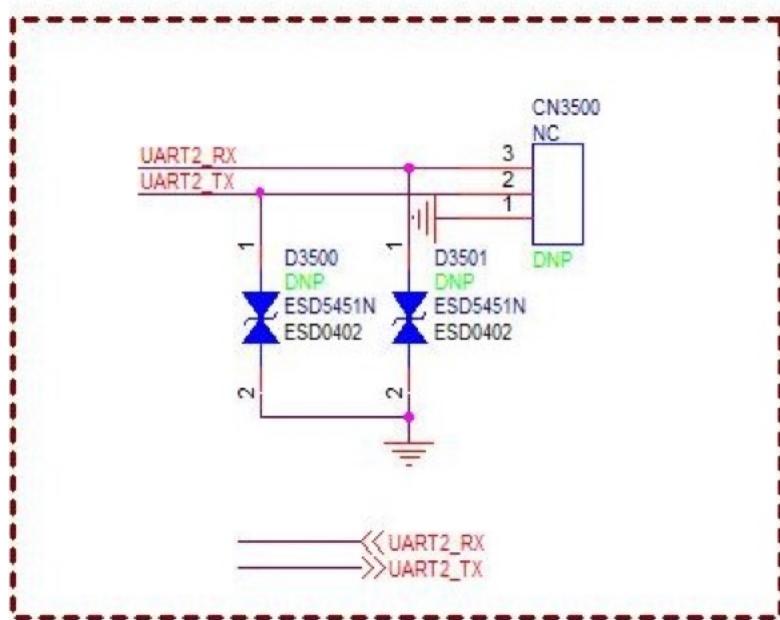
RK3328 uses SARADC_IN0 as the condition for entering RECOVER mode (without updating LOADER), as shown in the following figure. With firmware present, when SW900 is pressed at power on, SARADC_IN0 is kept at 0V, and RK3328 enters Rockusb programming mode. When the PC recognizes the USB device, release the button to restore ADC_IN0 to a high level (3.3V) and proceed with firmware programming.



6.7. Debug Circuit

For the convenience of online software debugging, RK3328 has a dedicated UART interface (UART2) for debugging purposes. In actual product applications, it is not recommended to use this interface for other functions. The interface should be designed as shown in Figure 3-46 to reserve a debugging interface for easy product debugging.

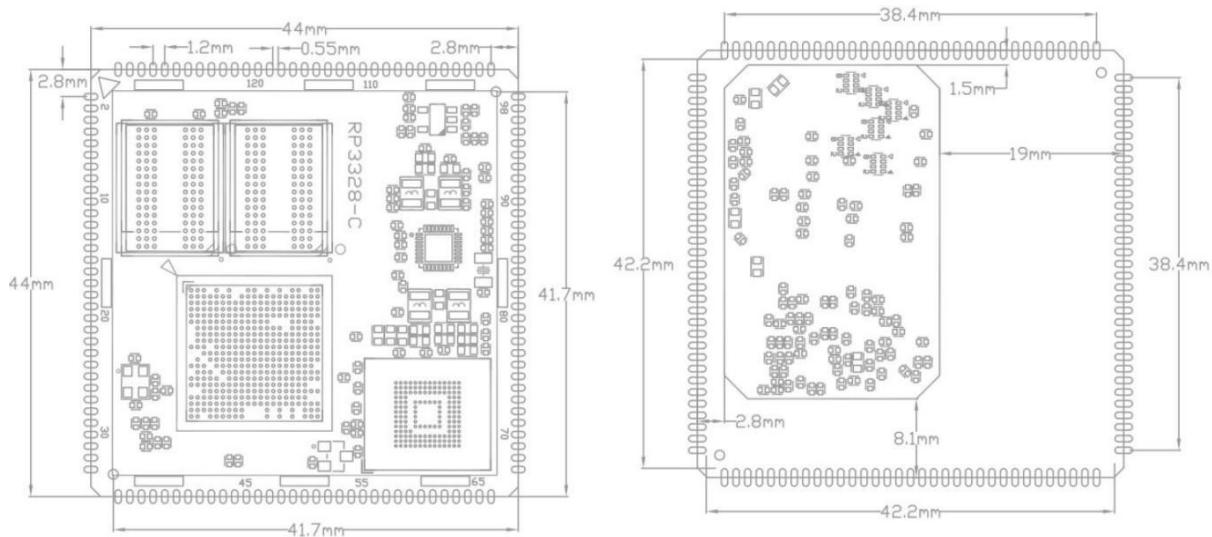
Debug UART2



If an RS232 Voltage level conversion chip is used, attention should be paid to the TXD and RXD directions.

PCB layout recommendations: If the Debug function is frequently used (such as in development boards or SDKs), it is recommended to add ESD devices to the interface to provide protection for the chip. When laying out the mainboard, it should be convenient to solder the DEBUG line.

7. Product Dimensions



Item	Parameter
Exterior	Stamp Hole
Core Board Size	44mm X 44mm X 3.5mm
Pin Spacing	1.2 mm
Pin Pad Size	1.6mm X 0.65mm
Number of Pins	132 Pins
Number of Layers	8 floors
Warpage	less than 0.5 %

8. The Methods of Coreboard Thermal Control

8.1. Thermal Control Strategy

There is a generic thermal system driver framework in the Linux kernel that defines a number of temperature control strategies. The following three strategies are currently in common use:

- **Power_allocator:** Introduces proportional-integral-derivative (PID) control, dynamically allocates power to each module based on the current temperature converts power to Frequency to achieve Frequency limiting based on temperature.
- **Step_wise:** Limits the Frequency in steps based on the current temperature.
- **User space:** Does not limit Frequency.

The RK3328 chip has a T-sensor that detects the chip's internal temperature and uses the Power_allocator strategy by default. The operating states are as follows:

- If the temperature exceeds the set temperature value:
 - If the temperature trend is rising, the Frequency is gradually reduced.
 - If the temperature trend is falling, the Frequency is gradually increased.
- When the temperature falls to the set temperature value:
 - If the temperature trend is increasing, the Frequency remains unchanged.
 - If the temperature trend is falling, the Frequency is gradually increased.
- Suppose the Frequency reaches its maximum and the temperature is still below the set value. In that case, the CPU frequency is no longer under thermal control, and the CPU frequency becomes system load frequency modulation.
- If the chip is still overheating after the Frequency has been reduced (e.g., due to poor heat dissipation) and the temperature exceeds 95 degrees, the software will trigger a restart. If the restart fails due to deadlock or other reasons and the chip exceeds 105 degrees, the otp_out inside the chip will trigger an immediate shutdown by the PMIC.

Note: The temperature trend is determined by comparing the previous and current temperatures. If the device temperature is below the threshold, the temperature is sampled every 1 seconds; if the device temperature exceeds the threshold, the temperature is sampled every 20ms, and the Frequency is limited.

8.2. Thermal Control Configure

The RK3328 SDK provides separate thermal control strategies for the CPU and GPU. Please refer to the ([Rockchip_Developer_Guide_Thermal](#)) document for specific configurations.

9. Production Guide

9.1. SMT process

Select modules that can be SMT or in-line packaged according to the customer's PCB design scheme. If the board is designed for SMT packaging, use SMT-packaged modules. If the board is designed for in-line assembly, use in-line assembly. Modules must be soldered within 24 hours of unpacking. If not, place them in a dry cabinet with a relative humidity of no more than 10% or re-pack them in a vacuum and record the exposure time (total exposure time must not exceed 168 hours).

Instruments or equipment required for SMT assembly:

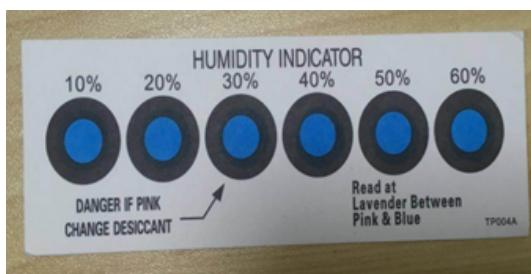
- SMT Mounter
- SPI
- Reflow soldering
- Oven temperature tester
- AOI

Instruments or equipment required for baking:

- Cabinet ovens
- Antistatic high-temperature trays
- Antistatic and high-temperature gloves

9.2. Module storage conditions:

Moisture-proof bags must be stored at a temperature <40°C and humidity <90% RH. Dry-packed products have a shelf life of 12 months from the date of sealing of the package—sealed packaging with a humidity indicator card.



9.3. Baking is required when:

The vacuum bag is found to be broken before unpacking.

After unpacking, the bag is found to be without a humidity indicator card.

The humidity indicator card reads 10% or more after unpacking, and the color ring turns pink.

Total exposure time after unpacking exceeds 168 hours.

More than 12 months from the date of the first sealed packaging.

Baking parameters are as follows:

Baking temperature: 60°C for reel packs, humidity less than or equal to 5% RH; 125°C for tray packs, humidity less than or equal to 5% RH (high-temperature-resistant trays, not blister packs for tow trays).

Baking time: 48 hours for reel packaging; 12 hours for pallet packaging.

Alarm temperature setting: 65°C for reel packs; 135°C for pallet packs.

After cooling to below 36°C under natural conditions, production can be carried out.

If the exposure time after baking is greater than 168 hours and not used up, bake again.

If the exposure time is more than 168 hours without baking, it is not recommended to use the reflow soldering process to solder this batch of modules. The modules are class 3 moisture-sensitive devices and may become damp when the exposure time is exceeded. This may lead to device failure or poor soldering when high-temperature soldering is carried out.

9.4. ESD

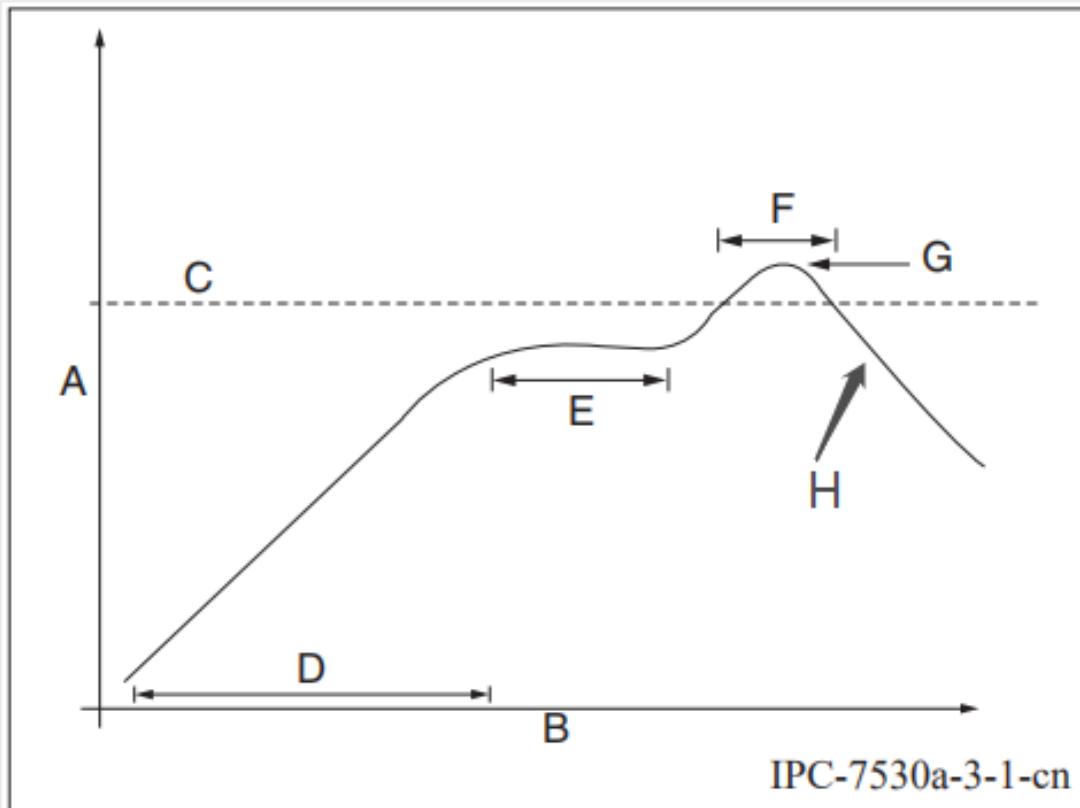
Please protect the module from electrostatic discharge (ESD) during the entire production process.

9.5. Conformity

To ensure product qualification rates, it is recommended to use SPI and AOI test equipment to monitor solder paste printing and placement quality.

9.6. Recommended Furnace Temperature Profile

Please follow the reflow profile for SMT placement with a peak temperature of 245°C. The reflow temperature profile is shown below using the SAC305 alloy solder paste.

**Description for graphs of curves.**

A: Temperature axis

B: Time axis

C: Alloy liquid phase line temperature: 217-220°C

D: Slope of temperature rise: 1-3°C/s

E: Constant temperature time: 60-120s, constant temperature: 150-200°C

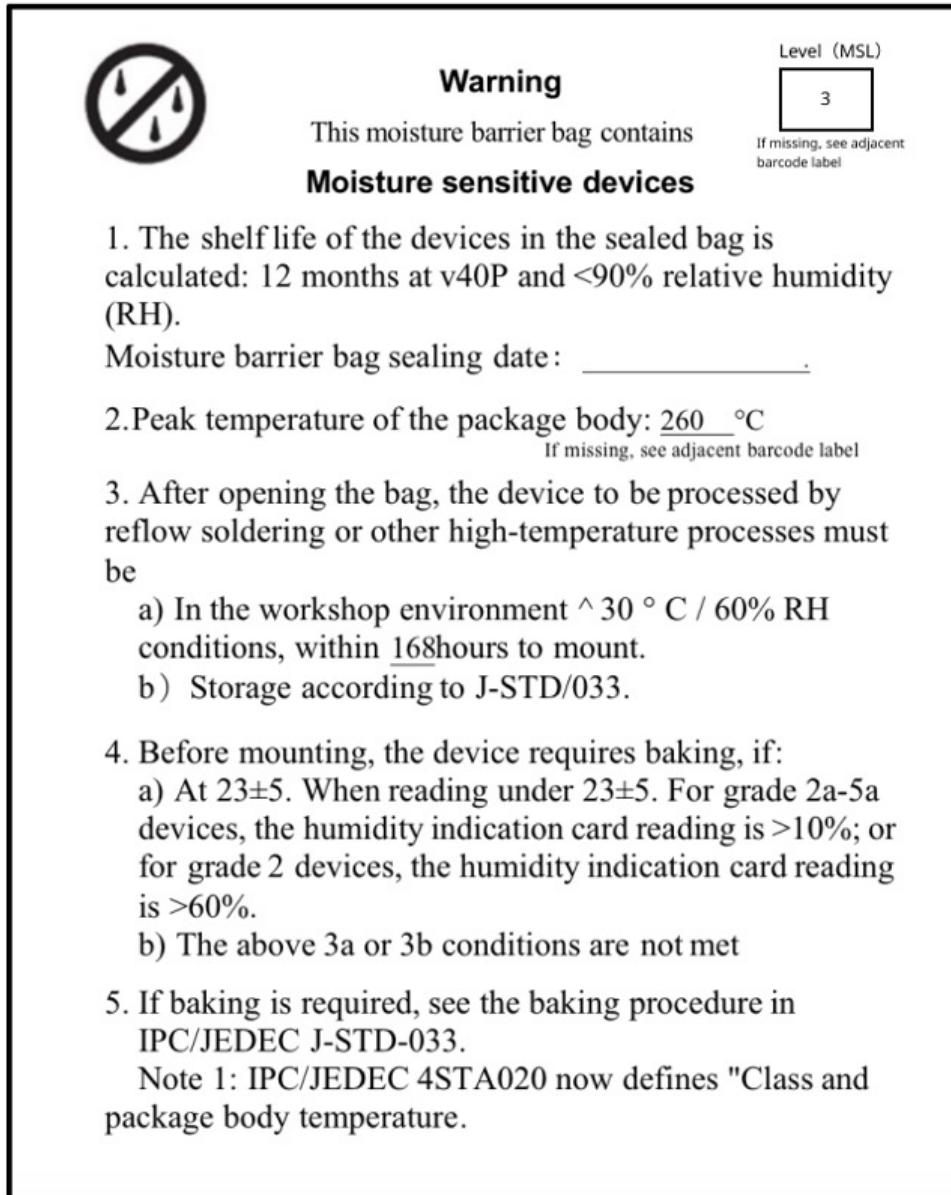
F: Time above liquid phase line: 50-70s

G: Peak temperature: 235-245°C

H: the slope of temperature reduction: 1-4°C/s

Note: above-recommended curves are based on SAC305 alloy solder paste as an example. Please set the recommended oven temperature curve for other alloy solder pastes according to the solder paste specification.

9.7. Storage



9.8. Order Information

Model	RAM	eMMC
DSOM-010R-1	2GB	8GB
DSOM-010R-2	2GB	32GB
DSOM-010R-3	2GB	128GB
DSOM-010R-2	2GB	16GB
DSOM-010R-3	1GB	8GB