Fully Differential Gilbert Cell Mixer Design

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Fully Differential Double Balanced Gilbert Mixer

1) Introduction

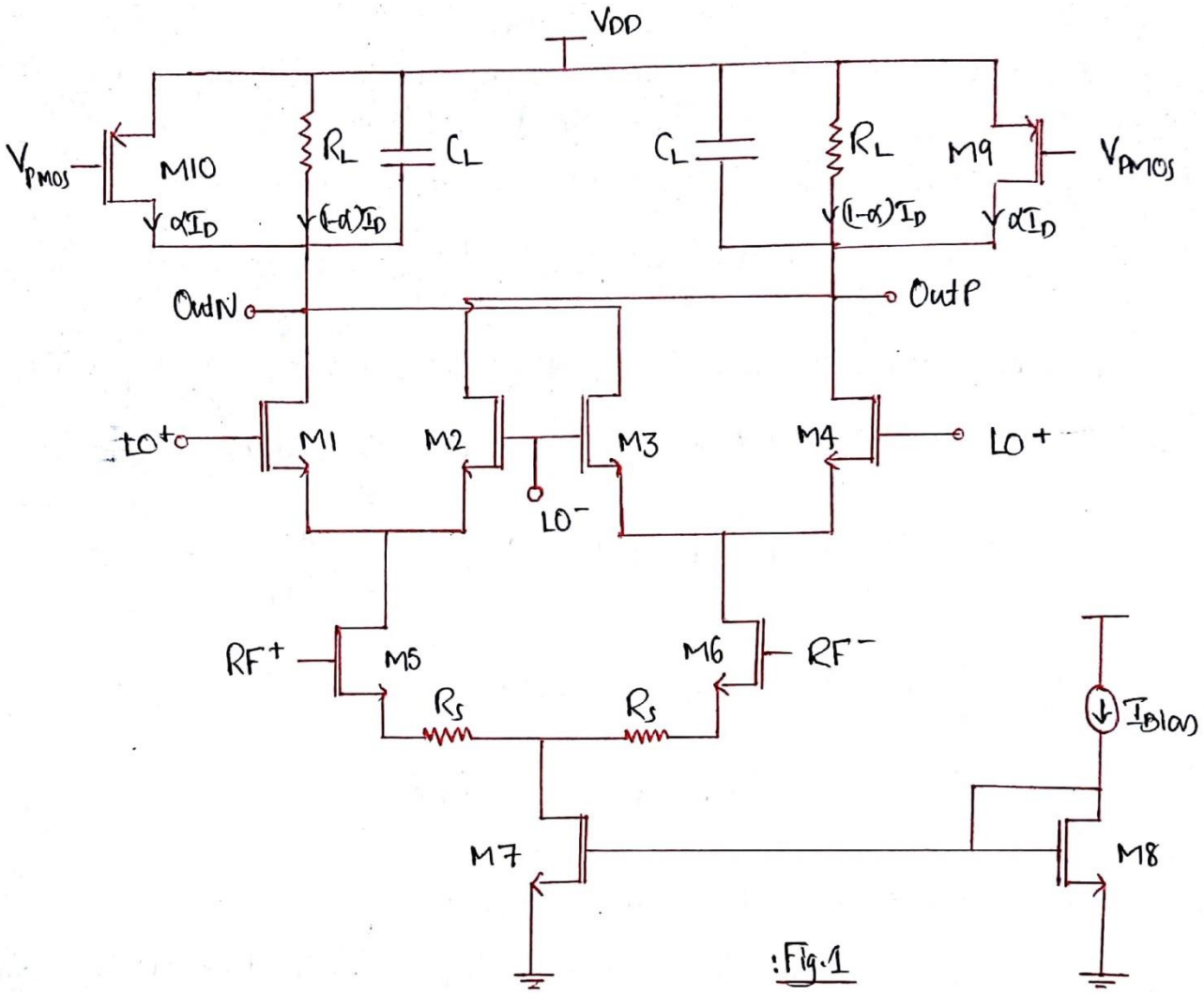
This project consists of design and simulation (in Eldo circuit simulator) of Fully differential Gilbert Cell mixer that works for Local Oscillator frequencies form 2.3GHz to 2.6GHz in IBM 90nm technology. The other specifications of the mixer are given below;

Specifications:

- VDD = 1.2V
- Conversion Gain > 15dB
- SSB Noise Figure >13dB
- IIP2 > 50dBm
- IIP3 > 5dBm
- Gain expansion < 2dB

IIP2 plot should be plotted under a mismatch of 0.1% between the two halves of the differential mixer. The bias transistor and current mirror transistors shouldn't be altered in this case since both of these are not part of differential pair. But IIP3 plot should be simulated under no mismatch between the two halves of Gilbert mixer. Gain expansion in IM2 and IM3 curves shouldn't be more than 2dB(not given as specification)

2) Circuit Diagram



:Fig.1

* M1, M2, M3 and M4 ⟶ Switching transistors
* M5 and M6 ⟶ Gm-stage transistors
* M7 and M8 ⟶ Bias transistors
* M10 and M9 ⟶ PMOS transistors for enhanced transconductance

Bulk terminals of all NMOSs are connected to ground and that of PMOSs are connected to V_{DD} (not shown in Fig.1).

Two resistors with value R_S (usually less than R_L) is used for better linearity of the circuit [2].

Take $\alpha = 0.7$

3) Hand Design

Refer Fig 1 : Apply KVL from V_{DD} to ground through $R_L - M1 - M5 - M7$.

$$V_{DD} = (1-\alpha) I_D R_D + 3V_{ov} \quad \text{-----} (1)$$

Assuming all the transistors will be in saturation during mixer operation and $V_{DSAT} = V_{ov}$ for all the NMOS transistors.

From the small signal analysis of the circuit in Fig 1;

$$\text{Voltage Conversion Gain, } V_{CG} = \frac{R_L(2/\pi)}{R_S + (1/g_{m6})} \geq 15\,dB = 5.62\ v/v \quad \text{----} (2)$$

On substituting the values $R_L = 10k\Omega$ and $R_S = 10\Omega$; $1/g_{m6} \leq 1769.359$

So $g_{m6} \geq 0.565\,mA/v \longrightarrow$ Take "$g_{m6} = 1mA/v$" ---- (3)

Put $I_D = \frac{g_{m6} V_{ov}}{2}$ in eqtn (1) ; "$V_{ov} = \left[\frac{2V_{DD}}{(1-\alpha) g_m R_D + 6}\right] = 0.312V$" ---- (4)

From (3) and (4) ; "$I_D = 88.14\mu A$" ----- (5)

Since $\alpha = 0.7$, "$I_{D9} = I_{D10} = 61.698\mu A$" ---- (6)

* Width Calculation of Bias NMOS (M7):

Here $V_S = 0v$, $V_D = V_{ov} = 0.312v$, $V_{Th} = 220mV$ (Based on simulation)

Then take $V_G = 0.532v$

On sweeping the value of W for $L = 500nm$, it is obtained that:

"$W_7 = 28.365\mu m$" for $I_{D_7} = 2 \times 88.14\mu A = 176.28\mu A$

* Width Calculation of Gm-NMOS (M5 and M6):

Here $V_{S6,5} = (V_{D7} + I_{D6} R_D) = 0.3129v$, $V_{Th} = 240mV$ (Based on simulation)

$V_{D6,5} = 0.6249v$

Then take $V_{G6,5} = 0.8649v$.

For $I_{D6} = I_{D5} = 88.14\mu A \longrightarrow$ "$W_6 = W_5 = 25.865\mu m$"

* Width Calculation of Switching NMOS (M1, M2, M3 and M4):

Here $V_S = 0.6249v$, $V_D = 0.9369v$ and $V_{Th} = 260mV$ (Based on simulation)
Then take $V_G = 1.197v$

For $I_{D_1} = I_{D_2} = I_{D_3} = I_{D_4} = 88.14\mu A$ Take " $W_1 = W_2 = W_3 = W_4 = 43.461\mu m$ "

* Width of PMOS (M9 and M10):

Here $V_S = 1.2v$, $V_D = 0.9369v$, $V_{Th} = 0.218v$ (Based on simulation)
Then take $V_G = 0.815v$

For $I_{D9} = I_{D10} = 61.698\mu A \longrightarrow$ Take " $W_9 = W_{10} = 20.362\ \mu m$ "

* Calculation of R_L and C_L:

- From Fig. 1; $(V_O)_{M9} = (V_{SD})_{M10} = \alpha I_D R_L = 0.3 \times 88.14 \times 10^{-6} \times R_L$
$= (2.6442 \times 10^{-5}) R_L$

Since $(V_{SD})_{M9} = 0.2631v \longrightarrow$ Take " $R_L = 10k\Omega$ " $\longrightarrow$ It will give slight variation in DC operating points

- The output parallel R and C acts as a low pass filter to filter out the frequencies above base band frequency (ie 20 MHz).

Take $f_{-3dB} = 50MHz = \frac{1}{2\pi R_L C_L} \longrightarrow$ Take " $C_L = 0.318pF$ "

* Width Calculation of current Mirror (W_{CS}):

Take $W_{CS} = (W_7/10) \longrightarrow \because I_{Bias} = (I_{D7}/10)$

So " $W_{CS} = 2.8365\mu m$ "

Hand calculated of specifications

i) $V_{IIP_2} = 4(V_{GS}-V_{Th})_{5,6} \cdot \frac{V_{LO}}{V_{OS}}$ ------> From [1]

where V_{LO} is the amplitude of square pulse given to LO port
V_{OS} is the gate offset voltage given to RF port-transistors

From the hand design; $(V_{GS}-V_{Th})_{3,6} = 0.312\,V$

$V_{LO} = 0.68\,V$

Offset voltage (V_{OS}) is calculated from the design by applying 0.1% mismatch between the two halfs of the differential pair.

$V_{OS} = 10\,\mu V$ ----> From the simulation

So "$IIP2 = 98.574\,dBm$"

ii) $P_{IIP3} \approx \frac{8}{3} \cdot \frac{V_{sat_6} L}{\mu_6 R_S} V_{OV} \left(1 + \frac{\mu_1 V_{OV6}}{4 V_{sat_6} L}\right)\left(1 + \frac{\mu_1 V_{OV6}}{2 V_{sat_6} \cdot L}\right)^2$ ----> From [2]

From simulation; (DCOP simulation) $V_{sat6} = 91.75\,mV$ and $V_{DS6} = 0.383\,V = V_{OV6}$
$= V_{sat5}$

So "$P_{IIP3} \approx 10.789\,dBm$"

iii) SSB Noise Figure, $NF_{SSB} = 1 + \frac{1}{4KTR_S}\left\{\overline{i_n^2} KT\left(\frac{\gamma}{g_{m6}} + \frac{2}{g_{m6}^2 R_L}\right)\right\}$

$= 1 + \frac{\pi^2}{4R_S}\left\{\frac{\gamma}{g_{m6}} + \frac{2}{g_{m6}^2 R_L}\right\}$

Put $\gamma = (2/3)$, $g_{m6} = 0.565\,mA/V$ ⟶ "$NF_{SSB} = 11.6\,dB$"

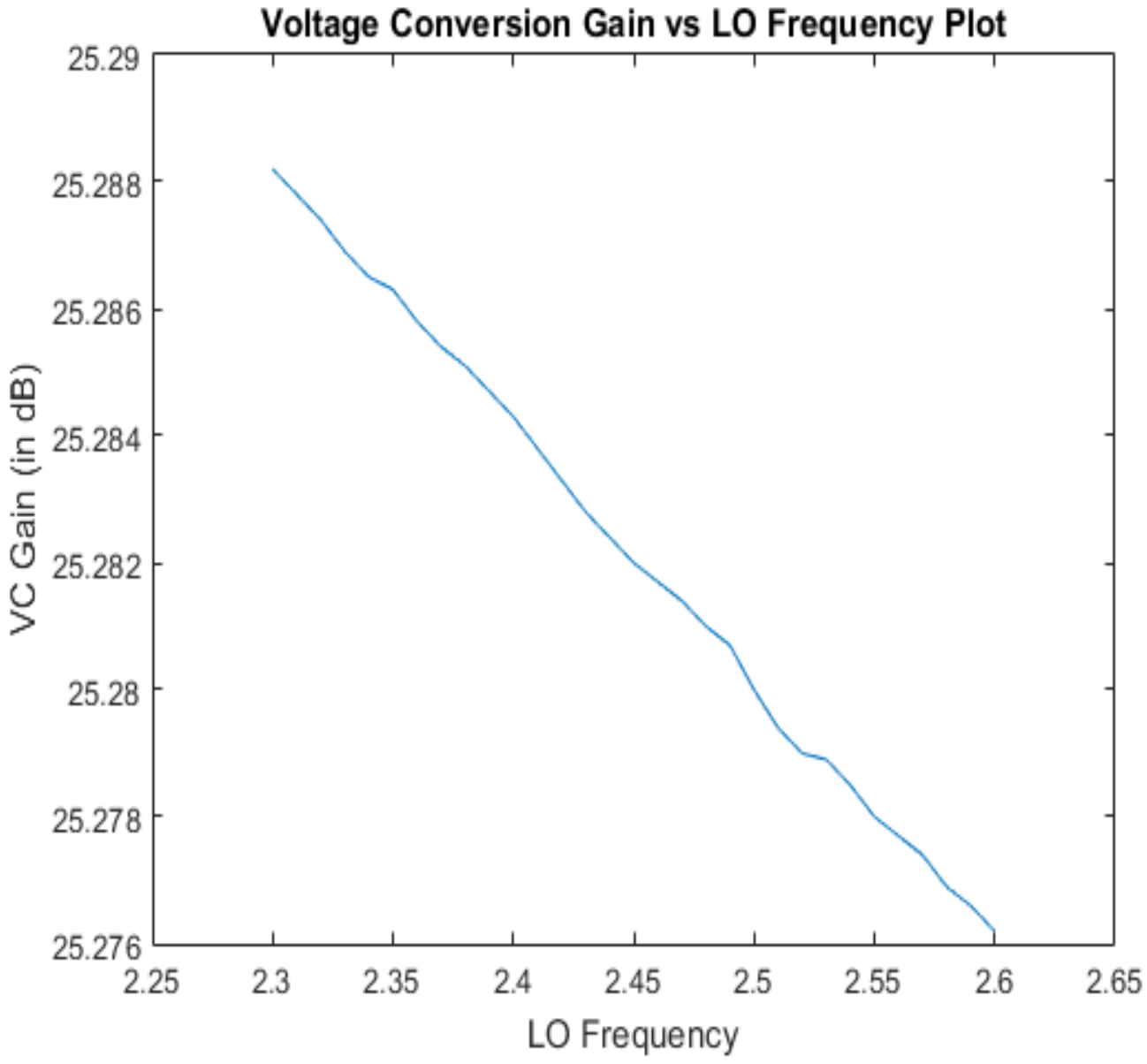
4) Results

a. Main Results

i. Voltage Conversion Gain v/s LO frequency Plot

A differential RF input of 10uV is applied to the RF port of the mixer and the ratio of Power of IM1 harmonic at IF port and the input at RF port are measured. For the entire simulation for finding voltage conversion gain, the LO frequency and RF frequency differs by 20MHz.

The plot of VC gain v/s LO frequency is given below (in Fig.1);



: Fig.1

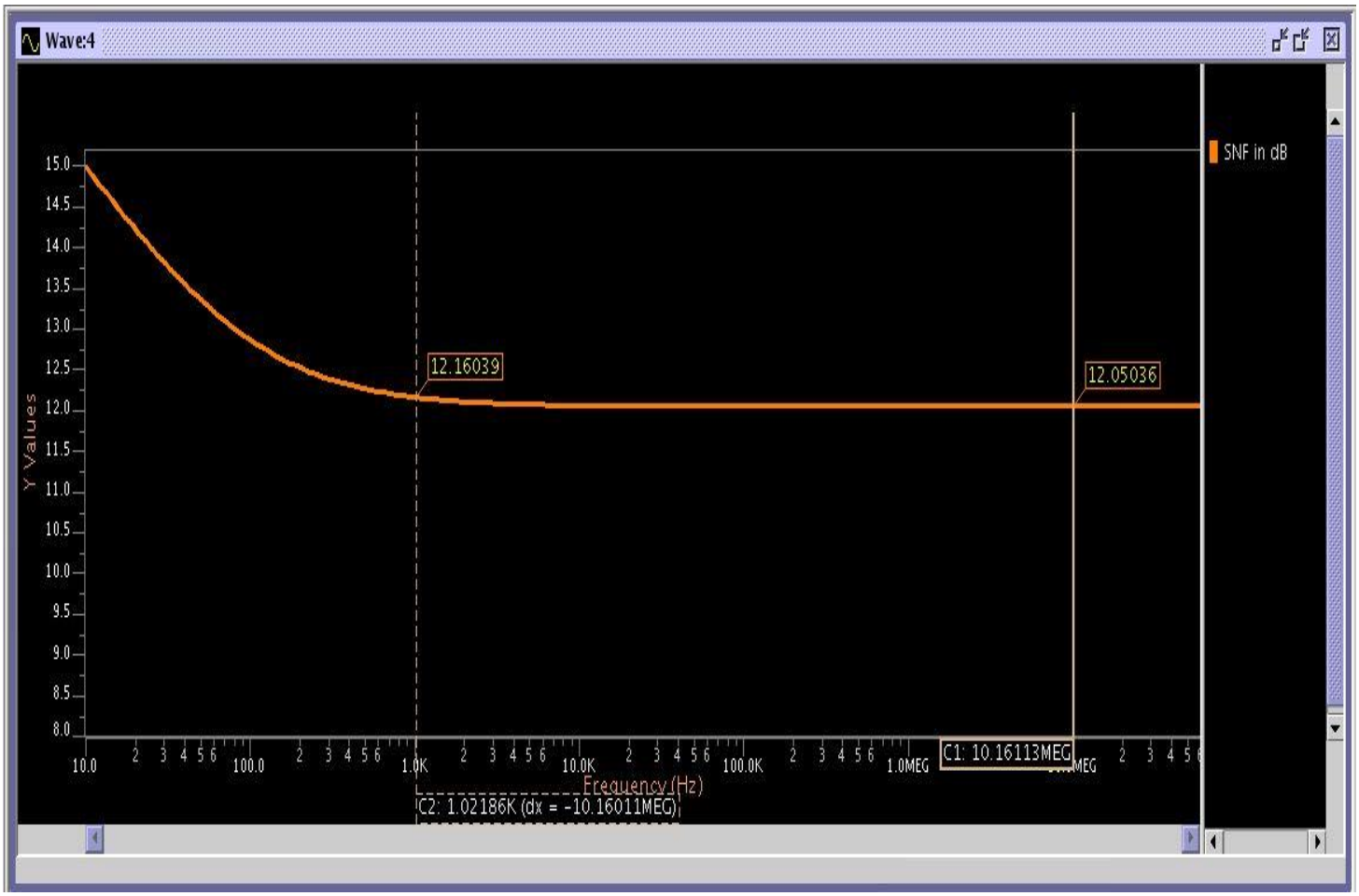
The VC gain v/s LO frequency values are tabulated in Table.1;

LO Frequency (in GHz)	VC Gain (in dB)
2.3	25.2882
2.31	25.2878
2.32	25.2874
2.33	25.2869
2.34	25.2865
2.35	25.2863
2.36	25.2858
2.37	25.2854
2.38	25.2851
2.39	25.2847
2.4	25.2843
2.41	25.2838
2.42	25.2833
2.43	25.2828
2.44	25.2824
2.45	25.282
2.46	25.2817
2.47	25.2814
2.48	25.281
2.49	25.2807
2.5	25.28
2.51	25.2794
2.52	25.279
2.53	25.2789
2.54	25.2785
2.55	25.278
2.56	25.2777
2.57	25.2774
2.58	25.2769
2.59	25.2766
2.6	25.2762

: Table-1

The VC gain shows a maximum value around LO frequency equal to 2.45GHz. The Voltage conversion gain will decrease as the base band message frequency decrease. This happens due to the low pass action of RC circuit at the drain side of switching transistors.

ii. Noise Figure



The screenshot of simulation results of top noise contributors are given below;

CONTRIBUTION FROM INDIVIDUAL INTERNAL NOISE SOURCES TO NOISE_PSD (SQ V/Hz):

M3	-> Flicker noise :	1.2028E-18
M4	-> Flicker noise :	1.2028E-18
M1	-> Flicker noise :	1.2028E-18
M2	-> Flicker noise :	1.2028E-18
M3	-> Thermal noise :	8.9195E-19
M1	-> Thermal noise :	8.9195E-19
M2	-> Thermal noise :	8.9195E-19
M4	-> Thermal noise :	8.9195E-19
M9	-> Thermal noise :	1.5148E-20
M10	-> Thermal noise :	1.5148E-20
M6	-> Thermal noise :	9.8202E-21
M5	-> Thermal noise :	9.8202E-21
M9	-> Flicker noise :	3.8559E-21
M10	-> Flicker noise :	3.8559E-21
R2	-> :	1.9254E-22
R1	-> :	1.9254E-22

At 10KHz

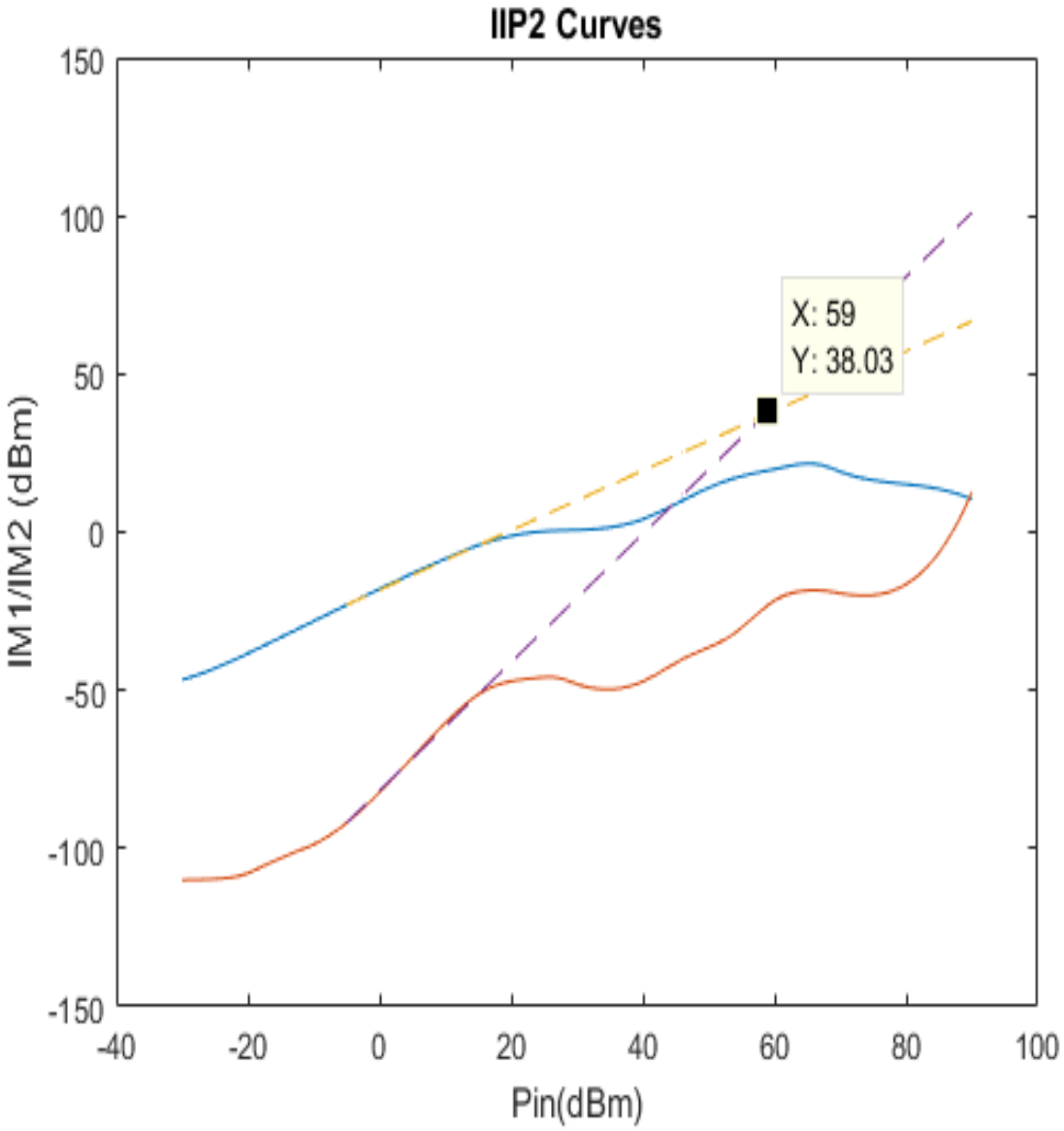
CONTRIBUTION FROM INDIVIDUAL INTERNAL NOISE SOURCES TO NOISE_PSD (SQ V/Hz):

M3	-> Thermal noise :	8.9195E-19
M1	-> Thermal noise :	8.9195E-19
M2	-> Thermal noise :	8.9195E-19
M4	-> Thermal noise :	8.9195E-19
M10	-> Thermal noise :	1.5148E-20
M9	-> Thermal noise :	1.5148E-20
M5	-> Thermal noise :	9.8202E-21
M6	-> Thermal noise :	9.8202E-21
M3	-> Flicker noise :	2.0902E-21
M4	-> Flicker noise :	2.0902E-21
M1	-> Flicker noise :	2.0902E-21
M2	-> Flicker noise :	2.0902E-21
R1	-> :	1.9254E-22
R2	-> :	1.9254E-22

At 10MHz

iii. IIP2 Plot

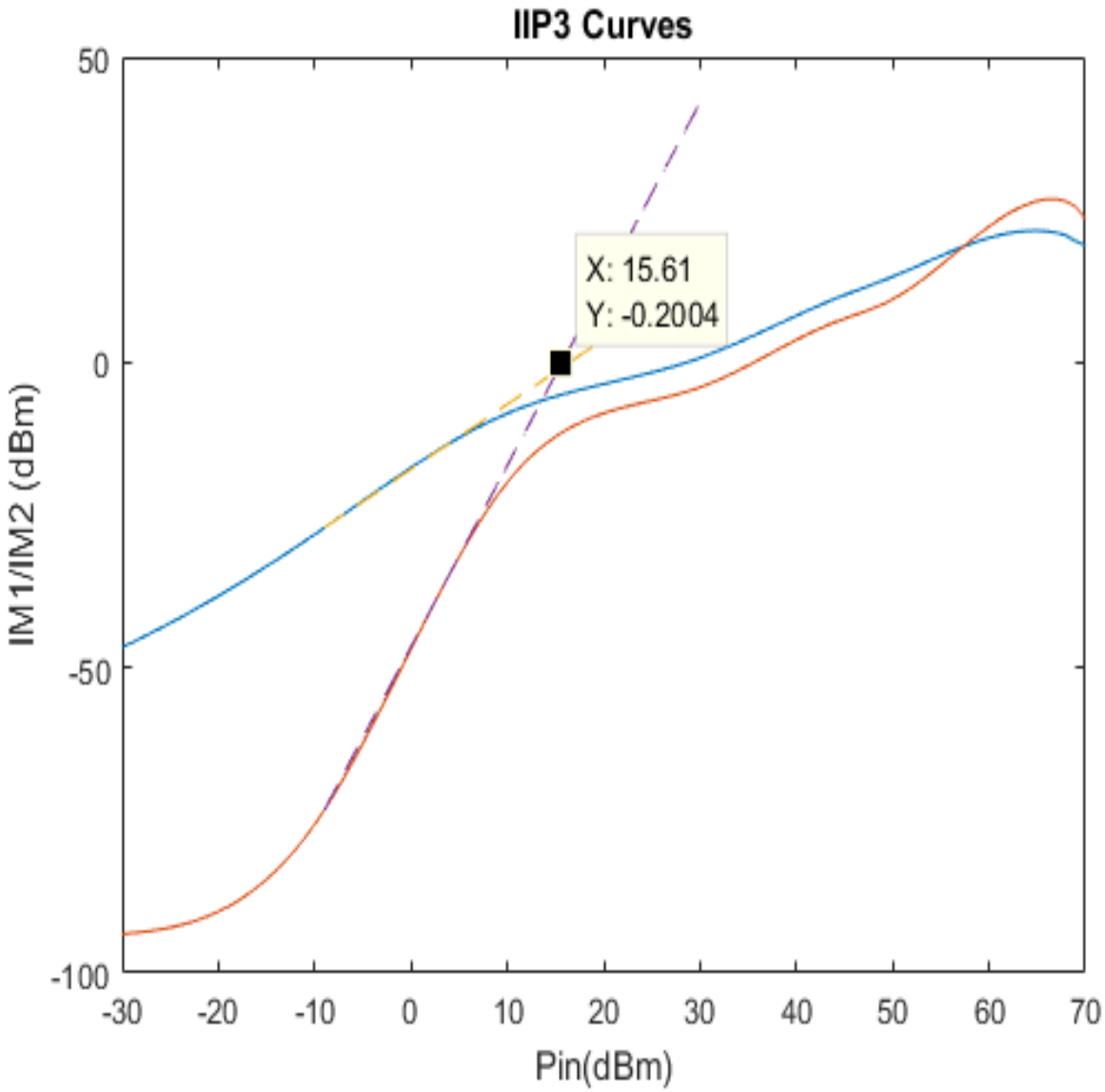
The IIP2 simulation is done after making a mismatch of 0.1% between the two halves of the differential Gilbert mixer. The width of transistors, resistance value and capacitance values are changed on both sides of differential Gilbert mixer so that the average value of both the sides equals with our initial design.



Simulated IIP2 Value = 59dBm

Simulated OIP2 Value = 38.03dBm

iv. IIP3 Plot



Simulated IIP3 Value = 15.61dBm

Simulated OIP3 Value = -0.2004dBm

5) Comparison of Simulated Results & Designed Values

a. Comparison of Circuit Design Variables

Design Variables	Designed Value	Simulated Value
I_{Bias}	17.628uA	17.64uA
I_{D7}	176.28uA	182.82uA
I_{D5}, I_{D6}	88.14uA	91.41uA
I_{D1}, I_{D2}, I_{D3}, I_{D4}	88.14uA	91.41uA
I_{D9}, I_{D10}	61.698uA	66uA
I_{RL}	26.442uA	25.41uA
ά (Alpha)	0.3	0.278
RFBias	0.815V	0.845V
LOBias	1.197V	1.2V
PMOSBias	0.8649V	0.8649V
gm_5, gm_6	1mA/V	0.942mA/V

b. Comparison of Design Specifications

Specification	Designed Value	Simulated Value
VC Gain	21.995dB	25.2914dB
SSB Noise Figure (at 10KHz)	11.6dB	12.16dB
IIP2	98.574dBm	59dBm
IIP3	10.789dBm	15.61dBm
Power Dissipation	370.188uW	383.28uW

6) References

[1] RF Microelectronics, 2nd Edition by Behzad Razavi, Prentice Hall Publications

[2]https://www.google.co.in/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=0ahUKEwisgNPV35PaAhUCT48KHU69BJcQFggmMAA&url=http%3A%2F%2Fwww.odyseus.nildram.co.uk%2FRFIC_Circuits_Files%2FMOS_Gilbert_Cell_Mixer.pdf&usg=AOvVaw1G-tR_WRm2eCXcx3m7grsq

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