Analog IC Design (EE5320): Project Report

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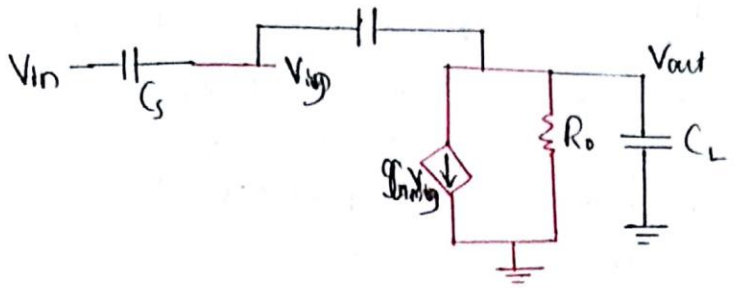
1) Design Approach

Design Procedure

* The amplifier used in the given circuit can be briefly represented as a transconductor. Refer the figure given below;



: Model-1

Here $\frac{V_{out}(s)}{V_{in}(s)} = -\frac{C_S}{C_F} \cdot \frac{\beta A_{DC}}{1+\beta A_{DC}} \cdot \frac{(1-s/\omega_Z)}{(1+s/\omega_P)}$ where $\omega_Z = \frac{G_m}{C_F}$ & $\omega_P = \frac{\beta G_m}{C_L + (1-\beta)C_F}$

$\beta = \frac{C_F}{C_F + C_S}$

The static error $= \frac{1}{\beta A_{DC}}$ & Dynamic error, $\epsilon_d(t_s) = \left(1 + \frac{\omega_P}{\omega_Z}\right) \exp\left(\frac{-t_s}{\tau}\right)$

The given specification are as follows;

Closed loop gain = 4 ----> Spec-①

Max.(Static + Dynamic error) = $2 \times 10^{-4} V = 0.2mV$ ----> Spec-②

$(Settling\ time)_{max} = 5ns$ ----> Spec-③

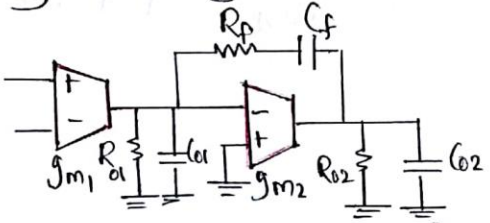
$|Closed\ loop\ gain| = \frac{C_S}{C_F} = 4 \longrightarrow C_S = 4C_F$ ----> Design-①

From Design-①; $\beta = 1/5$. From spec-① ; $A_{DC} \geq$

* Due to high gain requirement, we are using two stage amplifier with sufficient compensation techniques.

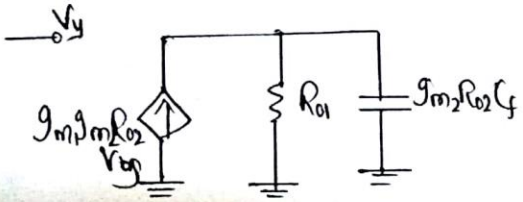
Here $\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}R_{o1} \cdot g_{m2}R_{o2}}{(1+s/\omega_{P1})}$

where $\omega_{P1} = \frac{1}{R_{o1}R_{o2} \cdot g_{m2}C_F}$



: Two stage amplifier Model

Comparing this model with model-1 (earlier discussed model); then



$G_m = g_{m1}g_{m2}R_{o2}$ & $C_L = g_{m2}R_{o2}C_F$

So Dynamic error, $\epsilon_d(t_s) = \left(1 + \frac{\omega_P}{\omega_Z}\right) e^{-t_s/\tau}$

$\frac{\omega_P}{\omega_Z} = \frac{\beta}{\frac{C_L}{C_F} + (1-\beta)} = \frac{1}{4 + \frac{5g_{m2}R_{o2}C_F}{C_F}}$

$\simeq \frac{1}{5g_{m2}R_{o2} \cdot \frac{C_F}{C_F}} << 1$ ----> Design-②

Take $\frac{C_f}{C_F} >> 1 \longrightarrow \underbrace{\varepsilon_d(t_1) \simeq e^{-t_1/\tau}}_{\text{Dynamic settling error}} \longrightarrow \tau = \frac{1}{\omega_p} = \frac{t_s}{\ln(1/\varepsilon_d(t_1))}$

* We know that; $\omega_p = \frac{\beta G_m}{C_L + (1-\beta)C_F} = \frac{\beta g_{m_1} g_{m_2} R_{o2}}{g_{m_2} R_{o2} . C_f + (1-\beta) C_F}$

Take $\frac{C_f}{C_F} >> 1 \longrightarrow \omega_p \simeq \frac{\beta g_{m_1} g_{m_2} R_{o2}}{g_{m_2} R_{o2} C_f} \simeq \frac{\beta g_{m_1}}{C_f}$

So $\frac{\beta g_{m_1}}{C_f} = \frac{\ln(1/\varepsilon_d(t_1))}{t_s} = \frac{\ln(0.1 \times 10^4) \times (1/3) 10^4}{2.25}$

Take $C_f = 1.9pF$ & $\beta = 1/3$ (already equal to $1/3$) $\longrightarrow g_{m_1} = 27.5\,mS$ ---> Design-③

* Phase margin $\geq 60^\circ \longrightarrow \tan^{-1}\left(\frac{\omega_u}{\omega_{p_2}}\right) = 180^\circ - \tan^{-1}\left(\frac{\omega_u}{\omega_{p_1}}\right) - PM$

We have; $\omega_{p_2} = \frac{g_{m_2}}{C_L}$, $\omega_{p_1} = \frac{\omega_u}{A_{DC}\beta}$, then

$$\tan^{-1}\left(\frac{\omega_u}{\omega_{p_2}}\right) = 180^\circ - 90^\circ - 60^\circ = 30^\circ \longrightarrow \frac{\omega_u C_L}{g_{m_2}} = \tan 30^\circ = \frac{1}{\sqrt{3}}$$

So $g_{m_2} = \frac{\omega_u C_L}{\tan 30^\circ}$ and $C_L = 2pF \longrightarrow g_{m_2} = \frac{2 \times 10^{-12} \times 2\pi \times 10^{10}}{1/\sqrt{3}}$

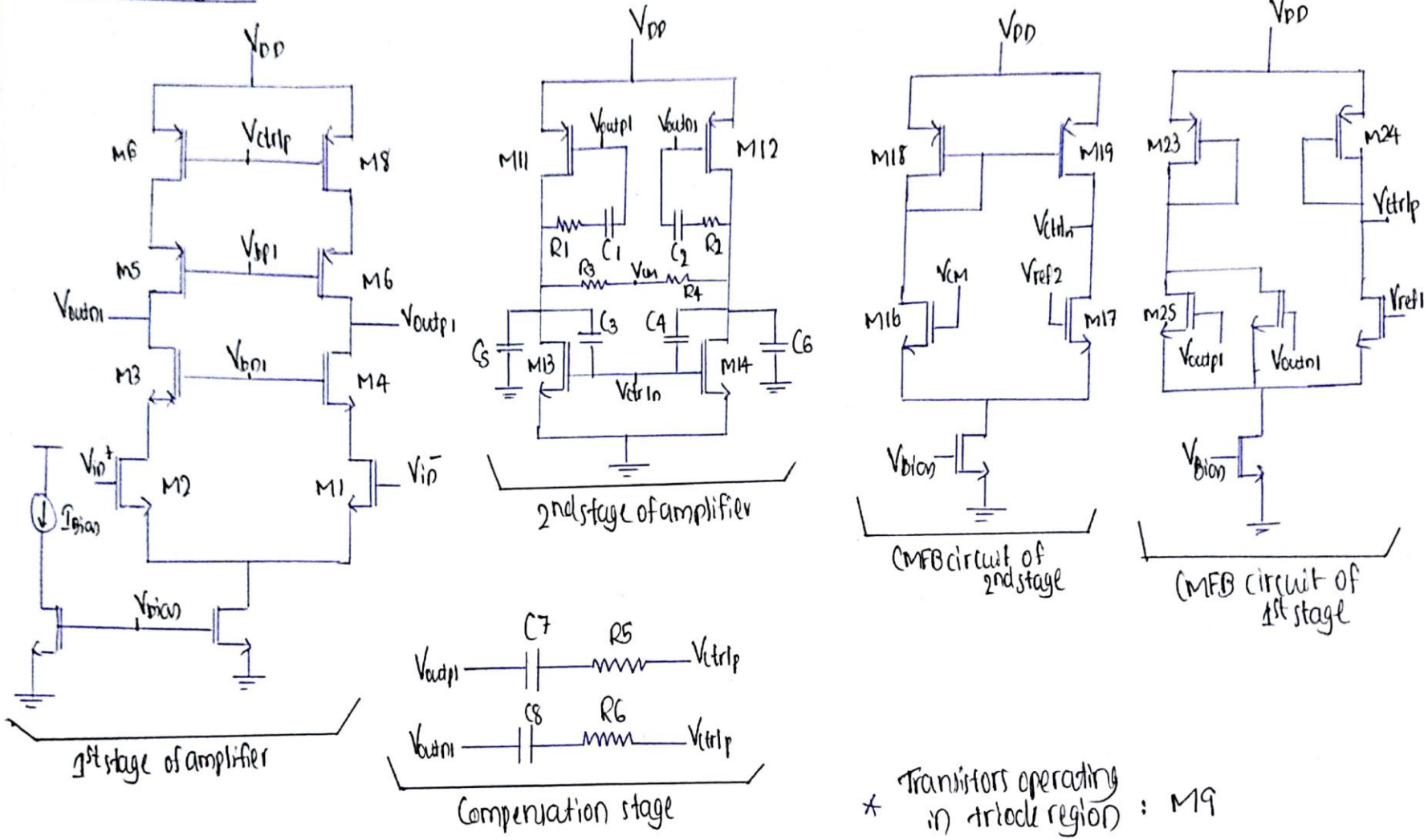
$= 76.21\,mS$ ---> Design-④

When $(V_{ov})_1 = 0.2v$ for $g_{m_1} = 27.5\,mS \longrightarrow I_{D_1} = 0.275mA$
When $(V_{ov})_1 = 0.2v$ for $g_{m_2} = 76.21mS \longrightarrow I_{D_2} = 0.219mA$
} $V_{ov} = 0.21v$ for best operation

So $I_{Bias} = 0.4945\,mA$ ---> Design-⑤

2) Amplifier Schematic

Circuit Diagram



* Transistors operating in triode region : M9

NB: The bulk terminal connection of transistors are avoided to reduce complexity in the circuit diagram while drawing.

3) Transistor Parameters

Device	Width (µm)	Length (µm)	Bias Current (mA)	Gm (in mS)	∆
M1	0.27	158.7	2.82	27.7	0.204
M2	0.27	158.7	2.82	27.7	0.204
M3	0.27	158.7	2.82	28.4	0.198
M4	0.27	158.7	2.82	28.4	0.198
M5	0.36	816.5	2.82	28.4	0.198
M6	0.36	816.5	2.82	26.1	0.216
M7	0.36	816.5	2.82	26.1	0.216
M8	0.36	816.5	2.82	26.1	0.216
M9	0.27	310.6	5.64	42.2	0.267
M10	0.27	20.13	.495	4.19	0.236
M11	0.36	3056.9	35.6	182	0.391
M12	0.36	3056.9	35.6	182	0.391
M13	0.27	595.9	35.6	168	0.423
M14	0.27	595.9	35.6	168	0.423
M15	0.27	589.8	12.5	104	0.240
M16	0.27	296.5	6.13	57.7	0.212
M17	0.27	296.5	6.34	57.9	0.219
M18	0.36	1545	6.13	57.8	0.212
M19	0.36	1545	6.34	59.4	0.213
M20	0.27	163.3	3.58	30.3	0.236
M21	0.27	39	1.26	9.03	0.279
M22	0.27	79.2	1.06	12.5	0.170
M23	0.27	39	2.51	14.8	0.339
M24	0.36	275	1.06	10.2	0.207
M25	0.36	275	1.26	9.03	0.279

4) Performance Summary

Design parameter / variable	Simulated Performance	Specification
Supply Voltage	1.8	≤1.8
Closed Loop Gain	4	4
Settling Error	1.87×10^{-4}	$\leq 2\times10^{-4}$
Load Capacitance	2pF	2pF
Settling Time	4.96ns	≤ 5ns
Peak SNR	115dB	≥ 62dB
Differential rms noise voltage [µV]	1.286×10^{-6}	—
THD (F_{in} = 1MHz)	-71.47dB	≤ -70dB
THD (F_{in} = 49MHz)	-37.7dB	≤ -70dB
Amplifier Core Power Consumption [mW]	164.36mW	Minimum
Bias Power Consumption [mW]	0.89mW	Minimum
Total Power Consumption [mW]	165.25mW	Minimum
Differential DC Loop Gain (v_{od} = 0) [dB]	81.95dB	—
Differential DC Loop Gain (v_{od} = $v_{od,max}$) [dB]	79.355dB	—
Differential Loop Gain Unity Gain Bandwidth [MHz]	151.59MHz	—
Differential loop-gain phase margin [deg]	75.79°	—
Differential loop-gain gain margin [dB]	27.166dB	—
Common-Mode loop-gain unity gain bandwidth [MHz]	1931.7MHz	—
Common-mode loop-gain phase margin [deg]	103.87°	—

5) Relevant Calculations

Relevant Calculations:

* We have taken $L = 0.27\mu m$ for all NMOSs and $L = 0.36\mu m$ for all PMOSs. (As already provided in the previous sections).

  Amplifier's DC gain, $A_{DC} = 82dB = 25589.254\ V/V$ } ---> Simulated values
  Amplifier feedback factor, $\beta = 1/5$

  Static settling error calculated, $\varepsilon_{ds} = \frac{1}{\beta A_{DC}} = 1.95 \times 10^{-4} V$ ---> within the specification

* Transconductance of first stage, $G_{m_1} = g_{m_1} = g_{m_2} = 27.7mS$

  So $\omega_p = (2.915\ GHz) \times 2\pi \Rightarrow \omega_p = 2.915 \times 10^9\ rad/sec$ --- (1)

  Settling time, $(t_s)_{calculated} = \frac{\ln(V_{ed(t)})}{\omega_p} = 2.931\ ns$ } ---> within specification
  Simulated settling time, $(t_s)_{sim} = 4.96ns$

* Power consumption:

  Bias power consumption, $P_{Bias} = I_{bias} \times V_{DD} = 0.8901\ mW$
  Total power consumption, $P_{total} = I_{total} \times V_{DD} = 165.25mW$
  ($I_{Bias} = 0.4945\ mA$ & $I_{total} = 91.806\ mA$ ---> Both from final simulation)

* Unity gain bandwidth calculated, $(\omega_u)_{calc} = A_{DC} \times \omega_{p_1} = 25589.254 \times 157 \times 10^5\ rad/sec$
  $= 4.019 \times 10^9\ rad/sec = 639.69\ MHz$

  Unity gain bandwidth simulated $(\omega_u)_{sim} = 639.6\ MHz$

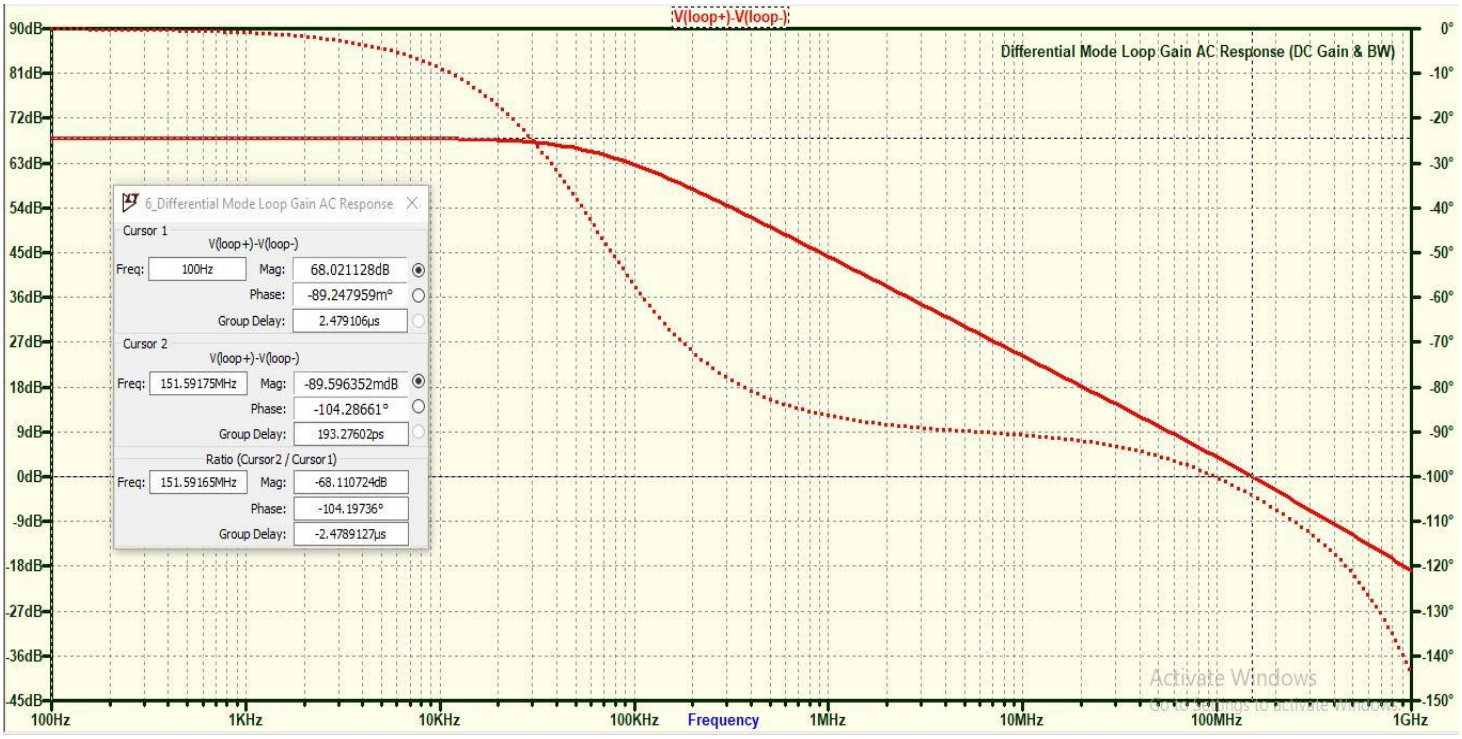
NB: The calculated values of the specifications are based on the re-iterated-simulated values of the other parameters and parameter value (simulated) is the exact value ~~after~~ obtained after simulation.

* The transistor sizes are designed based on the individual simulation of NMOS in which the approximated size is ~~cat~~ found out using required g_m and V_{OV} of the transistors. The accurate size of the transistors are found out using iterative simulation of the transistor with fixed terminal voltages (V_G, V_S, V_D are fixed based on circuit requirement) and fixed drain current (Sweep of MOS width is used in this case).

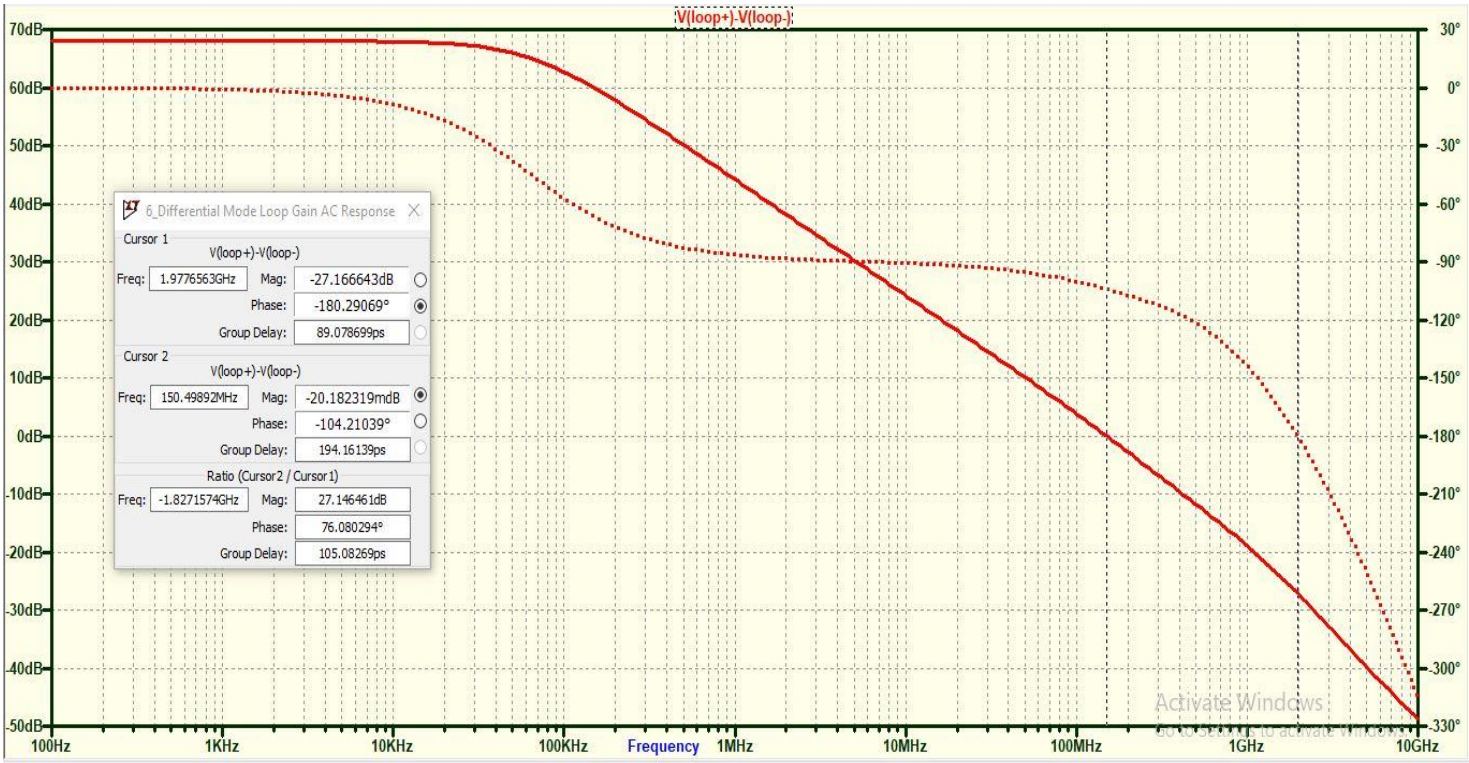
  For example consider the first amplifier stage of the differential-input differential-output amplifier. The V_{DS} values of the transistors in the stack of four transistors (2 PMOS + 2 NMOS) and bottom current sink NMOS are taken in such a way that $0.4 = (V_{DS})_{M4} = (V_{DS})_{M4} = (V_{DS})_{M7,8}$ but $(V_{DS})_{M9} = 0.13V$

6) Simulation Results

a. Differential Mode Loop Gain AC Response

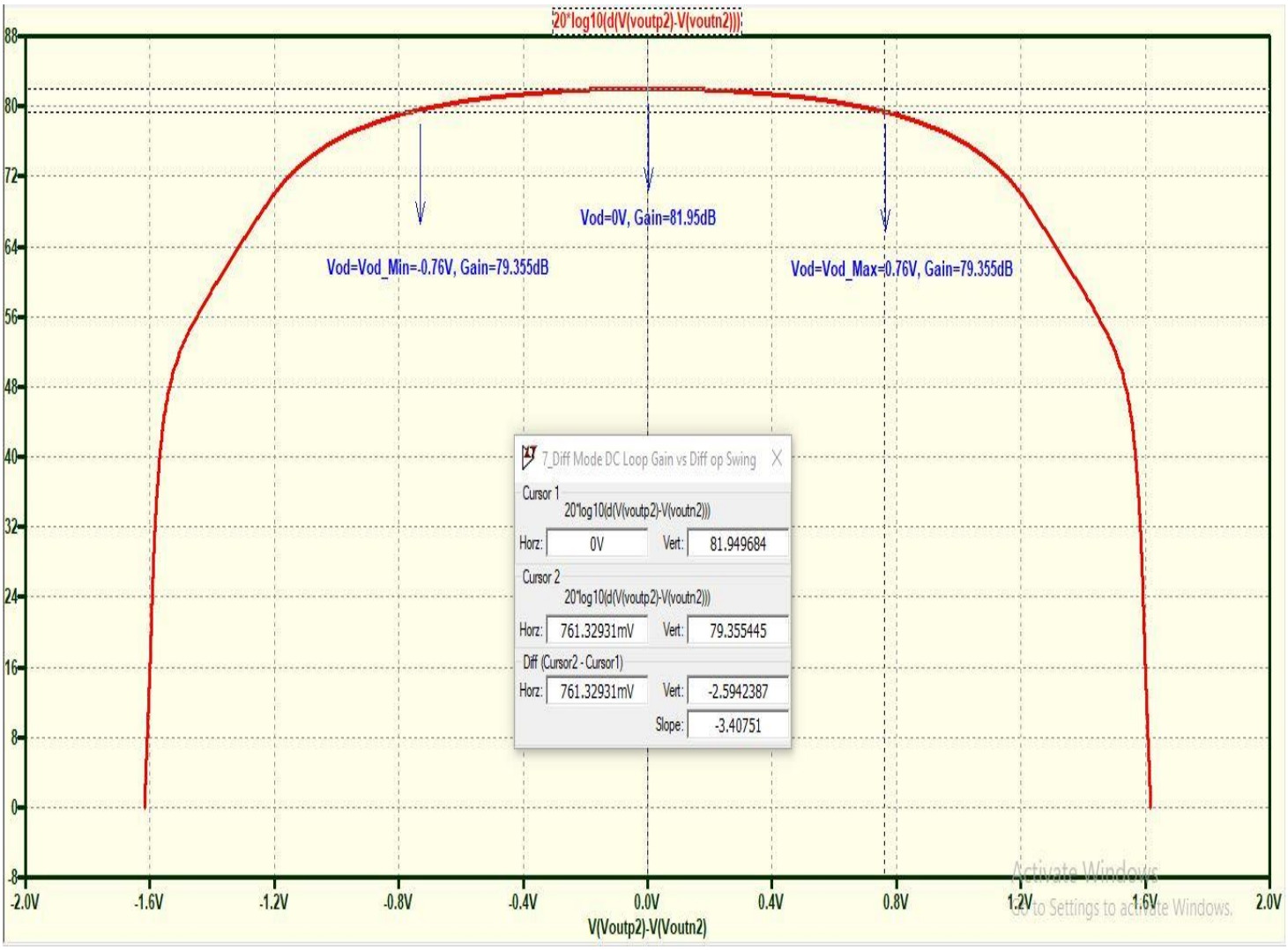


：DC Gain & Loop Bandwidth

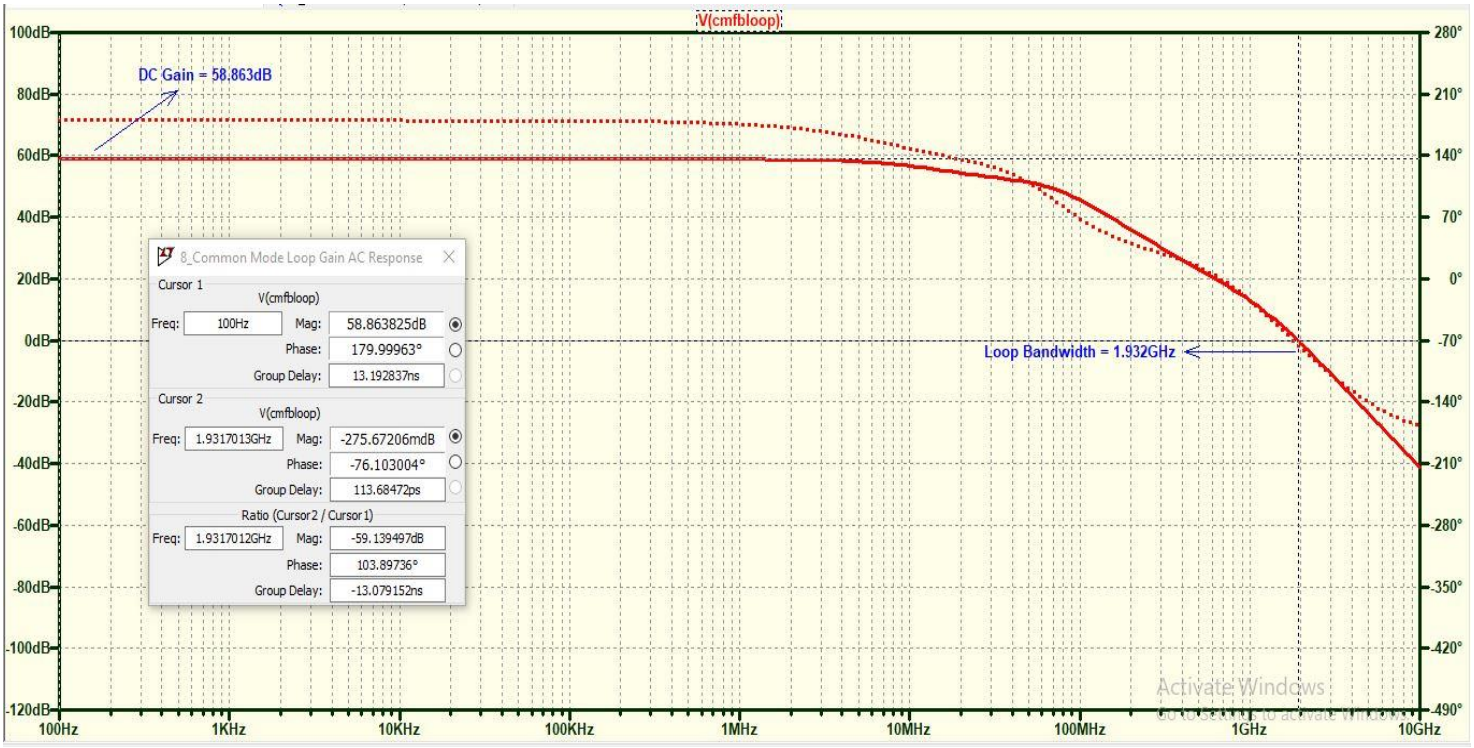


：Phase Margin & Gain Margin

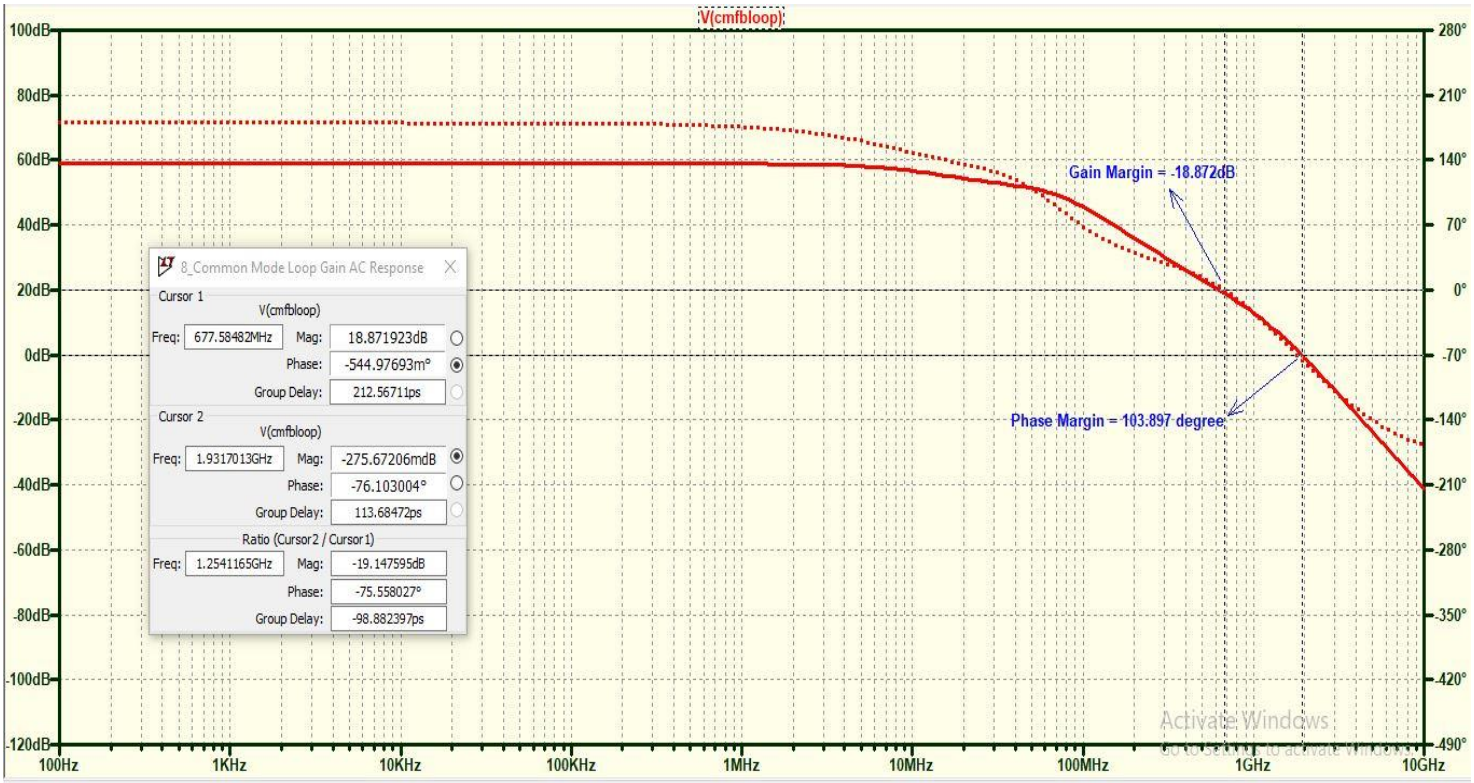
b. Differential Mode DC Loop Gain v/s Differential O/P Swing



c. Common Mode Loop Gain AC Response

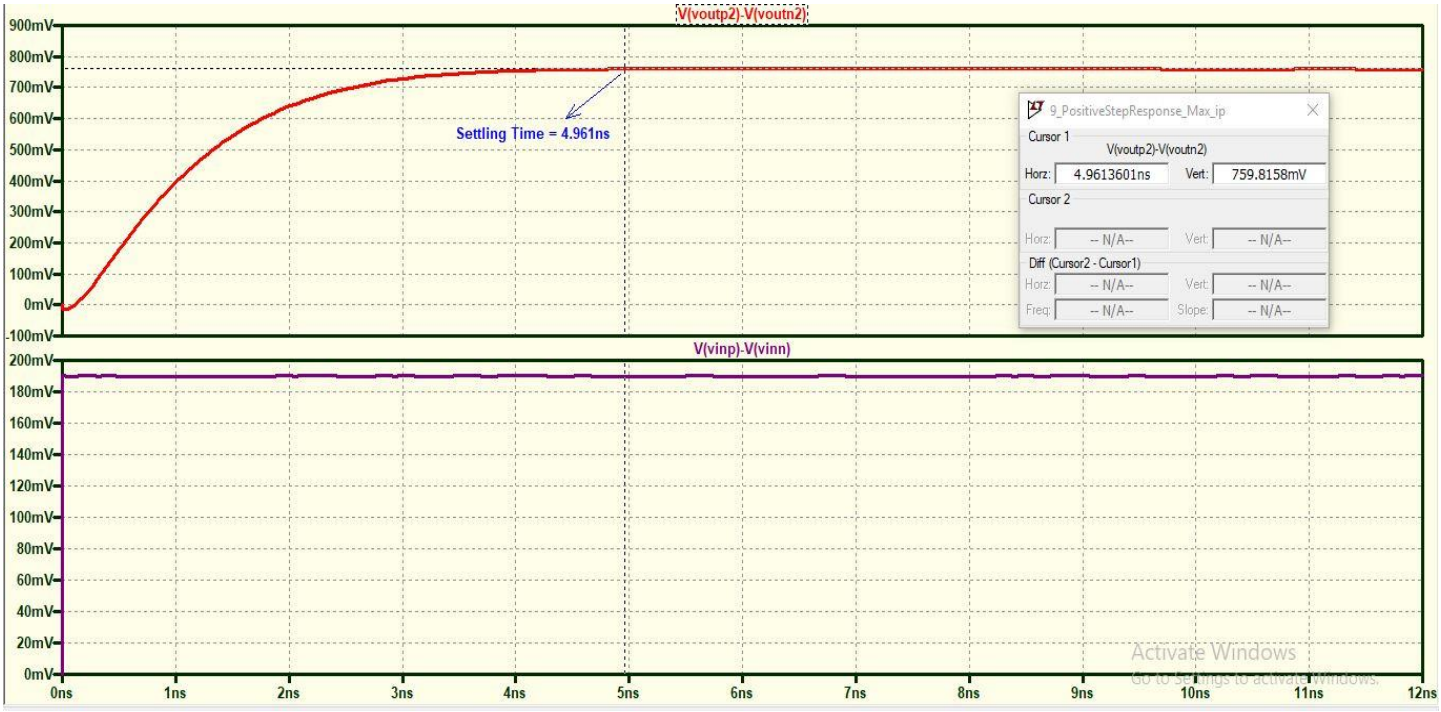


: DC Gain & Loop BW

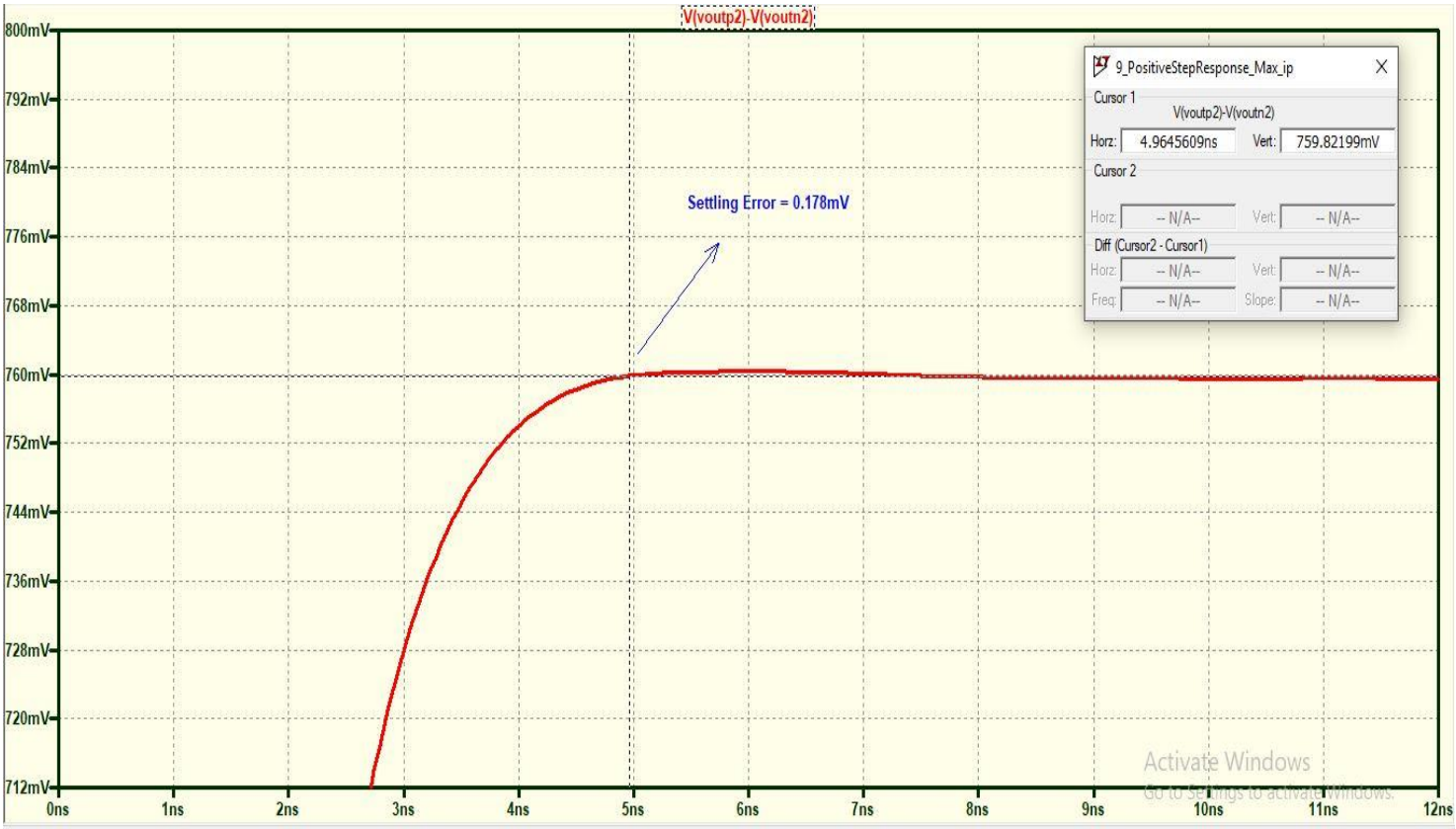


: Phase Margin & Gain Margin

d. Positive Step Response

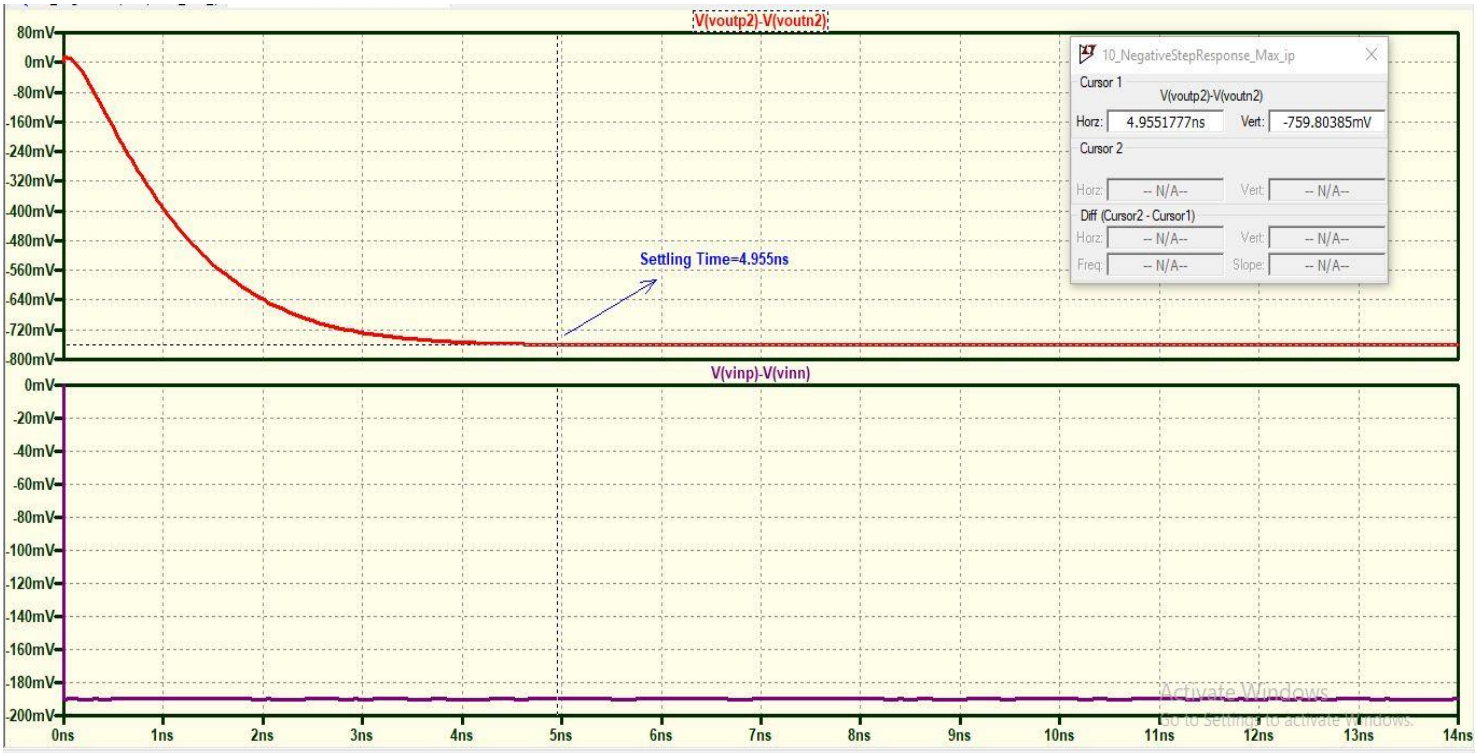


: Settling Time Plot

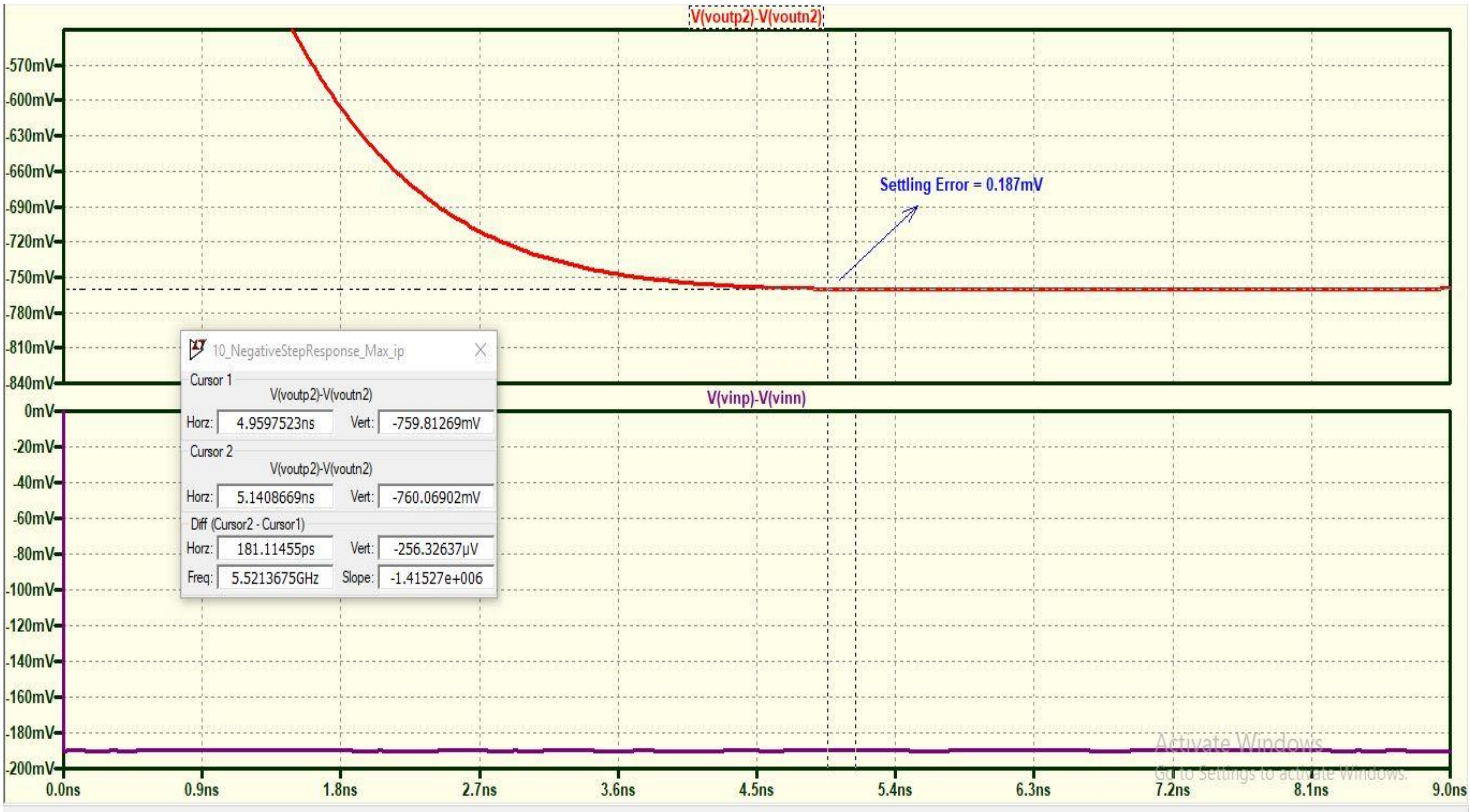


: Settling Error Plot

e. Negative Step Response

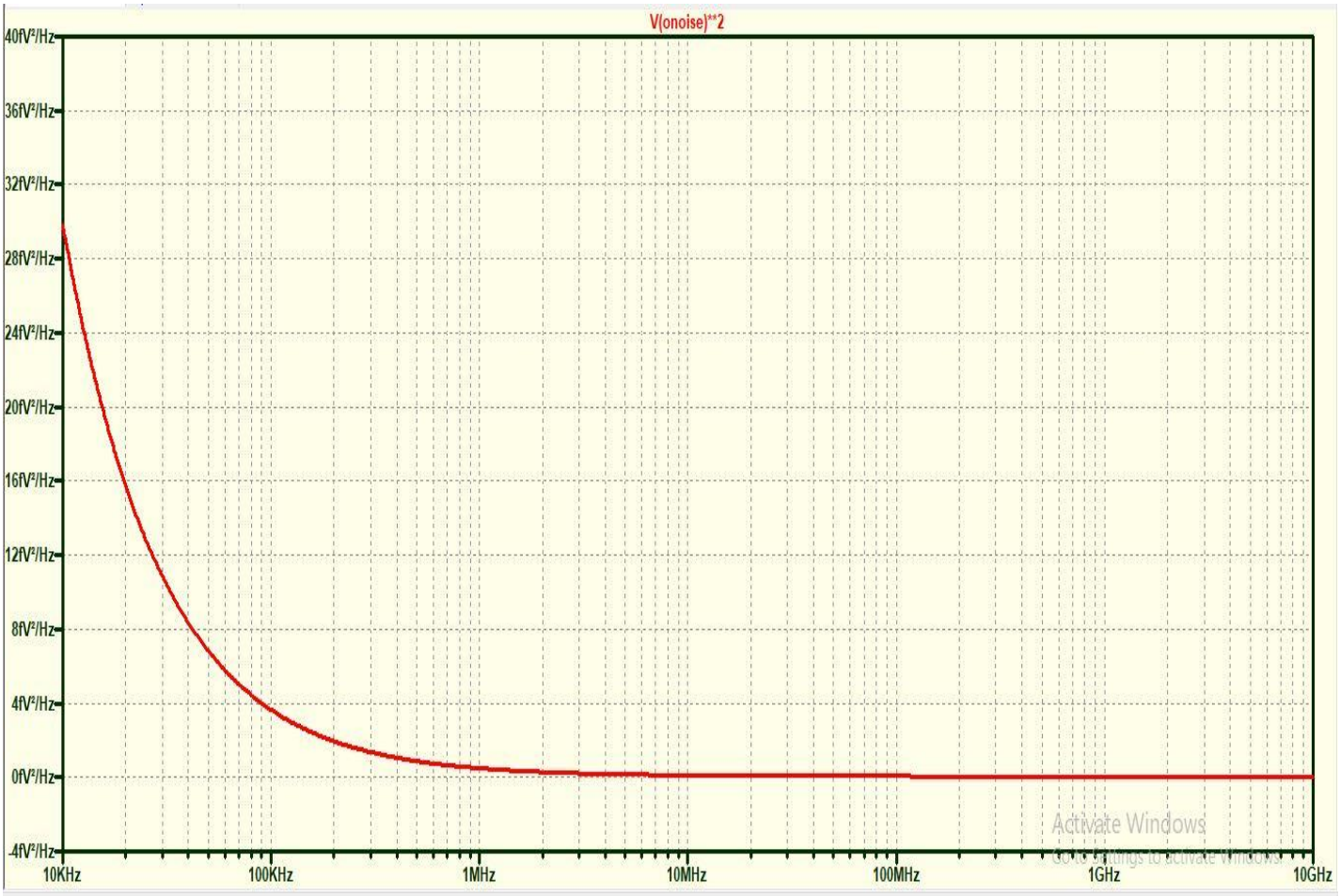


: Settling Time Plot



: Settling Error Plot

f. Differential Output Noise v/s Frequency



: Output Noise PSD

```
Gmin stepping succeeded in finding the operating point.

integrated_differential_noise: INTEG(v(onoise)**2)=1.65505e-012 FROM 100000 TO 9.9999e+009
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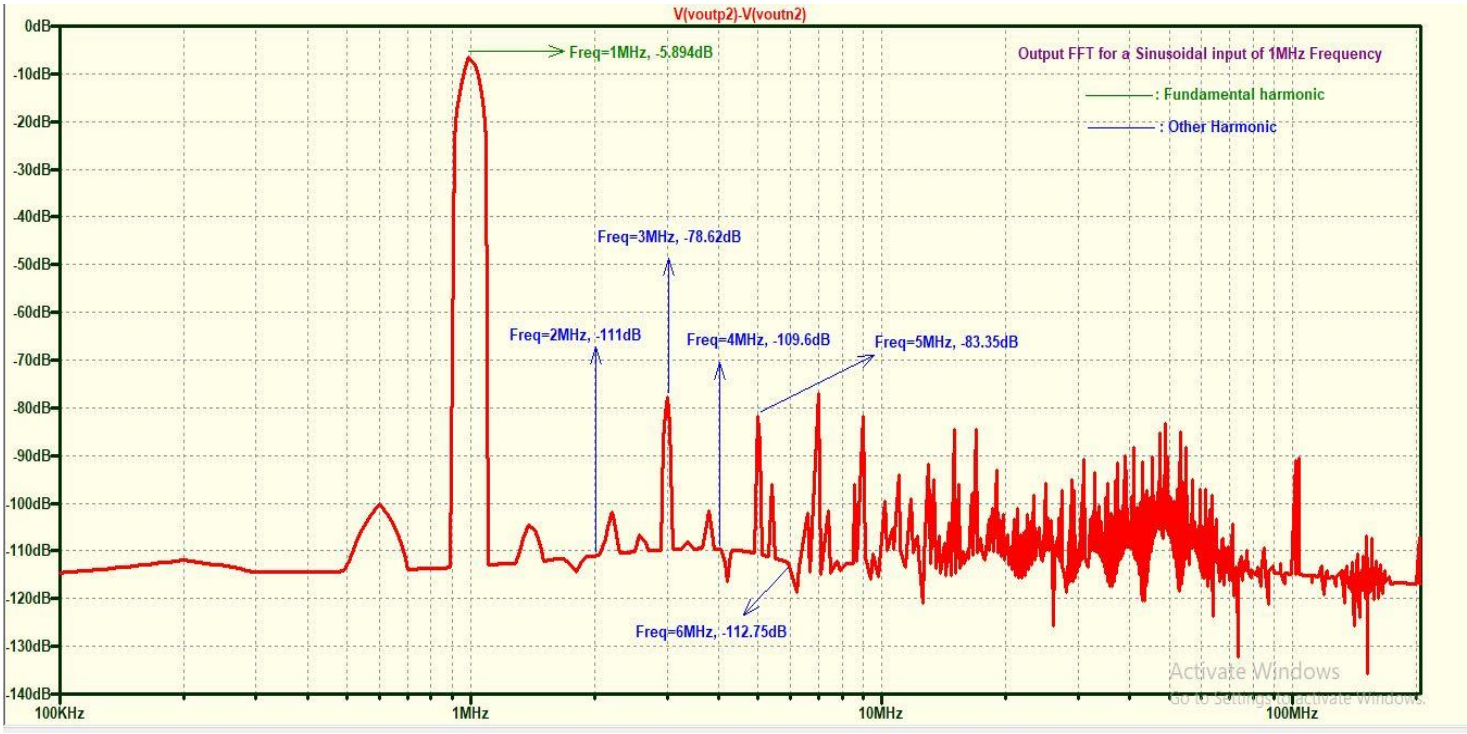
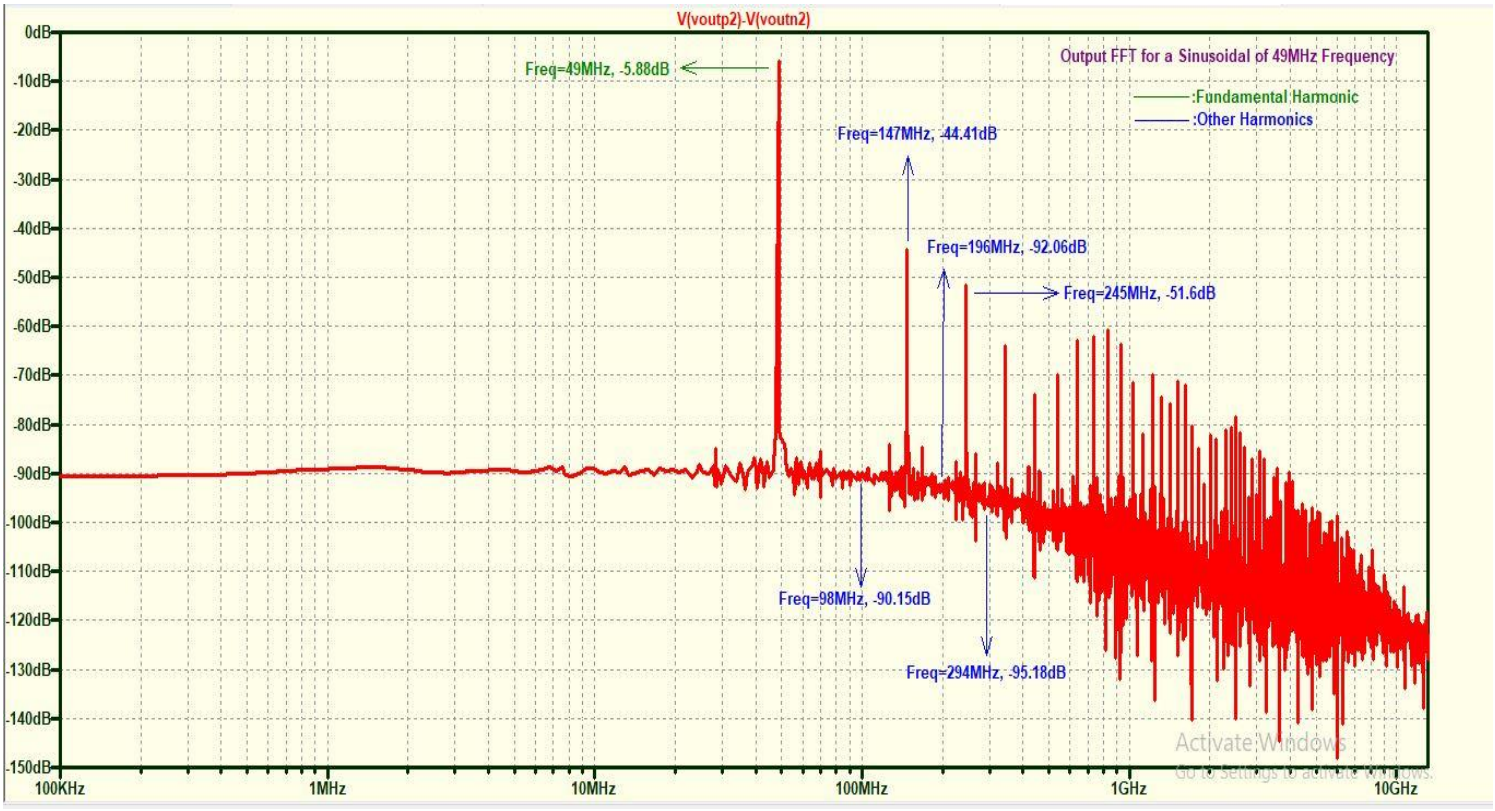
: Total Integrated Noise Power

g. Output FFT when Input sinusoid is applied

i. Sinusoidal Frequency = 1MHz

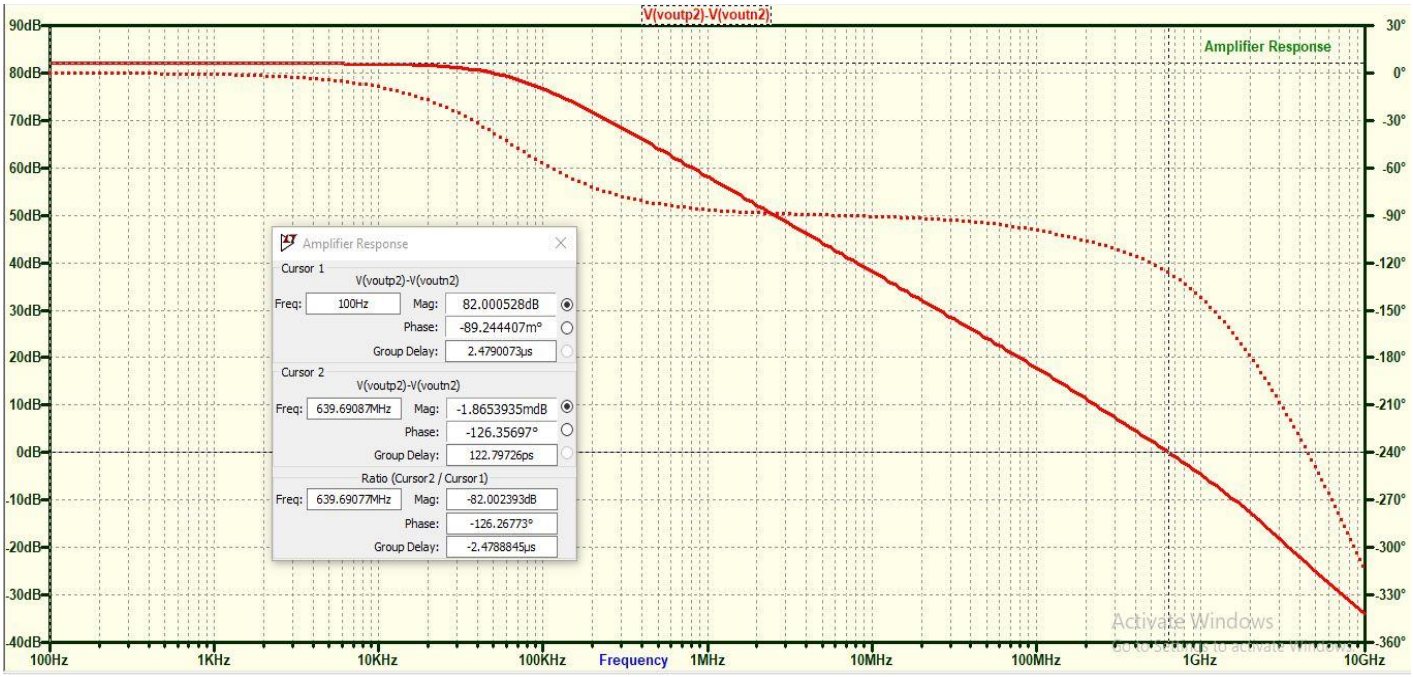


ii. Sinusoidal Frequency = 49MHz

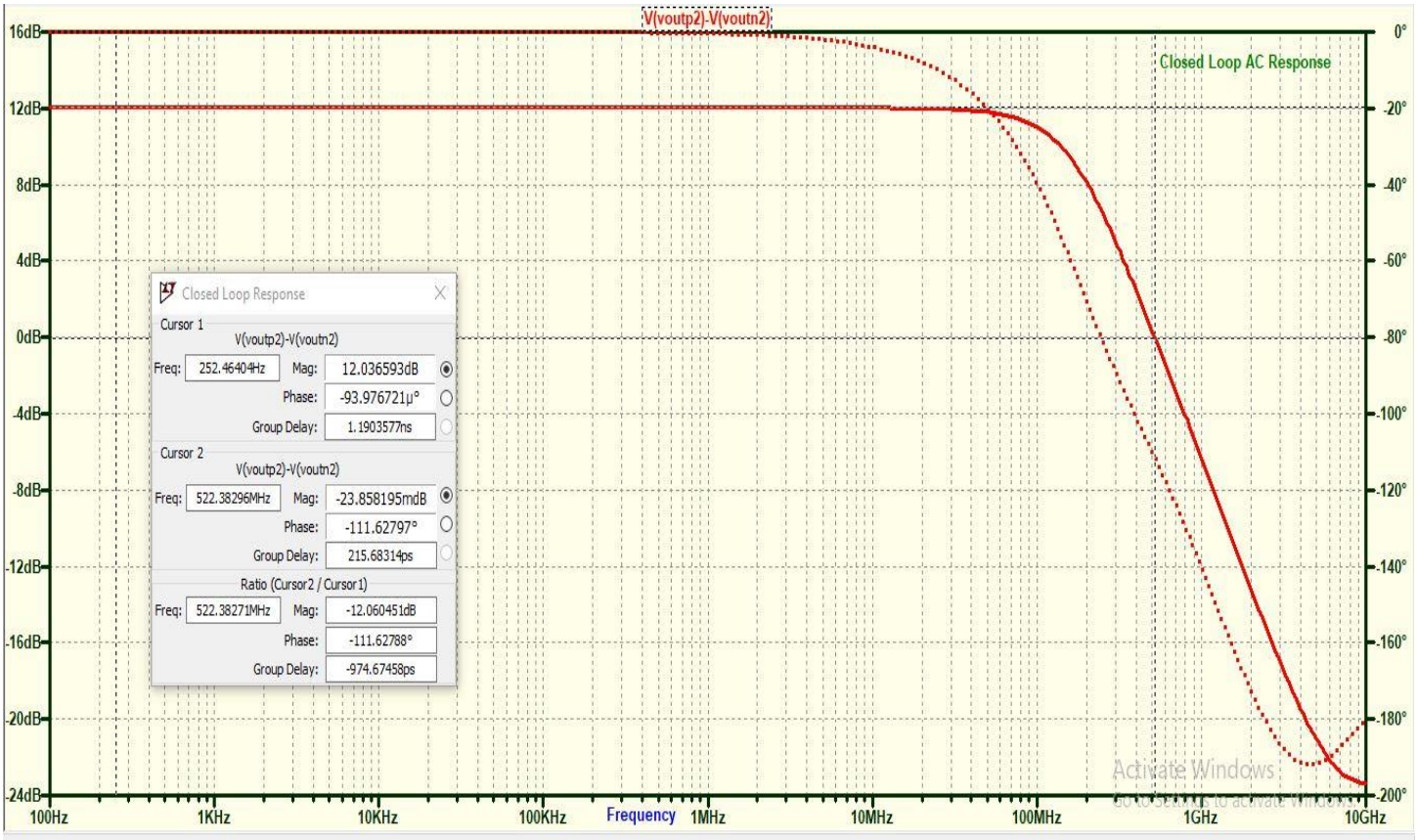


7) Subsidiary Results

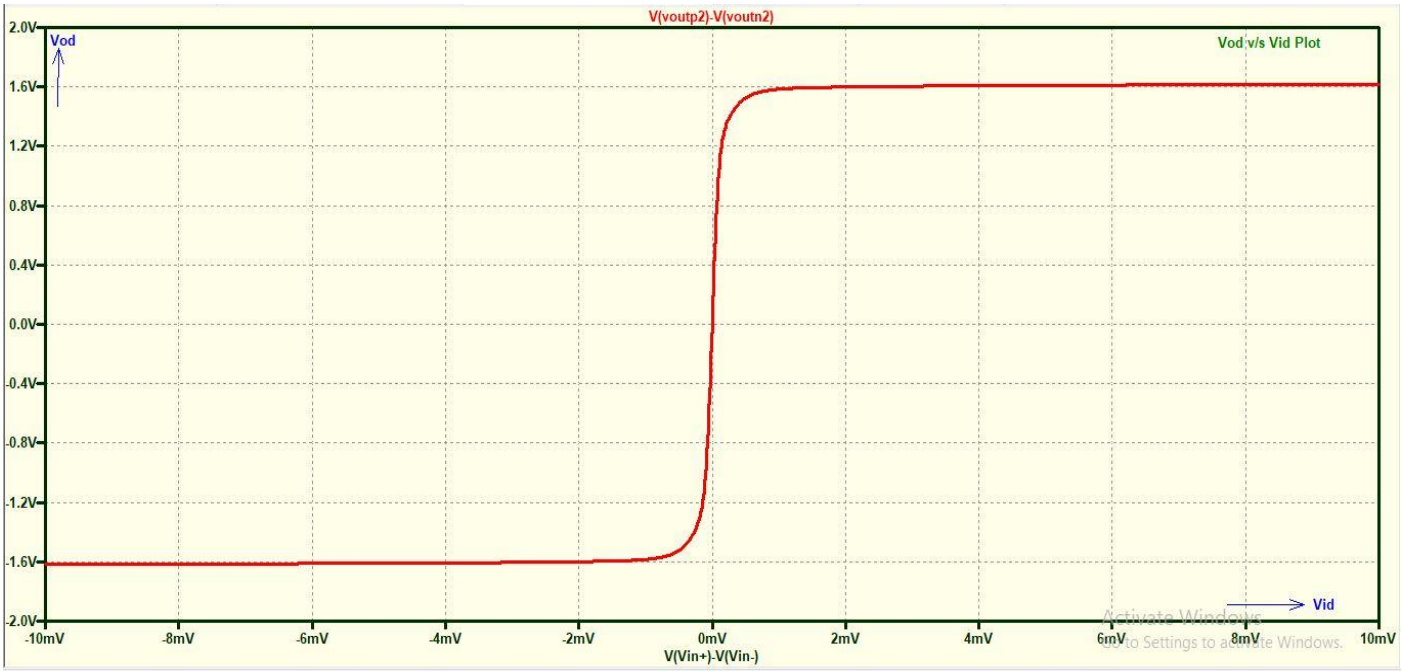
a. Open Loop Amplifier Response



b. Closed Loop Amplifier Response



c. Differential Output v/s Differential Output Plot



d. Power Consumption

I(Ibias):	0.0004945	device_current	⇨ Bias Current
I(R6):	0	device_current	
I(R5):	0	device_current	
I(R4):	6.58398e-015	device_current	
I(R3):	6.60117e-015	device_current	
I(R2):	0	device_current	
I(R1):	0	device_current	
I(V8):	0	device_current	
I(V7):	0	device_current	
I(V6):	0	device_current	
I(V5):	0	device_current	
I(V4):	0	device_current	
I(Vdd):	-0.091807	device_current	⇨ Total Current
I(V2):	0	device_current	
I(V1):	0	device_current	

8) References

[1] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, August 2000.

[2] *Analysis and design of Analog Integrated Circuits*, Gray, Hurst, Lewis, and Meyer, 4th Edition, John Wiley and Sons.