Differential LNA Design

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LNA Design Project Report

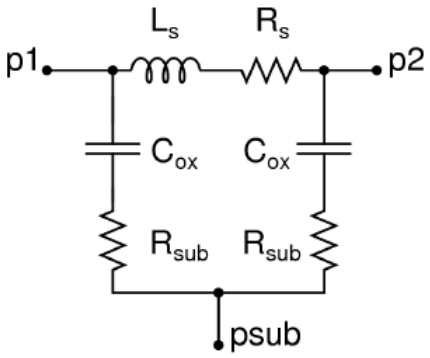
Introduction

This project consists of design and simulation (in cadence spectre) of a Pseudo Differential Amplifier which works in the frequency range of 2.3GHz to 2.6GHz. The other specifications desired for the LNA is given below;

Specifications

- Differential R_{in} = 100Ω
- S11 < -10 dB for the frequency of operation
- Voltage Gain > 20dB for Differential load of 100fF
- Noise Figure ≤ 2dB
- IIP3 ≥ -10dBm for two tones separated by 1MHz
- Supply Voltage, VDD = 1.2V

The inductors used for design is the Pi model of the inductor given below;

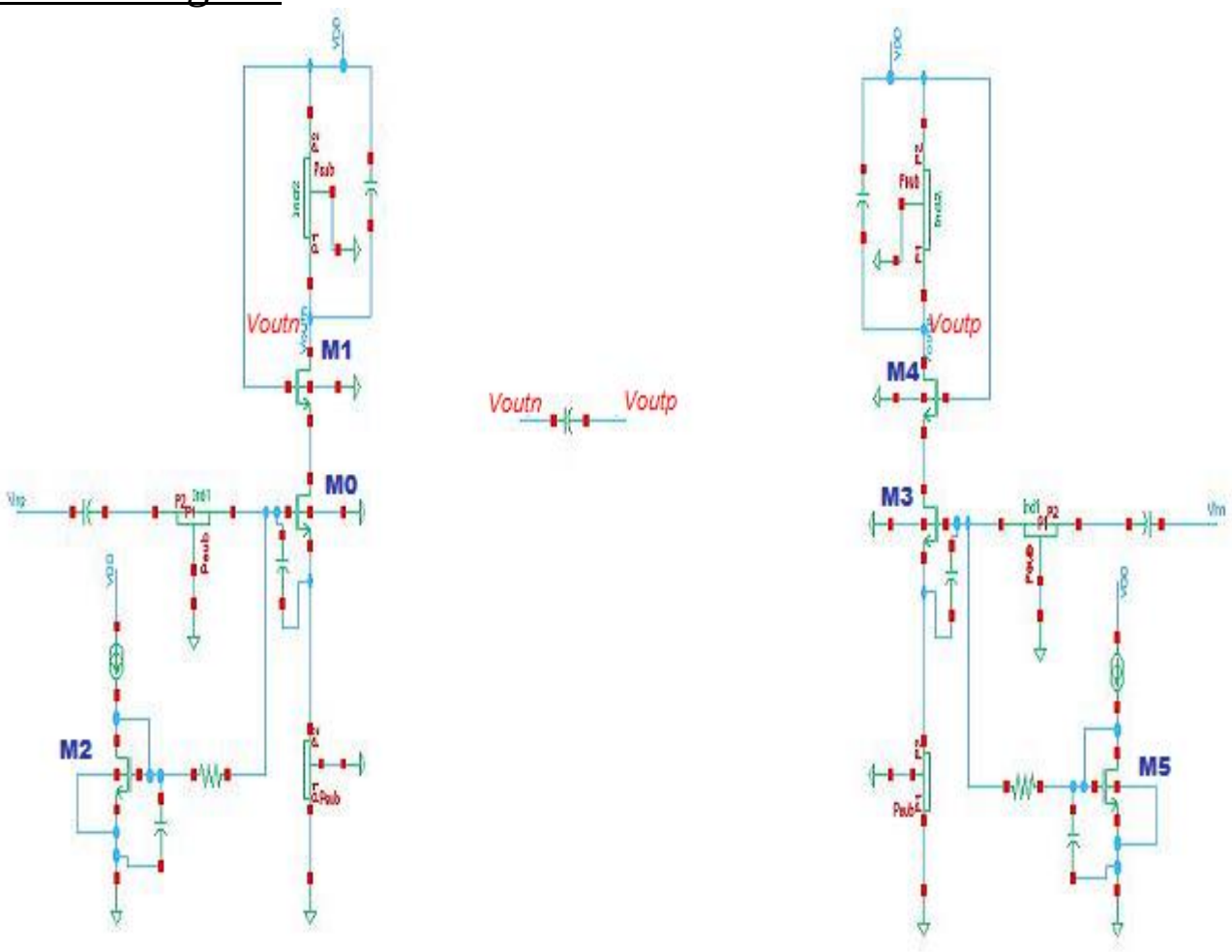


$R_s = 1.5e9 \cdot L_s$

$C_{ox} = -0.0005e6 \cdot L_s^2 + 0.0312e\text{-}3 \cdot L_s + 0.0543e\text{-}12$

$R_{sub} = 0.0789e18 \cdot L_s^2 + 31.7071 + 3.4892e\text{-}9/L_s$

Circuit Diagram



M0 and M3 are input transistors
M1 and M4 are cascade transistors
M2 and M5 are Bias transistors

Design

* Single sided input impedance, $Z_{in} = \frac{g_m L_s}{C_{gs}} + j\left(\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}\right)$

At resonant frequency ($f_0 = 2.45$ GHz); $Z_{in} = Z_0 = 50\,\Omega$

So $\frac{g_m L_s}{C_{gs}} = 50\,\Omega$ & $(L_g + L_s) \cdot C_{gs} = \frac{1}{\omega_0^2}$ ------①

Take $L_s = 4.4$ pH (This value is taken after two-three iterative comparison between hand designed and simulated component values which gives required Z_{in} and S_{11})

Angular transit frequency, $\omega_T = \frac{g_m}{C_{gs}} = \frac{50}{L_s} = 1.13636 \times 10^{12}$ rad/sec ----②

* Let Q_{ilp} be the quality factor of the series resonant circuit in the input loop.

Take $Q_{ilp} = 3.5$ (This value is taken based on the observation of peak (V_{gs0}/V_{in}) ratio during the simulations which gives required Z_{in} and S_{11}).

Input Quality factor, $Q_{ilp} = \frac{\omega_0(L_s + L_g)}{R_s} \longrightarrow L_g = \left\{\frac{Q_{ilp} \cdot R_s}{\omega_0} - L_s\right\}$

$= 11.561$ nH

* We have to connect a parallel capacitor across the Gate to source terminals of transistors (input transistors) M0 and M3, so that the resonant frequency can be set around 2.45 GHz even without taking very high W and L values for input transistors (ie M0 and M3).

Let $C_{gs} = (C_{gs})_{para} + (C_{gs})_{ext}$

$(C_{gs})_{para}$: Parasitic capacitance of MOSFET

$(C_{gs})_{ext}$: Externally connected parallel capacitor

$$C_{gs} = \frac{1}{\omega_0^2 (L_g + L_s)} = 378.94 \text{ fF}$$

* Calculation of widths of Bias transistors:

Take $I_{ref} = \frac{I_{D_0}}{10} \longrightarrow W_{bias} = \frac{W_0}{10} =$ "3.186 μm"

* Calculation of widths of Cascode Transistors:

The width of cascode transistors doesn't make much difference in Z_{in} and S_{11} but affects noise figure for lower values of cascode transistor widths (ie in 10^{-7}m range). The noise figure is not affected much if the width is in 10^{-5}m range.

Take "$W_1 = W_4 = 100\mu m$"

* Calculation of Q-factor of Inductor

Let Z_L be the impedance across the terminals of the inductor, then Quality factor (Q) is given by;

$$Q = \left|\frac{Im(Z_L)}{Re(Z_L)}\right| = \frac{1}{\omega C_{ox}(R_s + R_{sub})}$$

----> After neglecting some terms assuming inductance will be at the most of the order of 10^{-8} H.

Substituting the expressions of C_{ox}, R_s and R_{sub} in terms of L in the quality factor equation, we get;

$$\text{Quality factor, } Q = \frac{1}{4.8\pi \times 10^9 \times \left(46800L_s^2 + 1.07071\times10^{-3}L_s + 1.7217\times10^{-12}\right)} \quad \text{----(+)}$$

* For the inductance values;

$L_s = 44$ pH $\longrightarrow Q = 37.489$

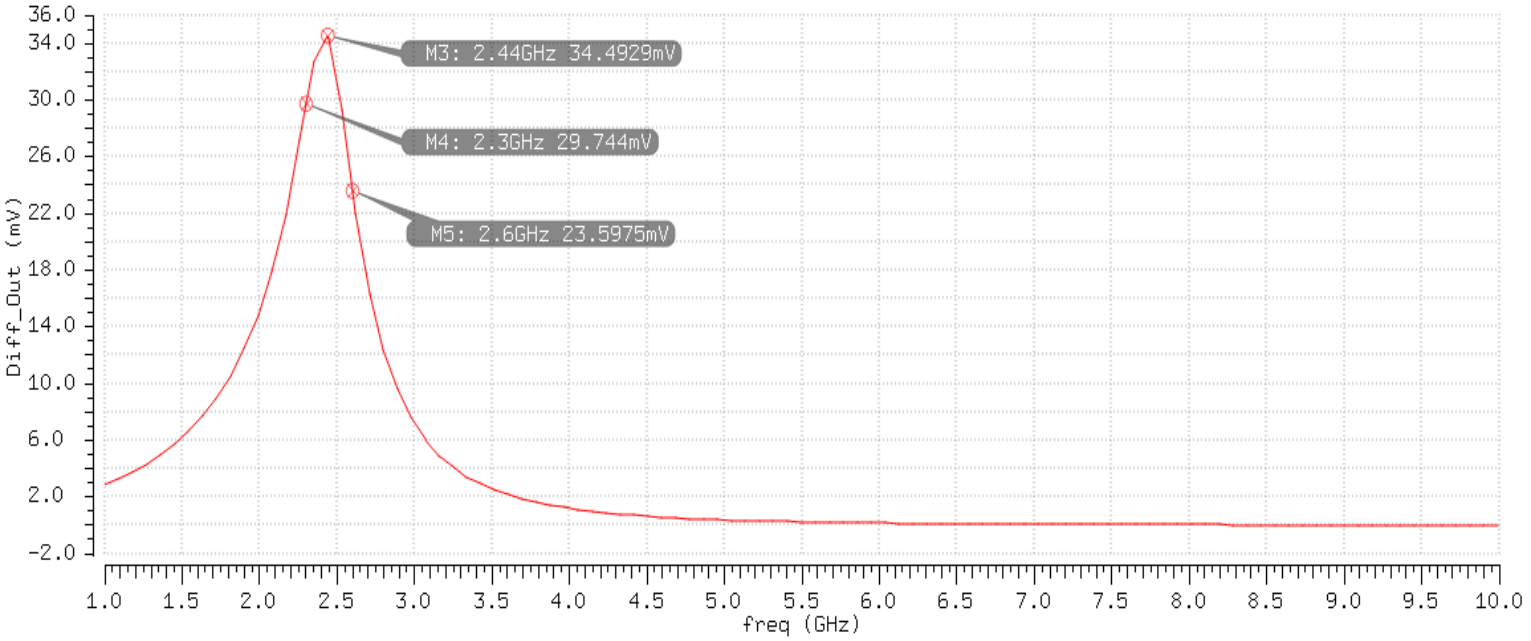
$L_d = 2.8$ nH $\longrightarrow Q = 13.037$

$L_g = 11.561$ nH $\longrightarrow Q = 3.2578 \longrightarrow$ L_g doesn't make much difference on the quality factor of output since L_d has higher Q-value

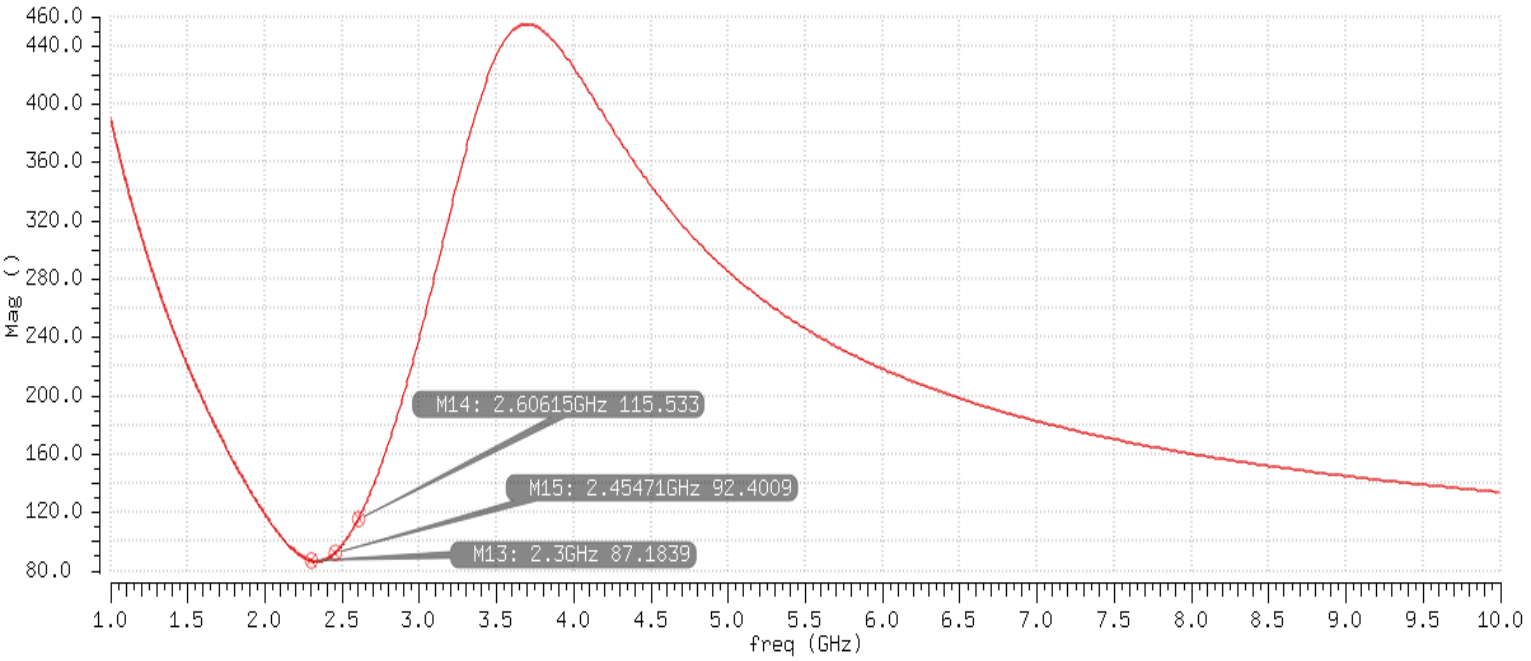
Main Results

1) Differential Output Voltage v/s Frequency Plot

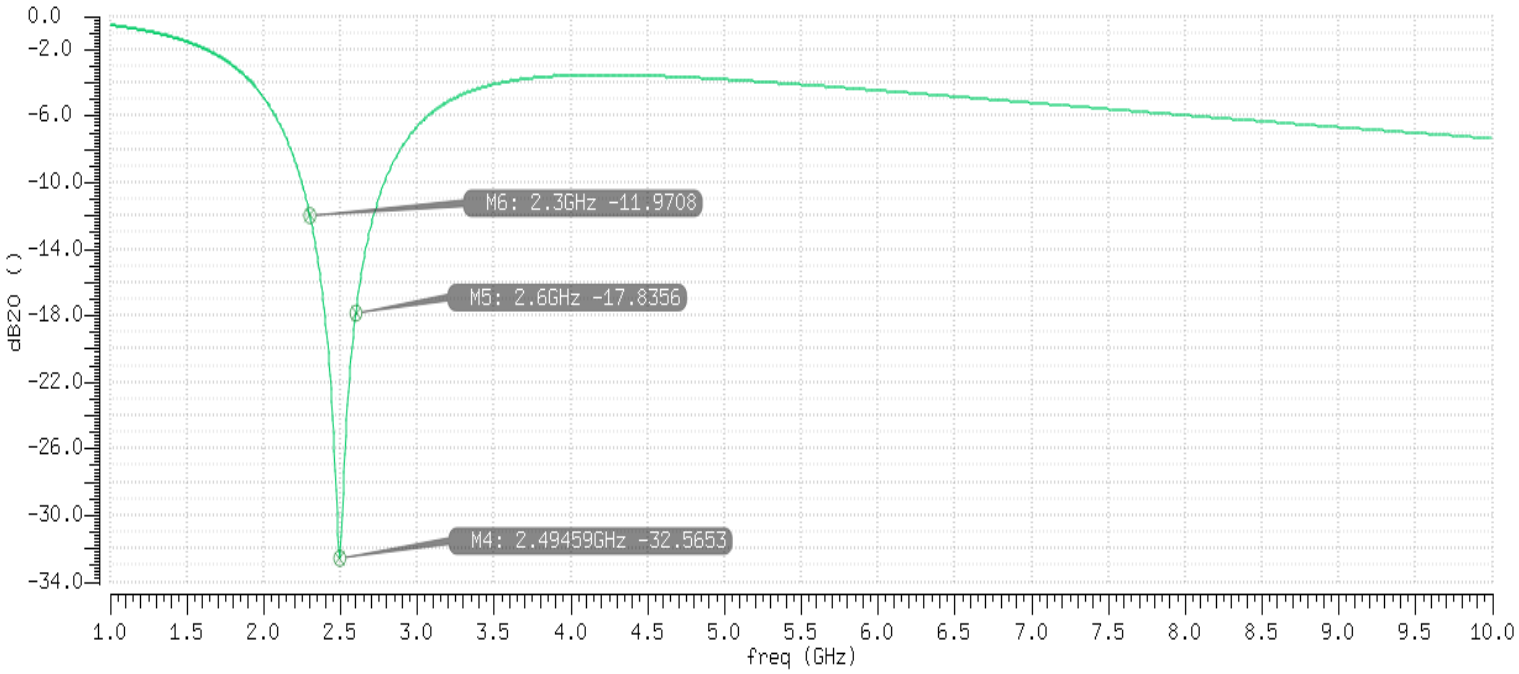
(For a differential input signal of 1mV)



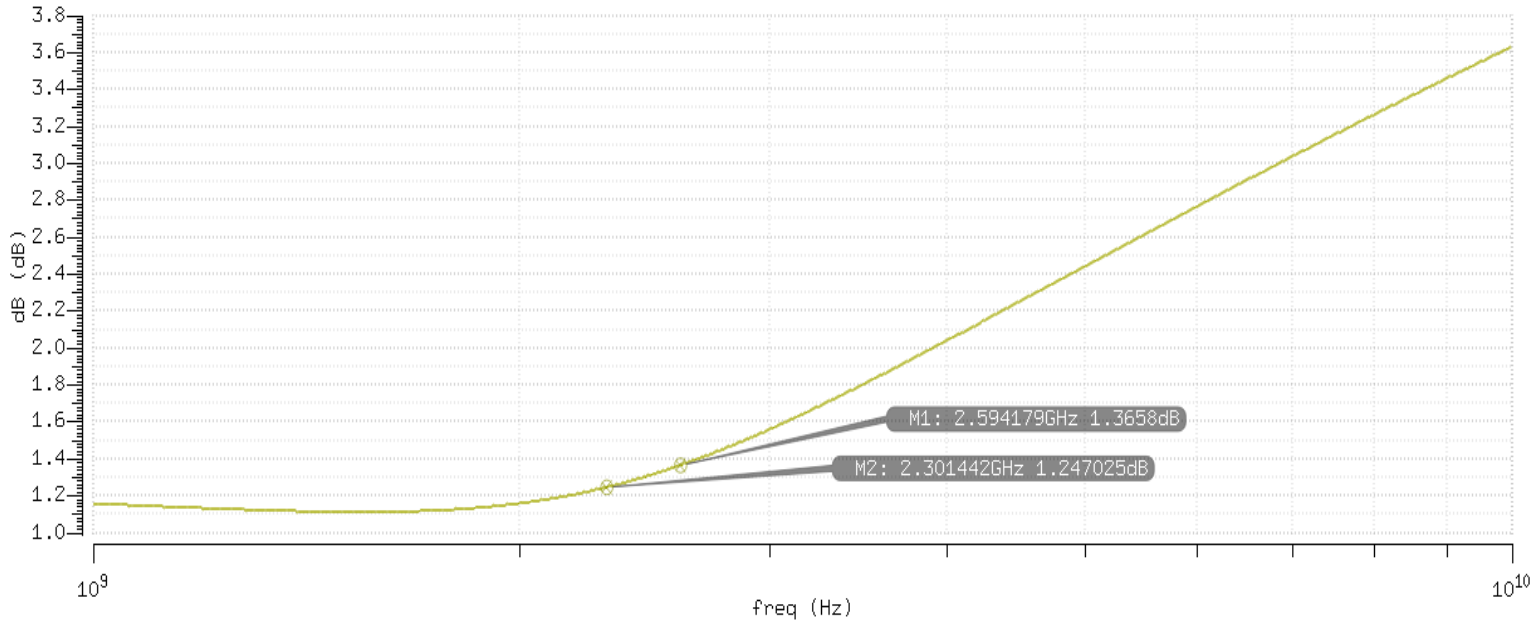
2) Differential Rin v/s Frequency Plot



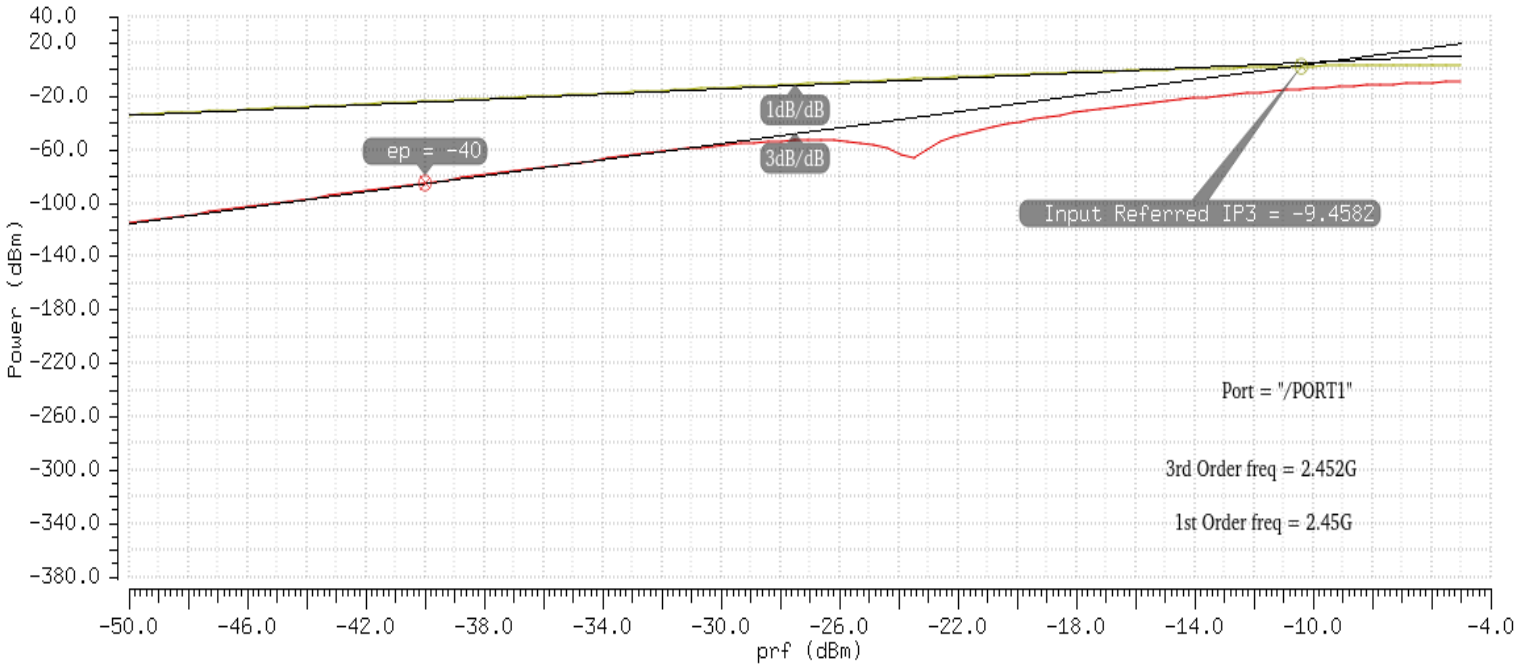
3) S11 v/s Frequency Plot



4) Noise Figure v/s Frequency Plot

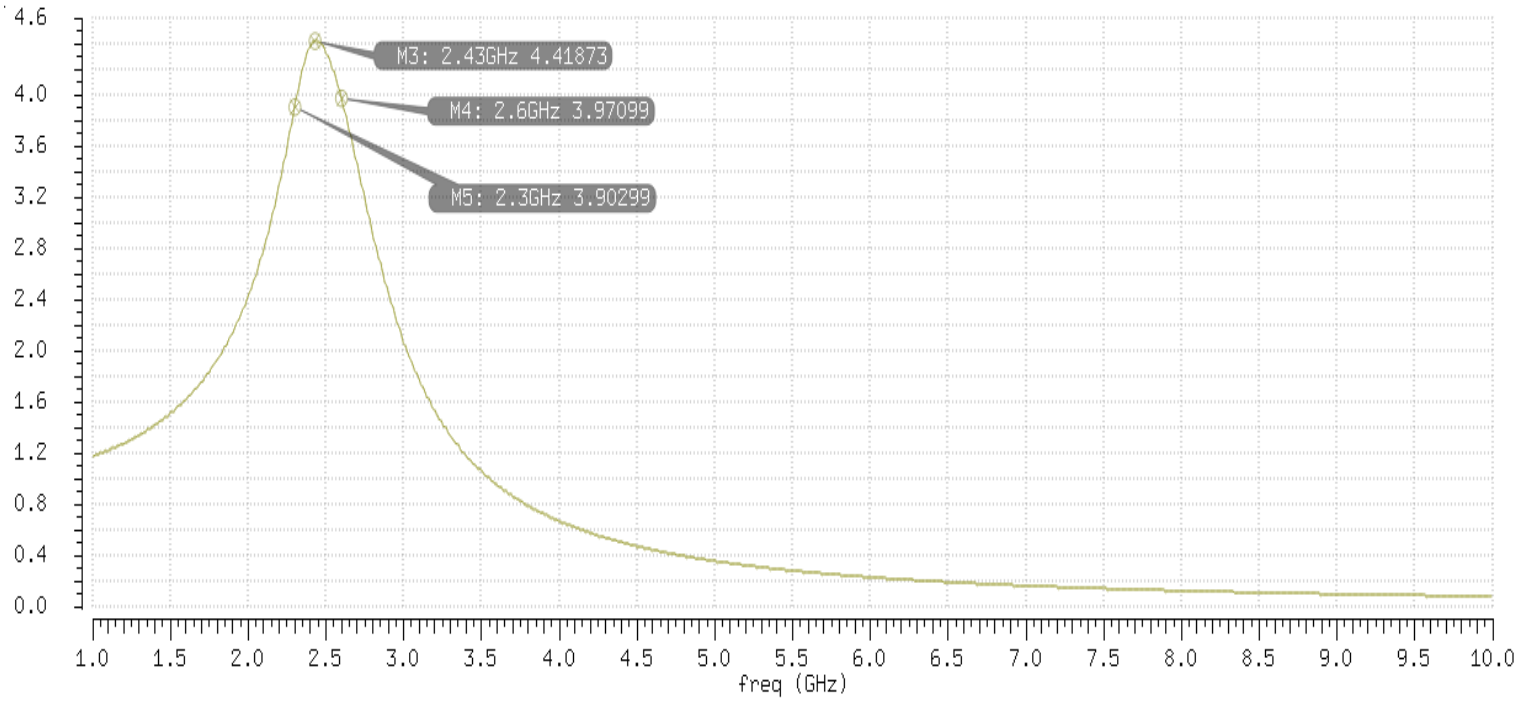


5) IIP3 Curve

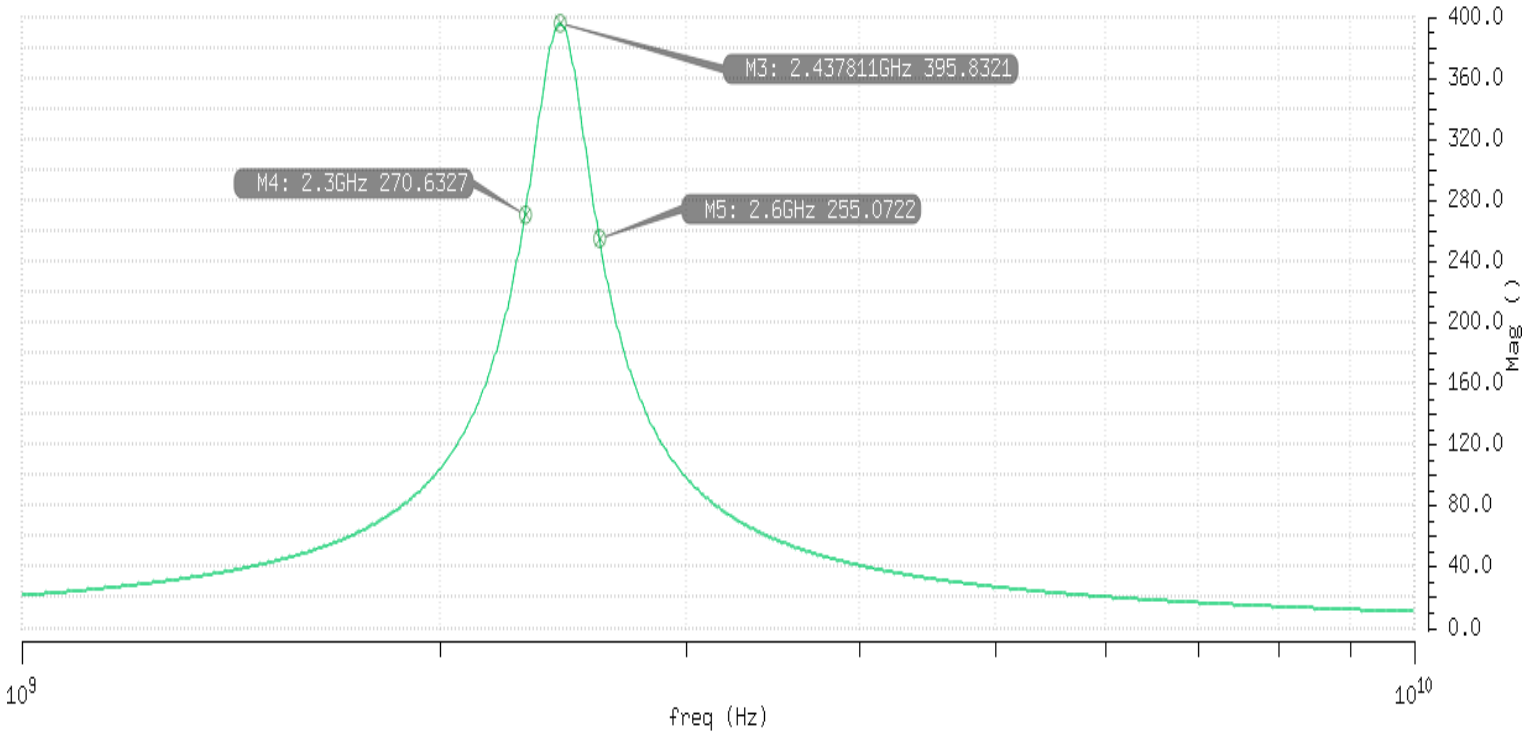


Subsidiary Results

1) (Vgs/Vin) of Input loop of one side v/s Frequency Plot



2) Output Impedance v/s Frequency Plot



Hand Designed v/s Simulated Values

Component Values		
Component Name	*Hand Designed Value*	*Simulated Value for Optimum result*
$(Cgs)_{ext}$	363fF	363fF
I_{bias}	1.867mA	2mA
L_{drain}	2.8nH	2.8nH
C_{drain}	2.1pF	1.374pF
Lg	11.561nH	11.11nH
Ls	44pH	44.3pH
W_0 (i/p Transistor)	31.86µm	29.5µm
W_1 (Cascoded)	100µm	40µm

Specifications		
Specification	*Hand Designed Value*	*Simulated Value*
Frequency of Operation	2.3 to 2.6 GHz	2.3 to 2.6 GHz
Resonant Frequency	2.45GHz	2.43GHz
Voltage Gain	20 V/V	34.49 V/V
Differential R_{in} (at Resonance)	100Ω	92.4Ω
S11 (at Resonance)	≤ -10dB	-32.56dB
Noise Figure (at Resonance)	0.00313dB	1.306dB

Circuit Parameters		
Parameter	*Hand Designed Value*	*Simulated Value*
g_m	17.405 mA/V	34.146 mA/V
C_{gs}	15.94 fF	30.91fF
V_{ov}	0.219 V	0.361 V
R_{out}	335.238 Ω	395.832 Ω
$Q_{i/p}$	3.5	4.4187

References

[1] RF Microelectronics, 2nd Edition by Behzad Razavi, Prentice Hall Publications

[2] http://www.odyseus.nildram.co.uk/RFIC_Circuits_Files/MOS_Diff_LNA.pdf
MOS Differential LNA Design Tutorial by J P Silvester

[3]https://pdfs.semanticscholar.org/3ed5/1a3d53e798d618b5792dbdd00aa976fd34c2.pdf
Design of A Low Power CMOS Differen tial Low Noise Amplifier by Using Die-Level EM analysis: Huseyin S. Savci, Numan S. Dogan, Zhijan Xie and Ercument Arvas