LC VCO Design Project

Submitted by KASYAP V KARUN (EE17M038)

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1) Introduction

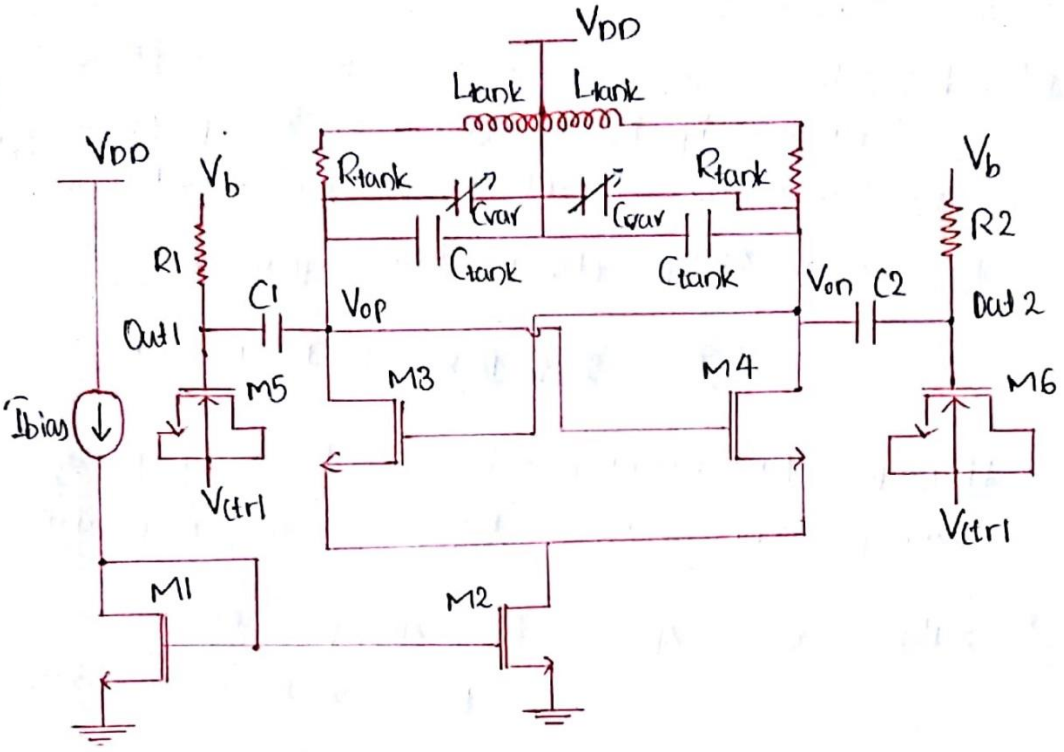
This project consists of design and simulation (in Eldo circuit simulator) of LC Voltage Controlled Oscillator (LC VCO) that generates for frequencies form 4.6GHz to 5.2GHz, realized by fine and course tuning in IBM 90nm technology. Design a VCO buffer also in order to produce 0 to V_{DD} swing across two single ended load capacitors of 100fF each. The other specifications of the VCO are given below;

Specifications:

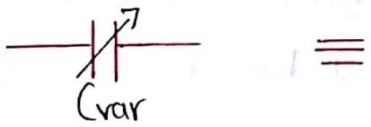
i) V_{DD} = 1.2V
ii) Frequency of Oscillation(f_{osc}) ranges from 4.6GHz to 5.2GHz
iii) Phase noise specification:
   a. -90dBc/Hz at f_{off} = 100kHz
   b. -135dBc/Hz at f_{off} = 20MHz
iv) Minimum VCO differential output amplitude = 0.8V
v) K_{VCO} = 50MHz/V for fine tuning
vi) Minimize Power dissipation

The LC VCO is expected to have a cross coupled pair of transistors and a resonance tank. There should be a current source either at the top or bottom of the LC VCO to provide enough drain current through the transistor. An NMOS in diode connected format (i.e. drain, source and bulk are tied together and gate acts as another terminal) is used for fine tuning of the capacitor value in the tank circuit at the drain of the cross coupled transistor pair. The course tuning of the oscillator is realized using a digitally controlled capacitor bank (refer the 2nd section of this document) and an ADC.

2) Circuit Diagram



M1 ⟶ Current mirror transistor
M2 ⟶ Bias bottom transistor
M3, M4 ⟶ Cross coupled transistors
M5, M6 ⟶ Acts as varactors for fine tuning



: Digital Capacitor Bank

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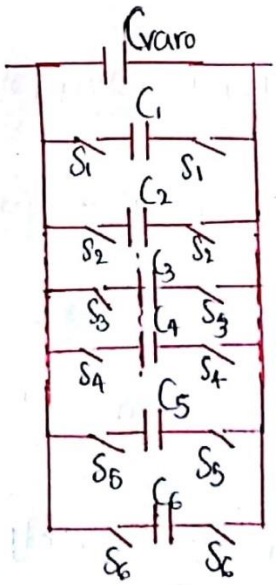
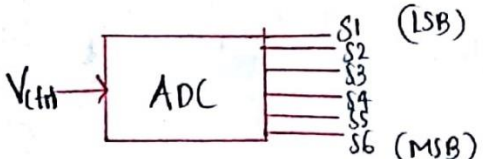




: 6-bit ADC

3) Hand Design

* Take $L_{tank} = 1nH$ ------ Assumption-①

We know that $\omega = 2\pi f = \frac{1}{\sqrt{LC}} \longrightarrow LC = L_{tank} \cdot C_{tank} = \frac{1}{4\pi^2 f^2}$ ----②

From assumption-① and ②;

$C_{tank} = 1.05pF$ ----③

Let R_{tank} be the equivalent series resistance of the inductor model given earlier; then $R_{tank} = 1.5\Omega$ (nearly) ----④

* Now apply KVL through one side of the LC VCO (ie through $V_{DD} \rightarrow L_{tank} \rightarrow R_{tank} \rightarrow M3 \rightarrow M2$), then

$$V_{DD} - I_{D3}R_{tank} - \{(V_{OS})_3 + (V_{DS})_2\} = 0$$

$$\Longrightarrow V_{DD} - 1.5I_{D3} - 2V_{ov} = 0 \quad \text{----⑤}$$

Since $V_{DD} = 1.2v$ & I_D is in mA range, $V_{ov} \approx \frac{V_{DD}}{2} = 0.6v$ ----⑥

* Output voltage swing, $V_{out} = \frac{4}{\pi} I_{Bias_{3,4}} \cdot R_{eq} \approx \frac{4}{\pi} \cdot I_{D_{3,4}} \cdot R_{tank}$

where R_{eq} is the equivalent resistance seen across the output terminals.

Since $V_{out} = 0.8v \longrightarrow I_{D_{3,4}} = 0.218mA = I_{D_3} = I_{D_4}$

Bias current through M2, $I_{D_2} = I_{D_3} + I_{D_4} = 0.436mA$

Take $(W/L)_2 = 10(W/L)_1 \longrightarrow I_{D_1} = I_{bias} = \frac{I_{D_2}}{10} = 43.6\mu A$ ----⑦

* From ⑥; take $V_{ov} = 0.55v = V_{DS2} = V_{DS3,4}$ ----> Assumption-②

- To find the width(W) of M2:

Take $V_{DS} = 0.55v$, $V_{th} = 220mV \longrightarrow V_{GS} = 0.7v$

Take $V_S = 0v \longrightarrow V_D = 0.55v$ & $V_G = 0.7v$ ---> for simulation purpose

On simulation; $W_2 = 132nm$ & $L_2 = 90nm$ ----> Design-①

- To find the width of (M3 & M4):

  Take $V_s = 0.55v$, $V_{th} = 340\,mV \longrightarrow V_D = 1.1v$ & $V_G = 1v$

  On simulation; $W_3 = W_4 = 7\mu m$ & $L_3 = L_4 = 290nm$ ----> Design-②

- From ⑦ and Design-①; $W_1 = 13.2\mu m$ & $L_1 = 90nm$ ---> Design-③

* Take $R1 = R2 = 500k\Omega$ & $C_1 = C_2 = 300fF$ ----> Connected to the gate terminal of M5 and M6 Design-④

  On simulation; $W5 = W6 = 32\mu m$ & $L_6 = L_5 = 90nm$ ----> Design-⑤

* Effective Cdrain of M3,4 , $C_{3,4} = C_{GS} + 4C_{GD} + C_{DB} + C_p + C_{var}$ (min to max) —⑧

  From simulation of M3 & M4;

  $C_{GS} = 141fF$, $C_{DB} = 19.29fF$, $C_{GD} = 2.98fF$ ---> Design-⑥

* From the simulation of M5 and M6 (in drain-source-body shorted configuration)

  - $C_{var} = 115fF$ when $V_{ctrl} = 0v$
  - $C_{var} = 87fF$ when $V_{ctrl} = 1v$ } ----⑨

  From ⑧, Design-⑥ and ⑨;

  Since $4.6GHz \le f_{osc} \le 5.2GHz \longrightarrow 0.937pF \le C_3 \le 1.199pF$ ---⑩

* From ⑨ and ⑩; $(C_3)_{max} - (C_3)_{min} = (C_{var})_{max} - (C_{var})_{min}$

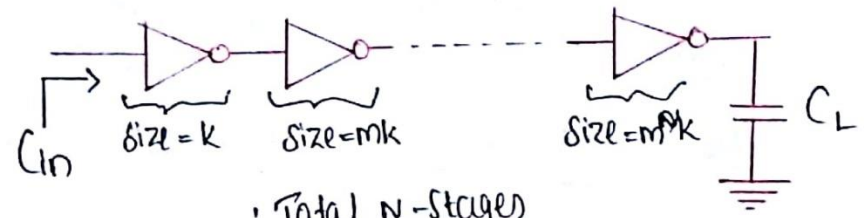
  So take $C_p = C_3 - [C_{GS} + 4C_{GD} + C_{DB} + C_{var}] = 649.79fF \approx 0.65pF$ --->Design⑦

* Hence from Design-①,②,③,④,⑤, ⑥ and ⑦;

Hand Designed Component Values

- $L_{tank} = 1nH$, $C_{tank} = 1.05\,pF$, $R_{tank} = 1.5\Omega$, $C_p = 0.65pF$
- $W_1 = 13.2\mu m$, $W_2 = 132\mu m$, $W_3 = W_4 = 7\mu m$, $W_5 = W_6 = 32\mu m$
- $L_1 = L_2 = L_5 = L_6 = 90nm$, $L_3 = L_4 = 290nm$
- $R1 = R2 = 500k\Omega$, $C1 = C2 = 300fF$ & $I_{bias} = 43.6\mu A$

* VCO Buffer Design:



: Total N-stages

Here $m = \left(\frac{C_L}{C_{in}}\right)^{1/N} \longrightarrow N = \frac{20\log\left(C_L/C_{in}\right)}{20\log(m)}$ **

On simulation; $C_{in} = 0.038fF$, $m \approx 2.616$, then $N = 7.85$

Take $N = 7$

Size of PMOS in 1st inverter stage $= \left(\frac{1.2\mu m}{90nm}\right) = \left(\frac{W_{p1}}{L_{p1}}\right)$

Size of NMOS in 1st inverter stage $= \left(\frac{0.6\mu m}{90nm}\right) = \left(\frac{W_{n1}}{L_{n1}}\right)$

Similarly;

Size of PMOS in 7th inverter stage $= \left(\frac{1.315mm}{90nm}\right)$

Size of NMOS in 7th inverter stage $= \left(\frac{65798\mu m}{90nm}\right)$

* Phase Noise Calculation:

Phase noise, $S(\Delta\omega) = \frac{\pi^2}{R_p} \cdot \frac{KT}{I_{D_2}^2} \cdot \left(\frac{3}{8}\gamma + 1\right) \cdot \frac{\omega_0^2}{4Q^2(\Delta\omega)^2}$

At $\Delta f = 100kHz \longrightarrow \Delta\omega = 200\pi$ krad/sec ; $S(\Delta\omega) = -90.7dBc/Hz$

At $\Delta f = 20MHz \longrightarrow \Delta\omega = 40\pi$ Mrad/sec ; $S(\Delta\omega) = -136.7dBc/Hz$

* Digitally controlled capacitor Bank Design:

$C_{var} = C_{varo} + (C_1 + C_2 + C_3 + C_4 + C_5 + C_6)$

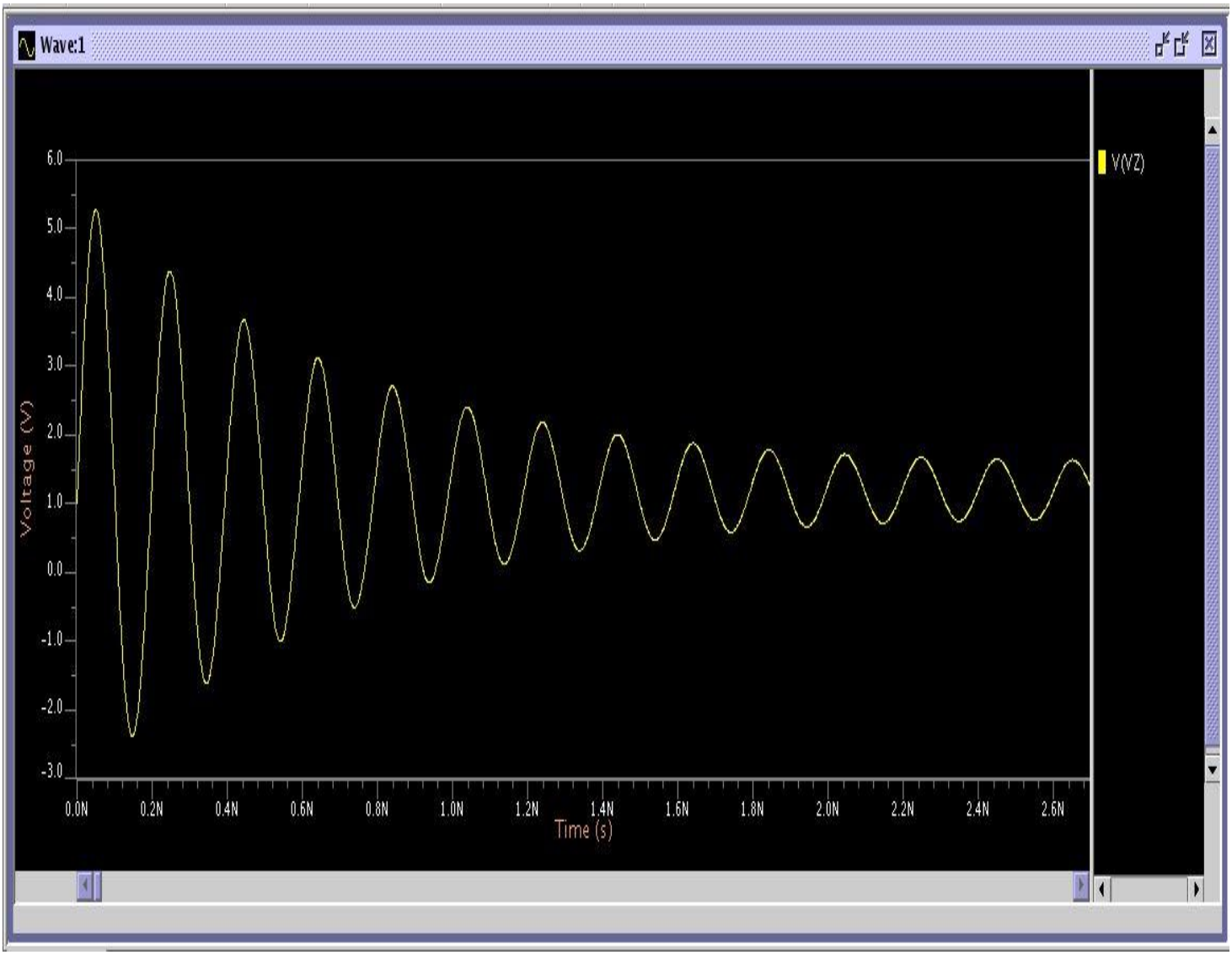
Take $C_{varo} = 80fF \longrightarrow 0 \le \left(\sum_{k=1}^{6} C_k\right) \le 63fF$

So "$80fF \le C_{var} \le 143fF$" but we need only 88fF to 115fF range

4) Results

a. Transient Response

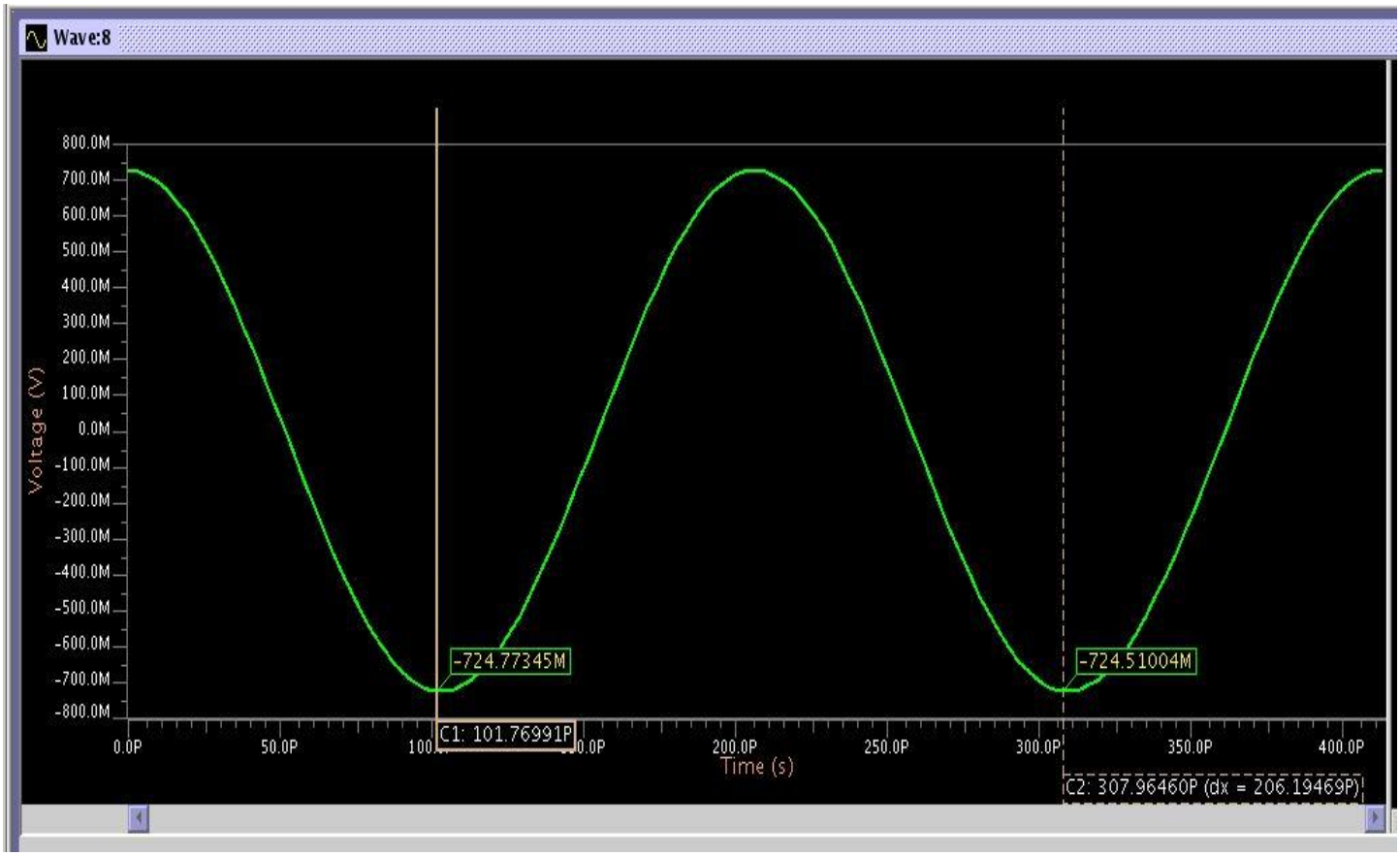
i. At the drain Node of M3 & M4



Initial Condition: V(Drain of M4) = 1V & V(Drain of M3) = 0V

The initial transient response of LC VCO (taken at the input of coupling capacitor at the drain of M4) is given above. It shows that the initial trans-conductance and hence the gain provided by the LC VCO to the drain voltages of M3 and M4 is high and it settles to a steady state value as time goes up. The DC bias point of output nodes are near to 1V since the drop across series resistance in the tank inductor is negligibly small.

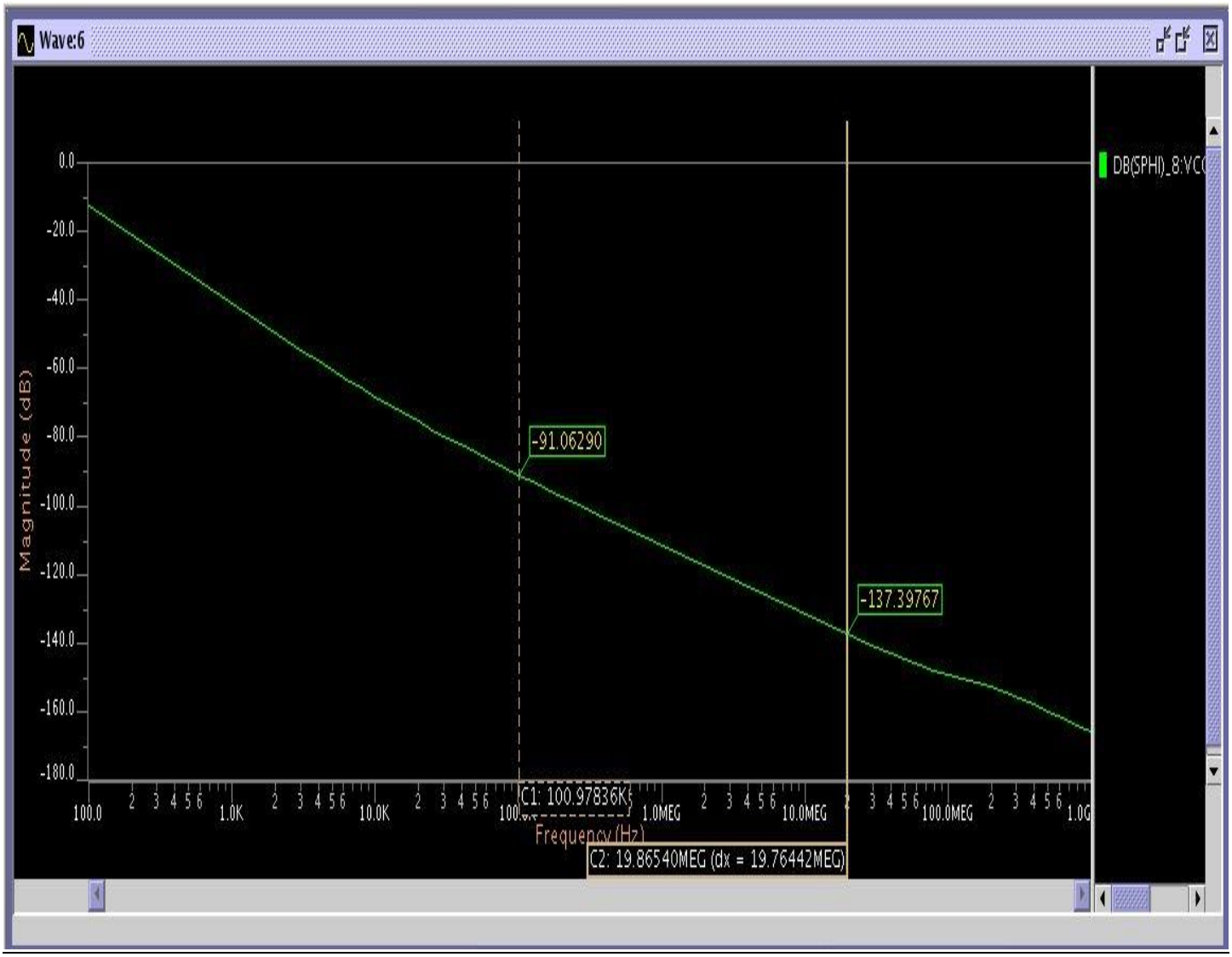
ii. <u>At the output of Coupling Capacitor</u>



Time Period of Oscillation = 206.1947ps
Frequency of Oscillation = 4.85GH
+ve Peak voltage of Signal = 724.773 mV
-ve Peak voltage of Signal = -724.773 mV

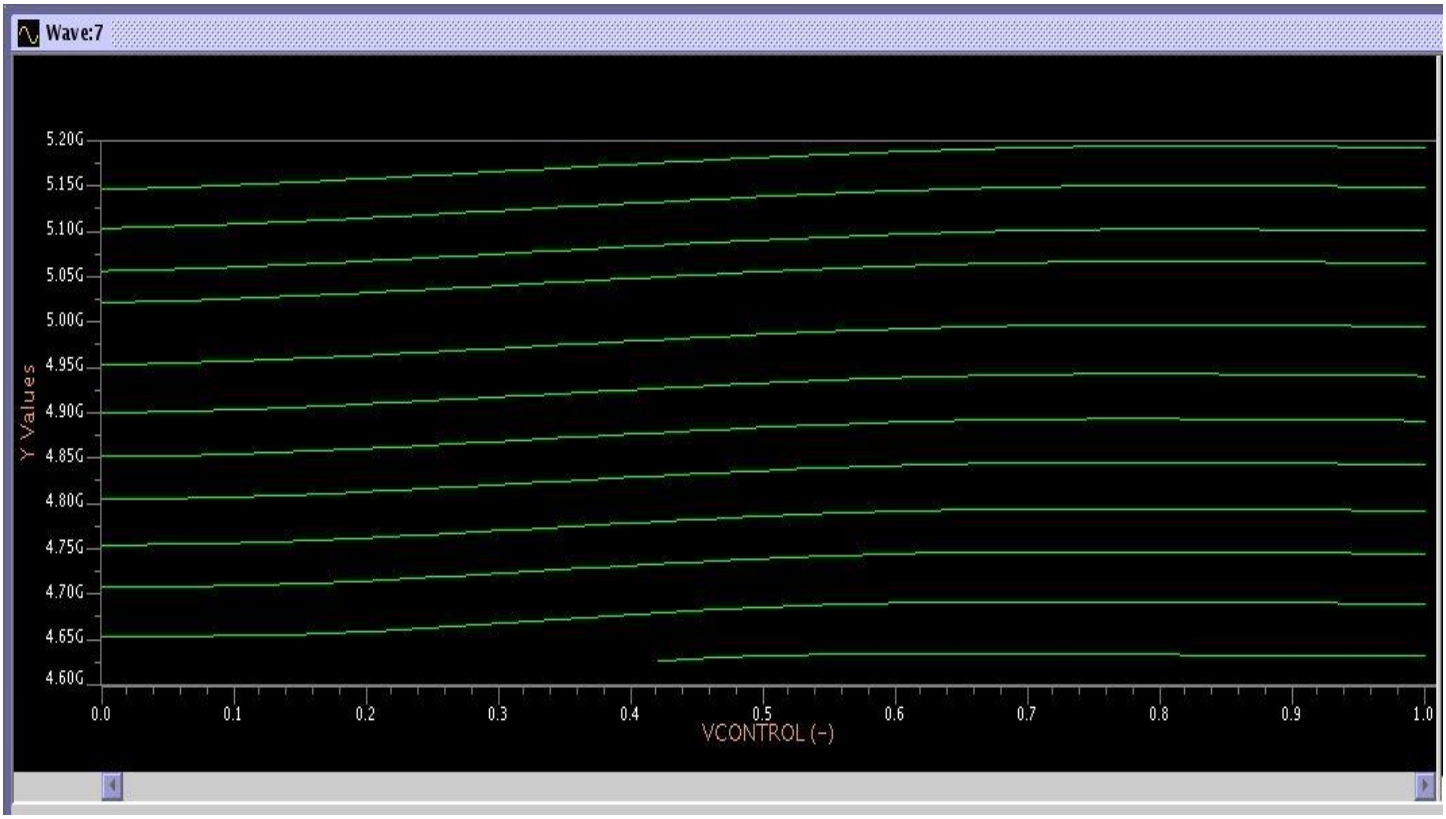
The output of coupling capacitor at the drain side of M4 is shown above. The DC bias signal is filtered off.

b. Phase Noise Plot



Phase noise at (Offset Frequency = 100 kHz) = -91.0629 dBc/Hz
Phase noise at (Offset Frequency = 100 kHz) = -137.398 dBc/Hz

c. Fosc v/s Vctrl plot for Course tuning

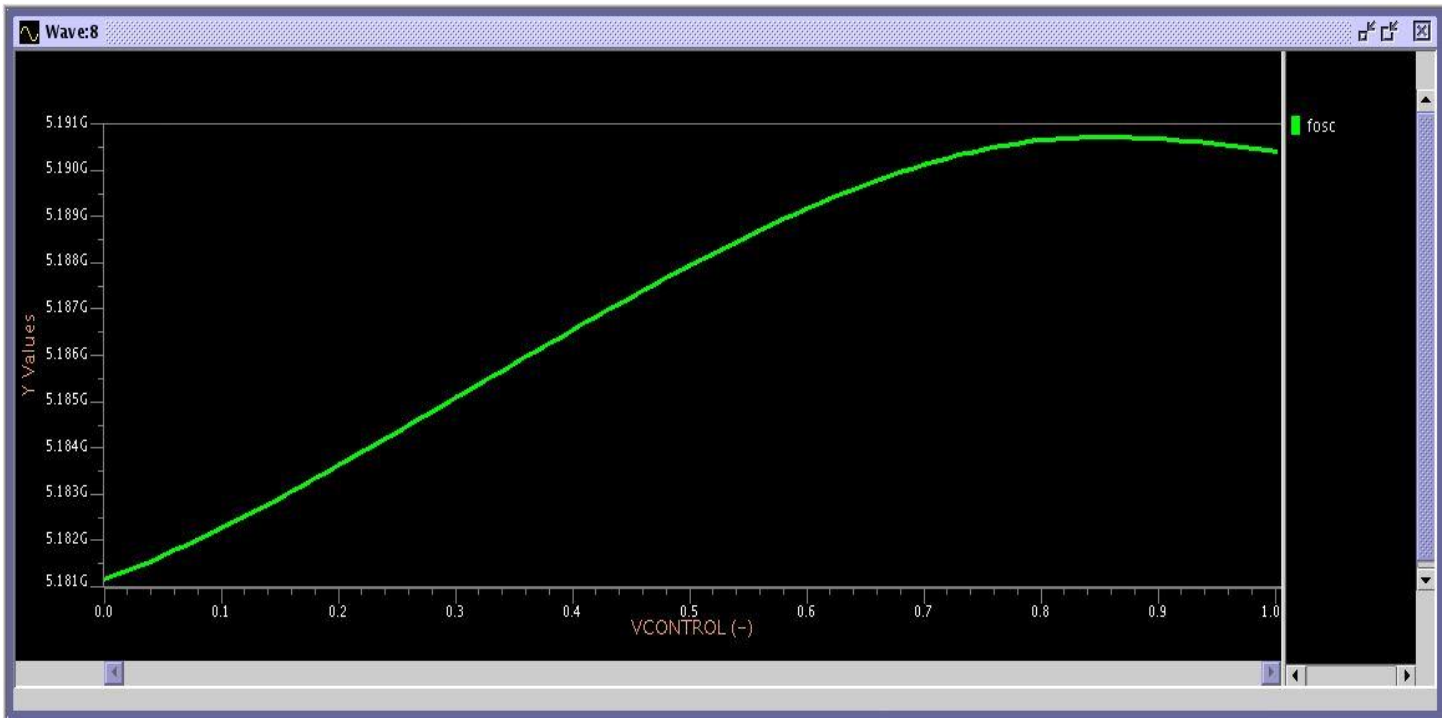


Minimum value of C_{var} = 115fF

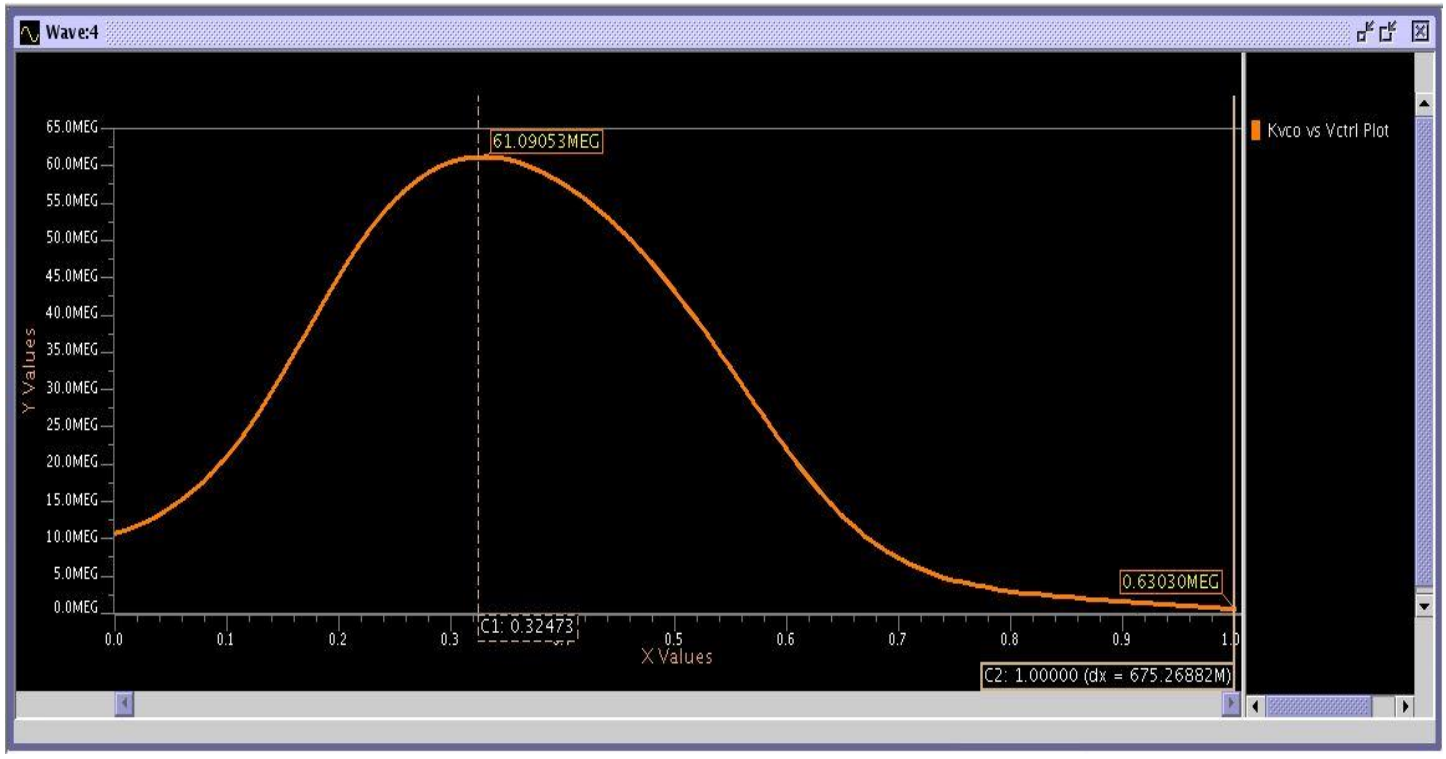
Maximum value of C_{var} = 87fF

The minimum value of Cvar gives the plot with highest frequency of oscillation and maximum value of Cvar gives the plot with least frequency of oscillation. The value of Cvar is varied using digitally controlled made of switched capacitors (C1 to C6 and Cvar) and 6-bit ADC (as shown in Circuit diagram given earlier in this document).

d. Fosc v/s Vctrl plot for Fine tuning

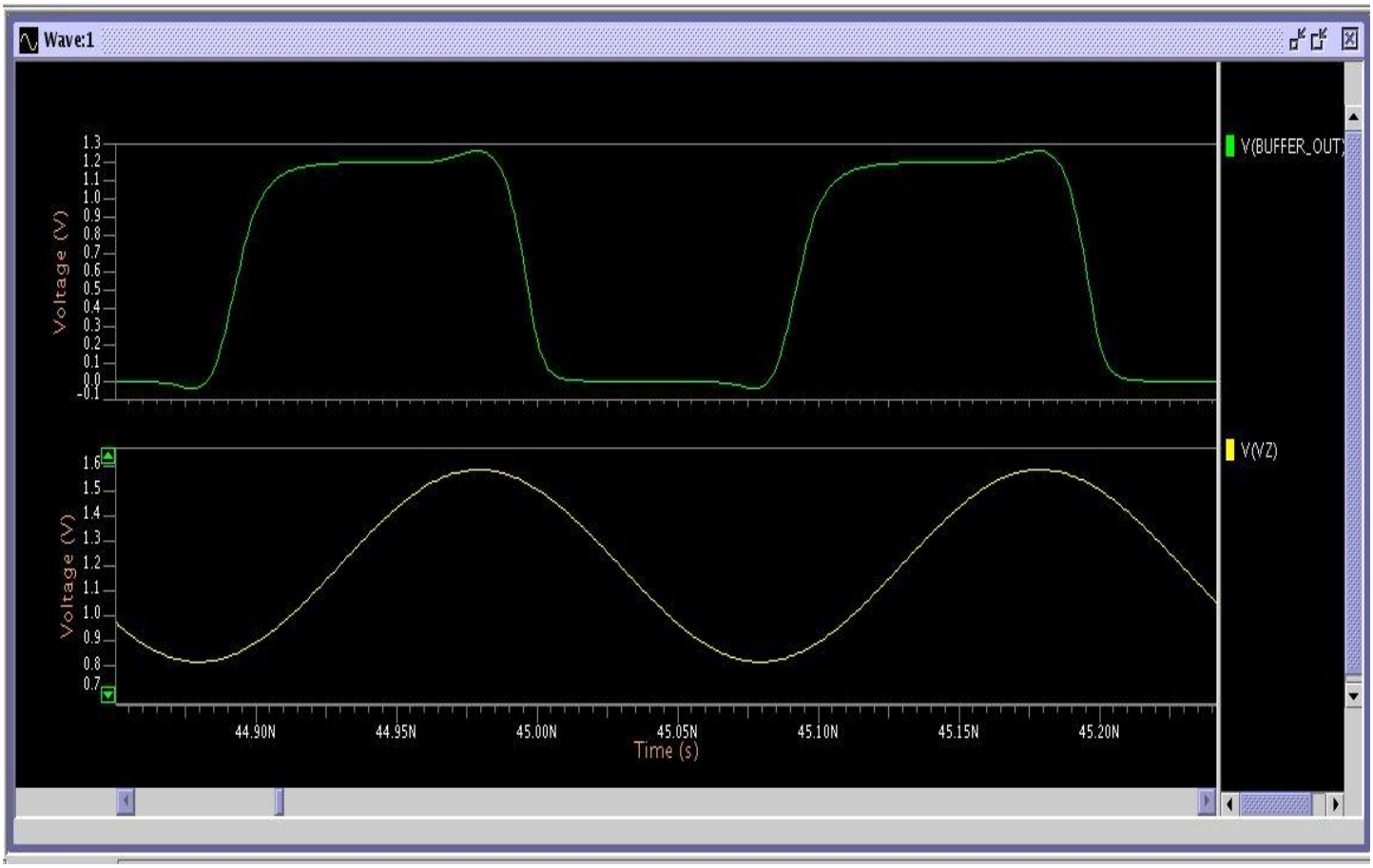


e. Kvco v/s Vctrl Plot



Maximum Value of K_{vco} = 61.09 MHz/V & Minimum Value of Kvco = 0.63 MHz/V

f. VCO Buffer Output



5) Comparison of Designed Parameters

Parameter	Designed Value	Final Value used
L_{tank}	1nH	1nH
C_{tank}	1.05pF	1.05pF
R_{tank}	1.5Ω	1.5Ω
(W1/L1)	(13.2µm/90nm)	(12µm/90nm)
(W2/L2)	(132µm/90nm)	(132µm/90nm)
(W3/L3) & (W4/L4)	(7µm/290nm)	(7.2µm/290nm)
(W5/L5) & (W6/L6)	(32µm/90nm)	(32µm/90nm)
R1 & R2	500kΩ	550kΩ
C1 & C2	300fF	300fF
I_{bias}	43.6µA	43.6µA

6) Comparison of Hand calculated and Simulated Results

Result	Hand Designed Value	Simulated Final Value
Frequency of Oscillation	4.6 to 5.2 GHz	4.6 to 5.2 GHz
VCO Differential Amplitude	≥0.8V	1.454V
Phase Noise	-90.7dBc/Hz at F_{off}=100kHz	-91.06dBc/Hz at F_{off}=100kHz
	-136.7dBc/Hz at F_{off}=20MHz	-137.4dBc/Hz at F_{off}=20MHz
Kvco	50MHz/V	59MHz/V
Number of Inverters in Buffer	7	7
Power Dissipation	575.52µW	576.39µW

7) References

[1] RF Microelectronics, 2nd Edition by Behzad Razavi, Prentice Hall Publications

[2] A 5 GHz LC-VCO with Active Common Mode Feedback Circuit in Sub-micrometer CMOS technology https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=0ahUKEwjBju7LncfaAhUBNY8KHaxOBtcQFggoMAA&url=http%3A%2F%2Fdigital.csic.es%2Fbitstream%2F10261%2F96022%2F1%2FA%25205%2520GHz%2520LC.pdf&usg=AOvVaw0W7ymEYAf-Tovkz0LAXm-a