
ITC Project REPORT

Kasyap V Karun
B130241EC
Christy George
B120885EC

Date : 20/06/14

ITC Project Report

AIM

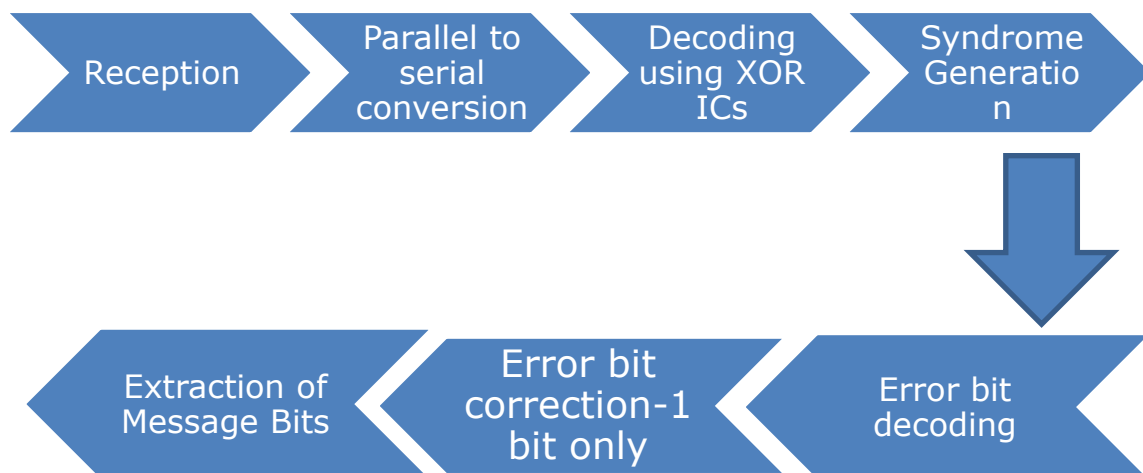
It is desired to generate the decoder and encoder circuitry for hamming code or (7, 4, 1) BCH code.

Block Diagram

Encoder



Decoder



Components Used

- XOR Gate IC – 74HC86
- Parallel to Serial Conversion IC – 74HC165
- Parallel to Serial Conversion IC – 74LS595
- LEDs - High Brightness
- Breadboard
- Connecting Wires

Theory

Hamming code generates 7 bit code words from 4 input message bits. We used systematic generator matrix in which four out of seven transmitted bits are message bits and the other three bits are parity bits. The generator matrix is given below;

The parity check matrix is used for generating 3 bit syndrome at the receiver side. The parity check matrix is given by;

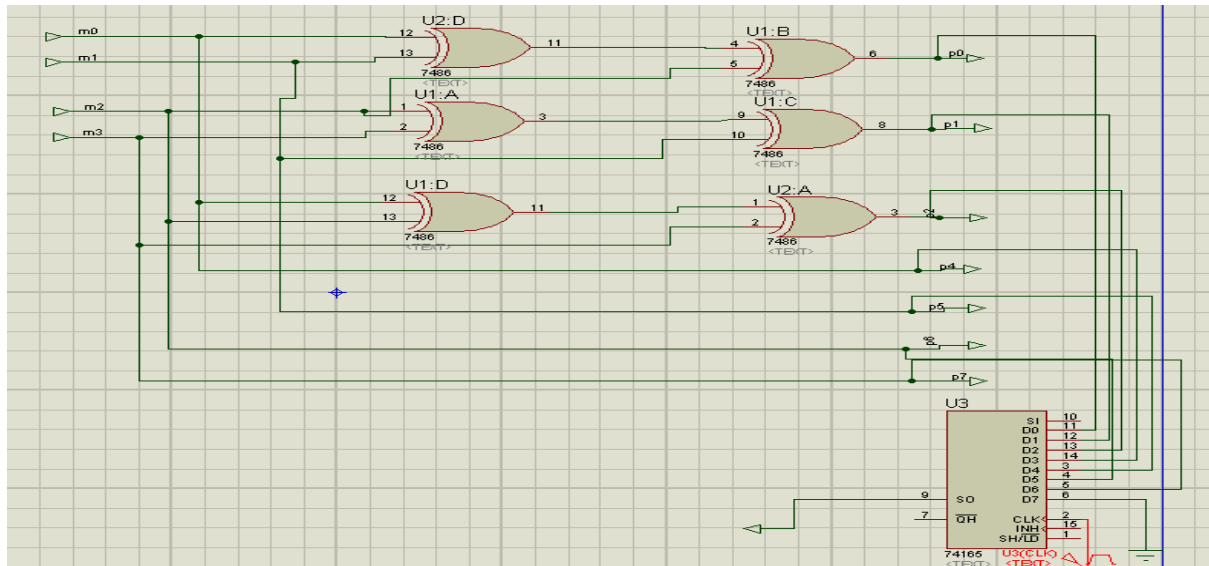
$$H = \left[\begin{array}{cccc|ccc} 1 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{array} \right]$$

Each syndrome denotes error in corresponding bits in received sequence;

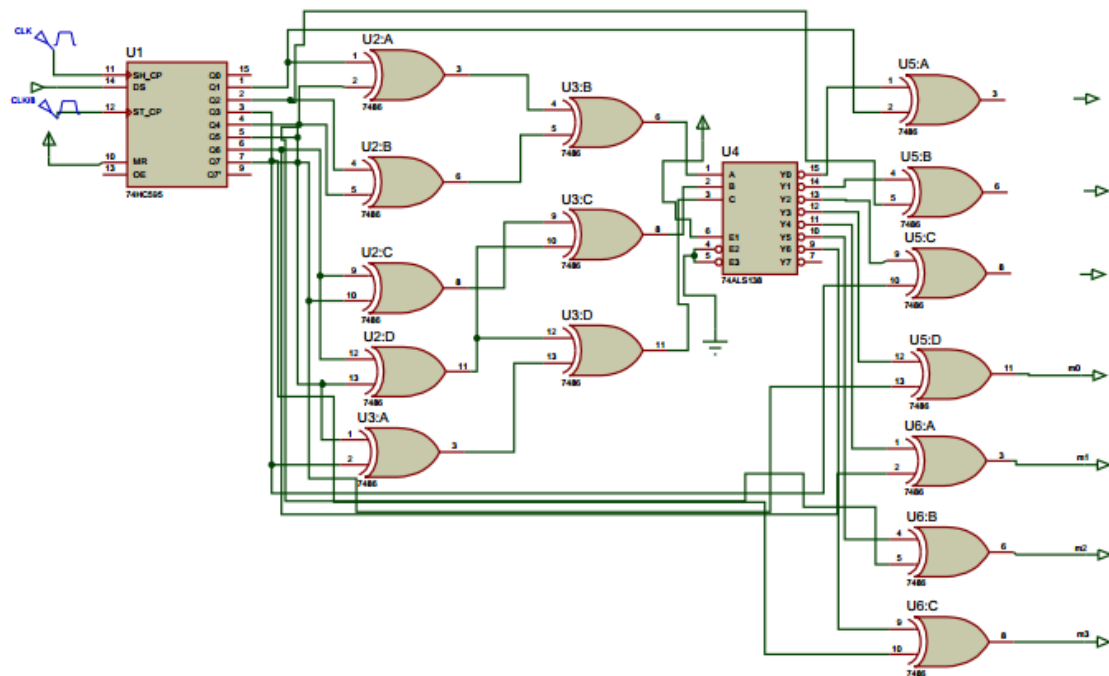
Syndrome	Error Bit
000	No error
001	R3
010	R2
011	R5
100	R1
101	R7
110	R4
111	R6

Circuit Diagram

Encoder



Decoder



Inferences

- i. 74LS595 IC needed two clock pulses, one is one-eighth of the other.
- ii. It should be careful that serial to parallel IC and parallel to serial IC are synchronized.
- iii. The output from decoder IC is active low, so that the output from decoder is also active low.