

EC4098 Major Project Report

BIO Moitoring System using FPGA

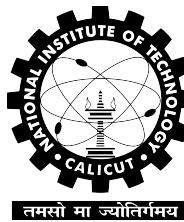
*Submitted in partial fulfillment of
the requirements for the award of the degree of*

**Bachelor of Technology
in
Electronics and Communication Engineering**

Submitted by

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Finally, we thank The Almighty for the wisdom and perseverance that he has bestowed upon us.

DECLARATION

We hereby declare that this submission is our own work and that, to the best of our knowledge and belief, it contains no material previously published or written by another person nor material which has been accepted for the award of any other degree or diploma of the university or other institute of higher learning, except where due acknowledgment has been made in the text.

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Abstract

Bio monitoring system is the diagnosis of important vitals of human beings to detect fatal diseases. The rising cost in diagnosing these diseases makes it uneconomical for common people. Doing the analysis on a FPGA board will open the opportunity to reconfigure functions specific to patients' need. The main vitals needed for diagnosis: EMG, ECG and EEG was acquired using different approaches. The EMG acquired signal was tested for muscle fatigue whereas the ECG signal for arrhythmia and the EEG signal was processed for finding the number of eye blinks. For testing the algorithms, we processed the signals on a Spartan 3E board and later we designed an FPGA board solely for the purpose of EMG and ECG processing.

Contents

1	Introduction	1
1.1	Motivation and Overview	1
1.2	Problem Statement	2
1.3	Thesis Organization	2
2	Literature Survey	3
2.1	Existing Bio monitoring systems in the market(COST)	3
2.2	Electromyography	4
2.2.1	EMG signal processing Algorithm	5
2.3	Electrocardiography(ECG)	6
2.3.1	ECG signal processing Algorithm	7
2.4	Electroencephalography	7
2.4.1	EEG signal processing Algorithm	8
2.5	XILNX SPARTAN 3E FPGA board	8
3	Signal Acquisition	10
3.1	EMG Acquisition	10
3.1.1	Instrumentation Amplifier	10
3.1.2	Low pass Filter	12
3.1.3	Sallen-key low pass filter	12
3.1.4	Sallen-key high pass filter	14
3.2	ECG Acquisition	15
3.2.1	AD8232 ECG ACQUISITION MODULE	15
3.2.2	Acquisition configuration	16
3.3	EEG Acquisition	18
3.3.1	Neurosky	18
4	Signal Analysis	19
4.1	EMG signal Analysis	19
4.2	EEG Signal Analysis	25
4.2.1	Algorithm and Working	25

4.2.2	Results	26
4.3	ECG Signal Analysis	28
4.3.1	ECG signal Acquired	28
4.3.2	ECG signal Processing	29
5	Real time implementation of Bio- monitoring system	33
5.1	ADC using Micro-controller	34
5.2	Current driver LN 298	34
5.3	Result	35
6	FPGA Board Design	37
6.1	Power up Circuit	37
6.1.1	Bypass capacitors	40
6.2	Clock Circuit	40
6.3	GPIO circuitry	41
6.4	JTAG circuitry	42
6.5	Schematic	43
6.6	Layout	43
6.7	FPGA Fabrication cost	44
7	Conclusion	45

List of Figures

2.1	CHOICEMMED MD100B handheld portable ecg monitor [1]	3
2.2	emg	5
2.3	ECG impulse [2]	6
2.4	EEG	7
2.5	XILNX SPARTAN 3 FPGA board [3]	9
3.1	Block Diagram For EMG Signal Acquisition	10
3.2	Circuit Diagram of INA 122IC	11
3.3	Simulated plot of output and input for 20 Hz sine wave	11
3.4	Circuit diagram of Low pass filter	12
3.5	Single stage Sallen- Key Low pass filter	14
3.6	Single stage Sallen-Key High Pass Filter	14
3.7	Simulated Frequency response of three stage Sallen Key High Pass Filter	15
3.8	AD8232 ECG ACQUISITION MODULE	15
3.9	Sensor pad wires	16
3.10	Placement of sensor pads on body	17
3.11	ECG Acquisition breadboard diagram	17
4.1	Algorithm to find Muscle fatigue	20
4.2	Muscle stressed condition time domain representation	21
4.3	Muscle relaxed condition time domain representation	21
4.4	Simulated values of moving average and moving rms of EMG signals.	21
4.5	Simulated values of Moving rms of EMG signals.	22
4.6	Simulated values of Moving average of EMG signal	22
4.7	Simulated plot of EMG signal(positive cycle only)	22
4.8	Simulated plot of slope of EMG signal	23
4.9	Simulated plot of EMG signal with muscle fatigue	23
4.10	Moving RMS plot of EMG signal under resting potential with muscle fatigue	24
4.11	Algorithm for EEG Anaysis	25

4.12	two blinks	26
4.13	Continuous Blinks	27
4.14	motion artifact	27
4.15	Power artifact	28
4.16	Observed ECG signal	28
4.17	Arrhythmia Algorithm	30
4.18	Matlab simulation of the preprocessing stage	31
4.19	Features Extraction	32
5.1	Block Diagram of the Implementation of Bio-Monitoring system	33
5.2	Ln298 Current driver	34
5.3	Working Plan of Bio Monitoring System	35
6.1	Block Diagram for Board Design	37
6.2	Internal Power supply Generation	38
6.3	Power Supply for IO pins	39
6.4	Power Supply for PLL	40
6.5	External clock	41
6.6	GPIO circuitry	41
6.7	JTAG circuitry	42
6.8	Schematic of the FPGA Board	43
6.9	Bottom layout	44

Chapter 1

Introduction

1.1 Motivation and Overview

Medical expenses are one of the most budgeted in one's lifetime. Chronic diseases can break more than a generation's savings. So early detection of the symptoms which these ailments produce is necessary.

Health issues related to heart and muscles are a raising concern nowadays. The analysis and deduction of EMG, ECG and EEG signals are important in medical science for proper treatments of these issues. But the readily available systems used in multi-speciality hospitals are high cost devices and are not suitable for a common man to use.

For early detection of diseases affecting muscles and hearts, we need a system that can be installed in homes and that are portable and that are cheap. Even though cheap acquisition modules and devices are available , the processing units are still very expensive and are incapable of multitasking,i.e processing more than one bio-signal.

The processing capability of FPGA board for simultaneous processing and analysing of ECG, EMG and EEG signals are very high. The digital filter implementation is equally possible in FPGA similar to DSP processing boards. Since more number of channels and least cost in large bulk of production makes FPGA more favourable to this job.

Moreover, FPGA allows systems to be made specific to patients requirements. It is not necessary for a patient to buy a high end system if he/she does not utilize its full functionality. Tailor-made FPGA systems are the

next cheap solution the medical treatments.

1.2 Problem Statement

The project aims to make a low cost Bio-Monitoring system using FPGA. The objectives of the project are:

- To acquire the ECG, EMG and EEG signal with sufficient accuracy.
- To analyse the EMG signal for muscle fatigue
- To analyse the EEG signal for detecting eye blink
- To analyse the ECG signal for detecting Arrhythmia
- To verify the working of the Bi-monitoring system on a standard FPGA board
- To implement the Bio-monitoring system on a custom made FPGA board.

1.3 Thesis Organization

In chapter 2, we have a study about existing Bio-monitoring systems and there is also background study on ECG, EMG, EEG signals and also on SPARTAN 3E FPGA Board. In chapter 3, there is detailed explanation on the EMG, ECG and EEG acquisition including the hardware circuit design and details about the modules used in acquisition. In chapter 4, There is a structured explanation of the algorithms used for detection of fatal diseases and plots of their simulation. In chapter 5, it explains how we have implemented a real time system on a standard FPGA Board and displays their results. In chapter 6, It fives information on how to make a custom FPGA board based on our purpose.

Chapter 2

Literature Survey

We began our project with designing our ECG, EMG and EEG signal acquisition stages. The design was made with keeping in mind the overall cost of the system and kept researching on the newly available systems and their cost. We wanted a system that can process multiple signals at a time over the accuracy and high end functions, cause normal people will not require so many functions. Having the ability in FPGA to reconfigure, it makes more flexible and cost efficient.

2.1 Existing Bio monitoring systems in the market(COST)

- CHOICEMMED MD100B HANDHELD PORTABLE AND ELECTRODE-FREE ECG MONITOR



Figure 2.1: CHOICEMMED MD100B handlheld portable ecg monitor [1]

This device records fast measurement in just 30 seconds, stores 100 ECG records, each record with 30-second ECG waveform and analysis result, Display of ECG waveform, heart rate and analysis results.

Price: Rs. 9800 [1]

This device is used solely for the purpose of ECG. It guarantees best ECG monitoring in the market but can't provide functions specific to patient needs. It has recording capability of 100 ECG records. But a patient who does not require such storage requirement will be wasting money and would rather like to spend it on a device tailor made to his requirement.

- **IX-BIOx EMG SYSTEM**

A four channel Bio potential amplifier that allows acquisition of ECG, EOG, and EMG from a moving or resting object. The interface is done in Labscribe software and connected to Mac or Windows.

Price: Rs 8500[4]

- **CONTEC 3 CHANNEL ECG MACHINE**

It has 12 leads and can simultaneously acquire ECG signals, it has a DSP processor and many filters to get high quality ECG waveforms. It auto analyzes and auto interprets the ECG waveform.

Price: Rs 32,000[5]

2.2 Electromyography

Electromyography (EMG) is a discipline that records and evaluates evaluating and recording the electrical signal that emanates from skeletal muscles. An instrument called electromyograph, which produces an electromyogram helps in recording these signals [1]. The electrical potential generated by muscle cells when these cells are electrically or neurologically activated is detected by an electromyograph [1]. It has wide applications in the medical field. It is used as a diagnostics tool for identifying neuromuscular diseases, or as a research tool for studying kinesiology, and disorders of motor control. They are used also as a control signal for prosthetic devices such as prosthetic hands, arms, and lower limbs.

A number of muscle fibers clubbed into different motor units form the most prominent part of a muscle. This motor unit can be regarded as the

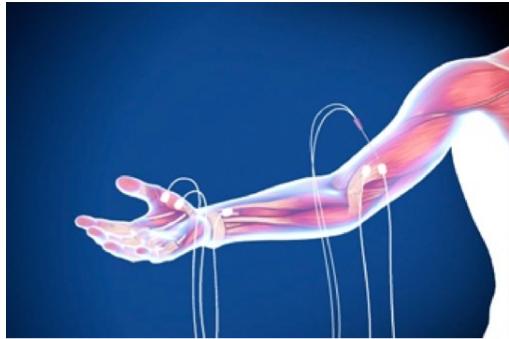


Figure 2.2: emg

fundamental building block of a muscle. Stimulations from motor neurons result in muscle contraction. As an action potential travels along a motor nerve to muscle fibers, it initiates an action potential along the muscle fiber membrane, which depolarizes the muscle fiber membrane and travels within the muscle fiber [2]. Electro-chemical reaction that follows will initiate attractive forces between the myosin and actin filaments and they start sliding together. This causes muscle contraction. There are three types of muscle contractions which are isometric, concentric and eccentric contractions.

The EMG signal can be described as the electrical manifestation of the neuromuscular activation arising from contracting muscles. The current generated by ionic flow across the muscle fiber membrane which propagates through intervening tissues to reach the detection surface of the electrode located in the environment is represented by this signal.

It is largely dependent physiological and anatomical properties of muscles and the control scheme of the nervous system and therefore, is quite complicated. It can be used to check the amount of fatigue in a muscle. It is done based on the changes in the mean absolute value of the signal, increase in the amplitude and duration of the muscle action potential and an overall shift to lower frequencies.

2.2.1 EMG signal processing Algorithm

The EMG signal has to be tested for muscle fatigue or not. The algorithm used was proposed by other authors. They showed that the moving average value of the EMG signal under zero action gives a higher value[7].

And the beginning of the action potential can be calculated by slope value higher than a predefined threshold value. A negative slope value soon after a large positive value determines relaxation.[9]

2.3 Electrocardiography(ECG)

Electrocardiography is the process of recording the electrical activity of the heart over a period of time using electrodes placed on the skin. These electrodes detect the tiny electrical changes on the skin that arise from the heart muscle's electro-physiologic pattern of depolarizing during each heartbeat. It involves measurements of voltage change or electric current on a wide variety of scales from single ion channel proteins to whole organs like the heart[6] .

The ECG signal is separated into two intervals

- PR interval
- QT interval

The PR interval is the first part of the wave generated by the impulse travelling from right to left atrium. These electrical signals will make the chambers in heart to depolarize. It drains the de-oxygenated blood by contraction.

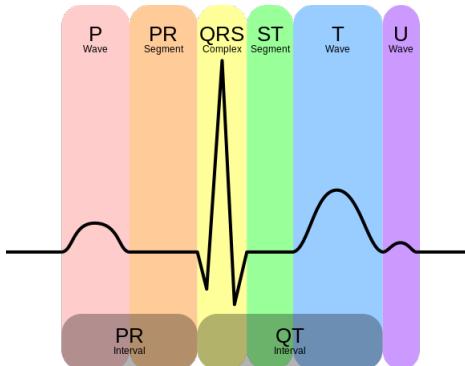


Figure 2.3: ECG impulse [2]

A lot of interesting events take place in the QT interval, the QRS interval causes the beep sound in the medical monitoring equipments since it is where both ventricles begin to pump. After this contraction comes the ST quiet time where the ventricles are waiting to be re-polarized and the T waves is when the ventricles are relaxing.

2.3.1 ECG signal processing Algorithm

The arrhythmia detection is divided into 4 sections and the ECG data has two go through these 4 sections:[10]

- ECG Preprocessing
- QRS Detection
- Features Extraction
- Arrhythmia Interpretation

Further information on these processes will be explained in ECG signal processing section

2.4 Electroencephalography

Electroencephalography (EEG) is an electrophysiological monitoring process capable of tracking the electrical activity of brain. Generally noninvasive way of placing the electrodes along the scalp is preferred. The fluctuations in voltage caused by the ionic current within the brain neurons are measured. That is, the spontaneous activity is recorded with the help of multiple electrodes placed on the brain. The specific features of spectrum are analyzed to arrive at diagnostic conclusions. Diagnosis of diseases like epilepsy, sleep disorders, coma, encephalopathies, and brain death can be diagnosed with the help of EEG. Though there are advanced options like MRI and CT, EEG has not lost its relevance as millisecond- range spacial resolution makes it unique from the rest.



Figure 2.4: EEG

Neurons, the main constituents of human brain, maintain the electric charge of human brain. They continuously exchange ions with the extracellular milieu in order to propagate action potentials and maintain resting potential. Because of volume conduction, push and pull voltages are formed and their measurement gives us the EEG. The potential formed in a single neuron is inconsequential. EEG activity therefore always reflects the summation of the synchronous activity of thousands or millions of neurons that have similar spatial orientation.

Conventionally, electrodes are placed on the scalp with the help of a conductive paste or gel. Each electrode is connected to one input of a differential amplifier and a common system reference electrode is connected to the other input of each differential amplifier. These amplifiers amplify the voltage between the active electrode and the reference. In the case of digital EEG systems, amplified signal is digitized via an analog-to-digital converter, after being passed through an anti-aliasing filter. It has significantly low hardware costs than other techniques and also very high temporal resolution. It doesn't trigger claustrophobia and is tolerant of subject movement.

2.4.1 EEG signal processing Algorithm

Analysis of EEG signal is based on two step:

- First is the Sample value verification.
- Second is calculation of the Kurtosis value.

[?]

The kurtosis value, i.e the fourth order central momentum is checked only after the sampled value of the EEG signal is high. The Kurtosis value ensures that the received EEG signal is because of blinking and not because of power or motion artifacts. [?]

2.5 XILNX SPARTAN 3E FPGA board

The reason for using an industry made XILNX 3E spartan board in this project for FPGA processing is to study how to process and analyse a EMG and ECG signals before developing a self designed FPGA board

Features of the Spartan 3E Board that makes it apt for our project:[3]

- Up to 232 user-I/O pins

These pins enable us to process many signals in parallel form. In this project we will be getting the ECG and EMG signal in 8 bit form. If we want to extend the applications to EEG or increase the monitoring applications, the board can support it. It can also handle a 8 bit LCD display through this pins.



Figure 2.5: XILNX SPARTAN 3 FPGA board [3]

- Low cost of board

The price of a Spartan 3E board is approximated to be Rs 3000/- which is cheaper compared to other high end DSP boards where its high end functions are not used for our project

- Xilinx ISE suite

It is a software tool released by Xilinx for analysis and synthesis of HDL, enabling the user to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Chapter 3

Signal Acquisition

3.1 EMG Acquisition

The approach towards the EMG signal Acquisition is the traditional way of using an instrumentation amplifier.

Given below is the block diagram for the acquisition stage:

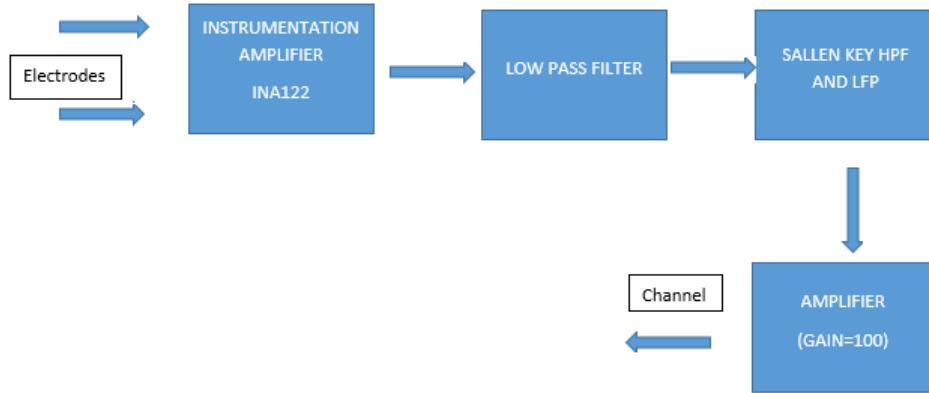


Figure 3.1: Block Diagram For EMG Signal Acquisition

3.1.1 Instrumentation Amplifier

INA 122 IC is used in this stage to amplify the input differential signal. The thermal noise and power supply noise can be avoided to an extent using this circuit. INA 122 IC can reject common mode voltages upto 3.4 volts with a CMRR of 96 (typical value). This is much higher than our common mode

noise voltages (switched power supply noise of 10-100uV range). The gain of the amplifier is given by the equation $5 + (200k/Rg)$ and is set to 10V/V. The gain of initial stage is set to a smaller value in order to avoid enormous amplification of noise. The PSRR of the IC is typically 120 and is enough to avoid 50 Hz power supply noise. There are higher ICs of the same series with better performance but INA 122 matches with our requirement and is locally available in the market.

Design:

$$5 + ((200k)/R1) = 10[7]$$

$$R1 = 47k[7]$$

where R1 is the resistor designed to be kept between pin 1 and 8 [7]

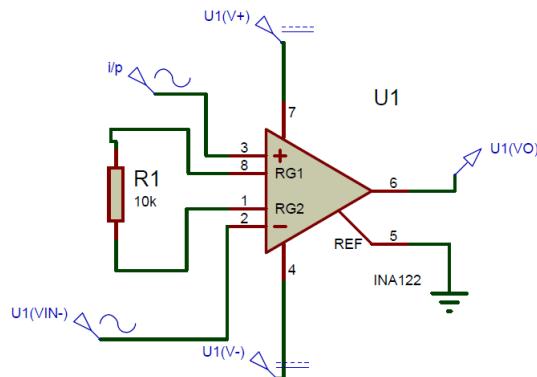


Figure 3.2: Circuit Diagram of INA 122IC

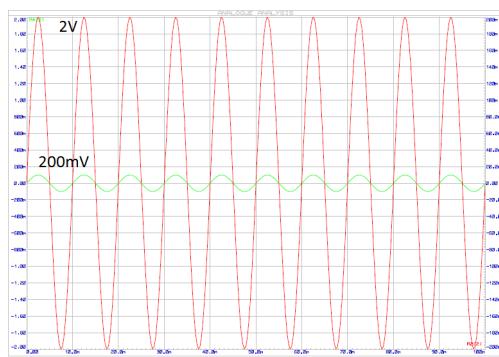


Figure 3.3: Simulated plot of output and input for 20 Hz sine wave

3.1.2 Low pass Filter

Due to the electrodes, noises greater than 40hz (Bandwidth of the EMG signal)are generated, therefore we are designing a low pass filter with cutoff 40hz.

Design:

$$H(s) = \frac{V_d(s)}{V_{in}(s)} = \frac{-Z_f}{R_{in}}[8] = \frac{(-R_f/R_{in})}{1+R_fCs}[8]$$

and

$$\begin{aligned} f_c &= \frac{1}{2\pi R_f C} = 100\text{kHz} \\ R_f &= 1K[8] \\ C &= 1.5\mu\text{F}[8] \end{aligned}$$

Hence the Value of R_f is taken as 1K and the Value of C is taken as 1.5uF.

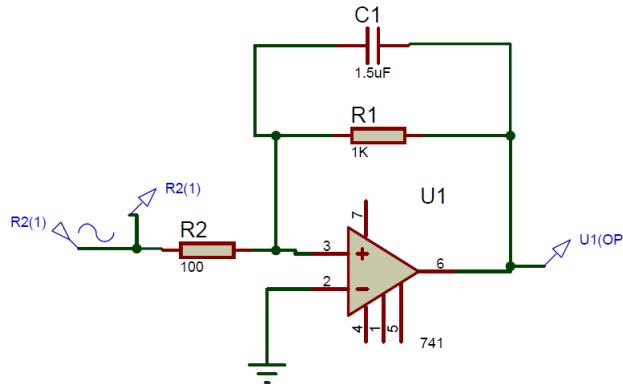


Figure 3.4: Circuit diagram of Low pass filter

3.1.3 Sallen-key low pass filter

Sallen key is a VCVS filter topology. These are two pole low pass, high pass, band pass, band reject filters with unity gain at zero frequency, out of which low pass filter and high pass filters are used here. Since we need a flat frequency response in the pass band even though the transition band is wider, we selected a filter with butter worth behaviour. The quality factor of the circuit used is about 1.58 and the cut-off frequency is designed to be

200 Hz. This is to suppress the high frequency noise of the switching mode power supply to maximum extent (around an attenuation of 60dB at 500Hz).

The transfer function for the sallen key opamp circuit can be derived in the following form

$$H(s) = \frac{w_0^2}{s^2 + s(w_0/Q) + w_0^2} [8]$$

and

$$\begin{aligned} V1 &= i_{c2}R_2 + V_{out} [8] \\ V_1 + v_{out}R_2C_2s + V_{out} &[8] \\ V_1 &= V_{out}(R_2C_2s + V_{out}) [8] \end{aligned}$$

The sum of the currents at node V1

$$i_{c2} = i_{c1} + i_{R_1} [8]$$

and

$$\frac{v_{out}}{\frac{1}{sC_2}} = \frac{V_{in}-V_1}{R_1} + \frac{V_{out}-V_1}{\frac{1}{sC_1}} [8]$$

substituting for V1

$$H(s) = \frac{\frac{1}{R_1R_2C_1C_2}}{s^2 + S(\frac{1}{R_2C_1} + \frac{1}{R_1C_1}) + \frac{1}{R_1R_2C_1C_2}} [8]$$

and

$$\begin{aligned} c_1 &= \frac{2Q}{Rw_0} [8] \\ c_2 &= \frac{1}{2RQw_0} [8] \end{aligned}$$

and

$$Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} [8]$$

Hence the values taken for R=16k and $C_1 = 330nF$ and $C_2 = 33nf$

A single section of the four stage cascaded sallen-key Low pass filter is given below

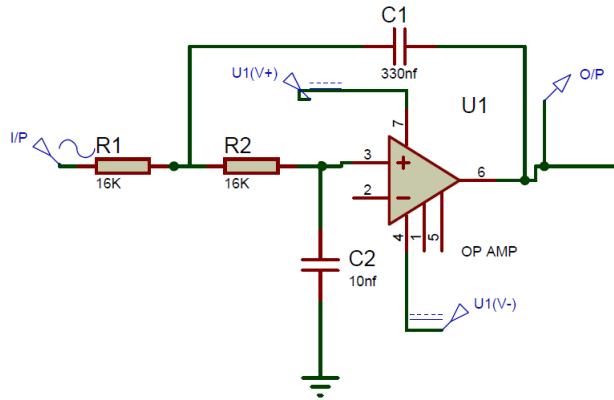


Figure 3.5: Single stage Sallen- Key Low pass filter

3.1.4 Sallen-key high pass filter

Sallen key High pass filter is also filter with butter worth characteristics. It is used to reject unwanted signals of frequencies less than 5 Hz. The noises at low frequencies would not be removed by the low pass filter section used. Sallen key High pass filter is used since it has a flat frequency response in the pass band and has good Q-factor.Hence Q is taken to be 2 and designed accordingly.

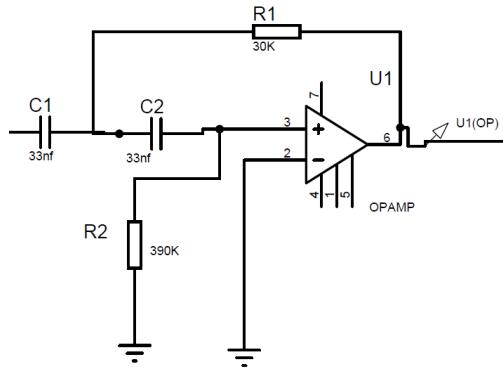


Figure 3.6: Single stage Sallen-Key High Pass Filter

$$H(s) = \frac{C_1 C_2 s^2}{\frac{1}{R_1 R_2} + \frac{s C_2}{R_2} + \frac{s C_1}{R_2} + C_1 C_2 s^2} [8]$$

and

$$w_0^2 = \frac{1}{R_1 R_2 C_1 C_2} [8]$$

and

$$Q = \frac{1}{2} \sqrt{\frac{R_2}{R_1}} [8]$$

$$R_1 = 30k, R_2 = 390k \text{ and } C_1 = C_2 = 33nf$$

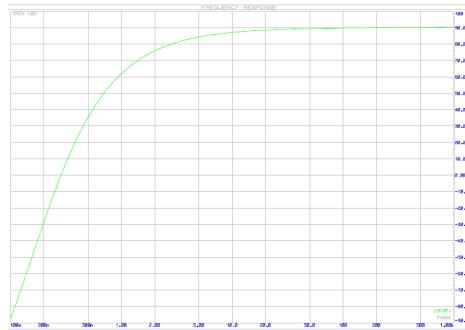


Figure 3.7: Simulated Frequency response of three stage Sallen Key High Pass Filter

3.2 ECG Acquisition

3.2.1 AD8232 ECG ACQUISITION MODULE

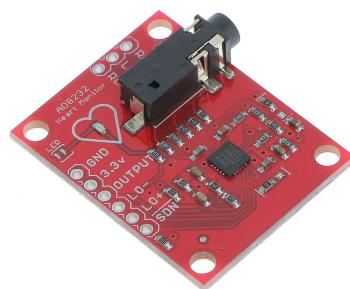


Figure 3.8: AD8232 ECG ACQUISITION MODULE

This module is an integral acquisition block which is used for acquiring the ECG signal. The module provides 9 connections that you can solder

pins, wire and other connectors. The essential pins in the board are:

Pin Label	Pin Function
GND	Ground
OUTPUT	Output Signal
3.3v	3.3v Power Supply
SDN	Shutdown
LO+	Leads-off Detect +
LO-	Leads-off Detect -

The SDN pin is not connected, since making this pin high will power down the board. The sensor pad pins are also given above.



Figure 3.9: Sensor pad wires
[2]

Pin Label	Pin Function
BLACK	RA (Right Arm)
RED	LA (Left Arm)
BLUE	RL (Right Leg)

3.2.2 Acquisition configuration

Since we have done our EMG acquisition in a purely hardware approach due to time constraints we have used the AD8232 ECG acquisition module.

We have seen the basic pin connections in the theory section and now we can look at the placement of the sensor pad. It is said to connect the pads

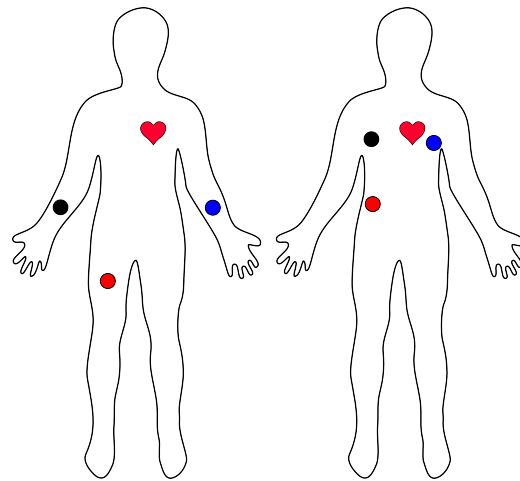


Figure 3.10: Placement of sensor pads on body
[2]

on to the leads before attaching to the body to protect the sensors.

The sensor pads are connected to the body as shown in one of the above diagrams. The RA, LA, RL stands for right arm, left arm and right leg respectively. The lead sensors have been soldered in and connected according to the circuit given below:

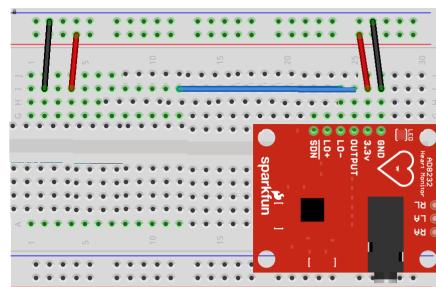


Figure 3.11: ECG Acquisition breadboard diagram
[2]

3.3 EEG Acquisition

3.3.1 Neurosky

Neurosky mindwave mobile, a BCI technology, is used for EEG signal Acquisition. It is used in major for low cost EEG linked products and research.



It detects the alpha band EEG wave which is in the frequency range of 8-15Hz. Its major advantage is its inexpensive dry sensor which is durable. The Neurosky module is interfaced using a software called OPENVIBE.

Openvibe is a real time software used for processing and testing of brain wave signals. Brain Signal acquisition ,Filtering, processing and classification can be done by using this software. Brain computer interface is one of the prominent application of openvibe software which provide real time diagnosis and biofeedback of brain signals. It consist of a set of software modules that are written in C++ . Main features of openvibe software including its portability, modularity ,vast signal processing methods and user friendly graphical language.

Openvibe software is used in the neurosky platform. It handles electrical signals that are transmitted from the surface of brain .Noise reduction process is done after data acquisition phase. Next stage is feature extraction which keeps the frequency range corresponding activites. At the same time it learns users different reactions.This is followed by signal processing stage. Available functions are listed in the right side of openvibe software. So user can easily take advantage of these functions and visualize the 2D and 3D signals in the monitor.

Chapter 4

Signal Analysis

4.1 EMG signal Analysis

EMG is a recorded electrical signal which represents the mathematical activity of the skeletal muscles due to the stimulation by our nervous system. In the simulation stage, we are considering a mathematical model of EMG signal represented by $96 * (t^3) * e^{-t} - 90$. Since the information obtained from the negative portion of EMG signal is also obtained from the positive portion of the EMG signal even though they are of different magnitudes, we are considering only the positive portion of EMG signal represented by the mathematical model $96 * (t^3) * e^{-t} - 90$ for simplicity.[9]

A moving window of 10 sample is considered and the moving average and moving rms values are calculated in order to identify the peak of EMG signal, muscle fatigue and the beginning of action potential. The difference in time between the beginning and the ending of action potential shows the information about muscle ageing, more the time delay more will be the ageing. The detailed block diagram of our analysis methodology is give below as a flow chart;[9]

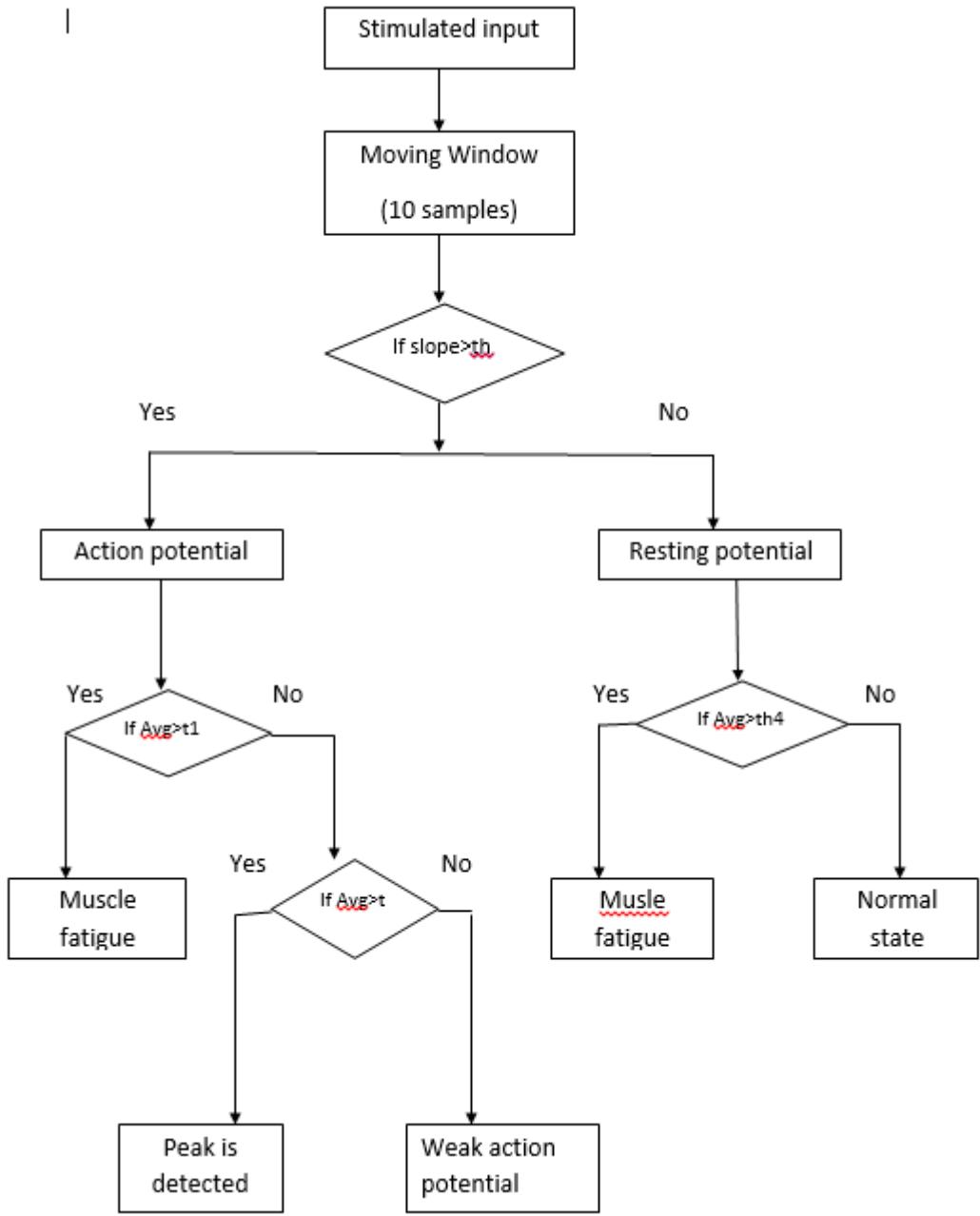


Figure 4.1: Algorithm to find Muscle fatigue

- EMG signal Acquisition

The EMG detection has been done using analog circuitry as explained earlier. The EMG signal under relaxed and stressed muscle conditions are given below

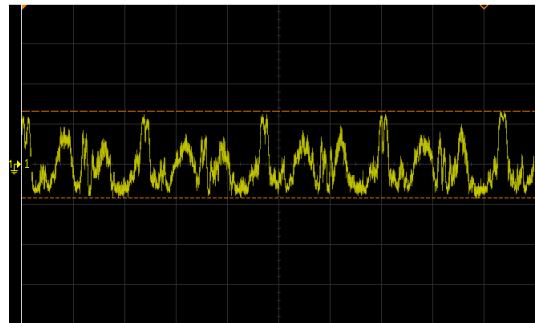


Figure 4.2: Muscle stressed condition time domain representation



Figure 4.3: Muscle relaxed condition time domain representation

- Xilinx ISE suite simulation

The sampled values of mathematical model of EMG signal that have been acquired from the MATLAB are then processed in ISE suite to obtain the moving average, moving RMS values. The simulation window of the final results are given below;

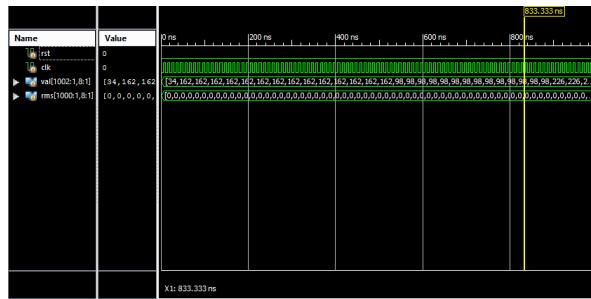


Figure 4.4: Simulated values of moving average and moving rms of EMG signals.

Name	Value	0 ns	200 ns	400 ns	600 ns	800 ns	833.333 ns
[S44,B:1]	240						
[S43,B:1]	240						
[S42,B:1]	240						
[S41,B:1]	240						
[S40,B:1]	8						
[S39,B:1]	8						
[S38,B:1]	8						
[S37,B:1]	8						
[S36,B:1]	8						
[S35,B:1]	8						
[S34,B:1]	8						
[S33,B:1]	8						
[S32,B:1]	8						
[S31,B:1]	8						
[S30,B:1]	72						
[S29,B:1]	72						

Figure 4.5: Simulated values of Moving rms of EMG signals.

Name	Value	0 ns	200 ns	400 ns	600 ns	800 ns	833.333 ns
[B68,B:1]	242						
[B67,B:1]	242						
[B66,B:1]	242						
[B65,B:1]	242						
[B64,B:1]	242						
[B63,B:1]	10						
[B62,B:1]	10						
[B61,B:1]	10						
[B60,B:1]	10						
[B59,B:1]	10						
[B58,B:1]	10						
[B57,B:1]	10						
[B56,B:1]	10						
[B55,B:1]	10						
[B54,B:1]	10						
[B53,B:1]	130						

Figure 4.6: Simulated values of Moving average of EMG signal

The simulated plots (in MATLAB) of the EMG signal and the plot obtained from data processed in ISE design suite 14.2 are shown below;

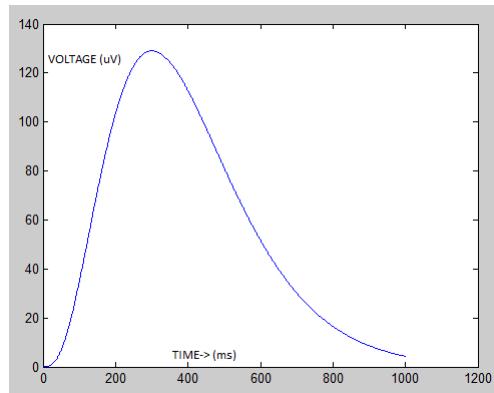


Figure 4.7: Simulated plot of EMG signal(positive cycle only)

The moving average value of the emg signal will cross the usual value if there is muscle fatigue. Muscle fatigue can be detected in two ways[9]

- If the moving average value of EMG signal under zero action gives a higher value.
- If the peak value of the action potential gives a higher value than usual. The beginning of action potential can be calculated by slope value higher than a predefined threshold value. A negative slope value immediately after a large positive value determines the relaxation.

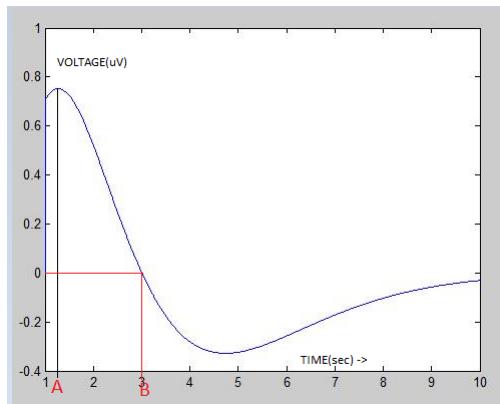


Figure 4.8: Simulated plot of slope of EMG signal

The points A and B represent the beginning and ending of action potential of muscles.[9]

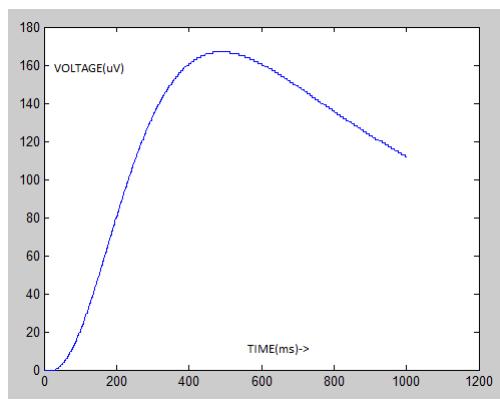


Figure 4.9: Simulated plot of EMG signal with muscle fatigue

If the muscles are in resting potential, in order to analyse the EMG activity we are considering moving rms value of the EMG signal. Moving

average method is avoided here to reject the effect of nominal voltages below zero threshold.[9]

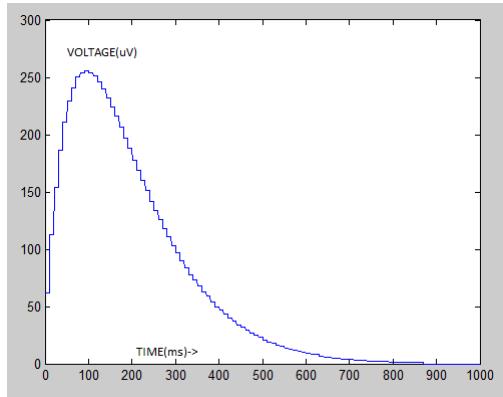


Figure 4.10: Moving RMS plot of EMG signal under resting potential with muscle fatigue

4.2 EEG Signal Analysis

4.2.1 Algorithm and Working

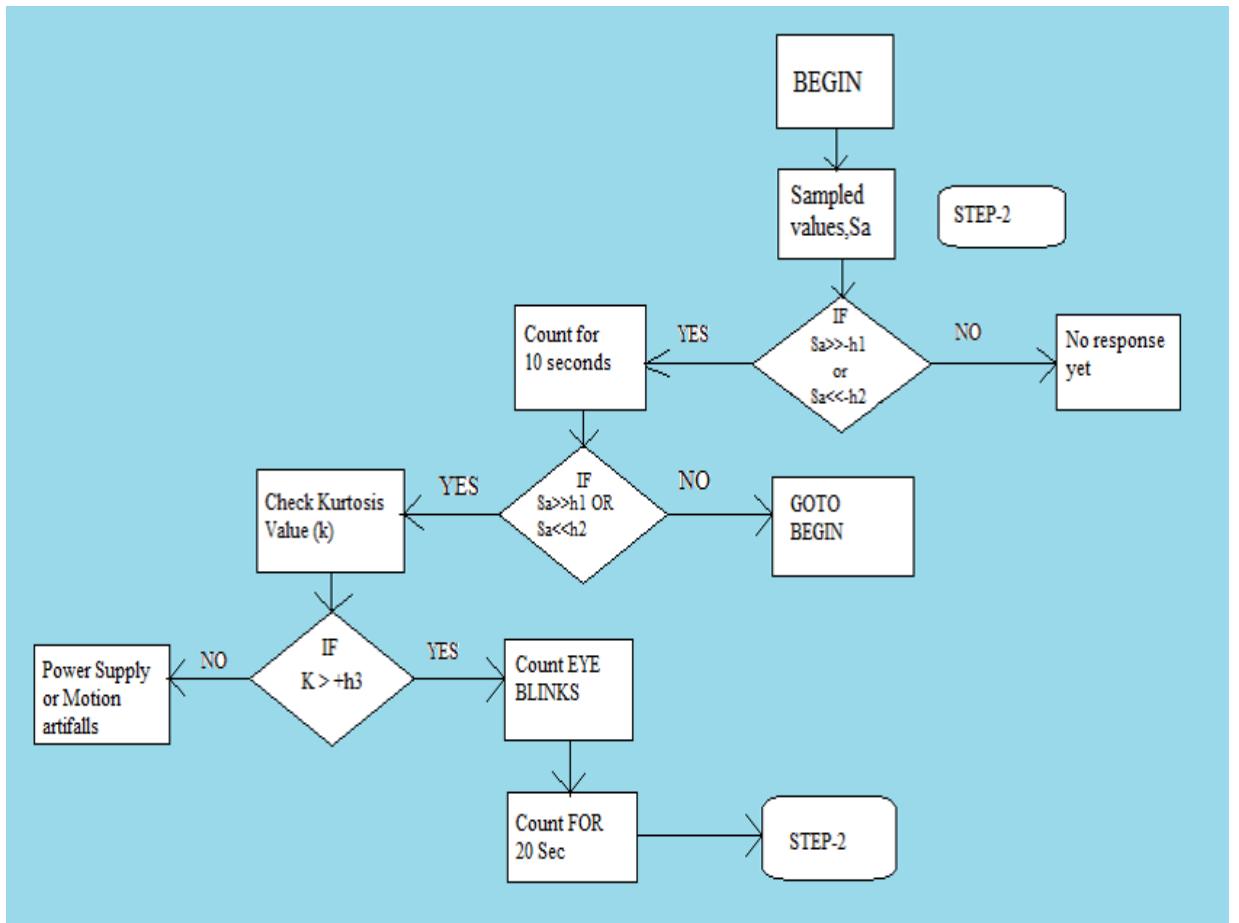


Figure 4.11: Algorithm for EEG Anaysis

Basically, two values are checked for the blinking detection:

- The sample value(Min or Max)
- Kurtosis value [?]

$$KURT = \frac{\frac{n}{i=1} \sum_{i=1}^n (x_i - x_{avg})^4}{(\sum_{i=1}^n (x_i - x_{avg})^2)^2}$$

The signal will be processed if either the positive peak or the negative peak exceeds a pre-defined positive threshold and negative threshold respectively. Then we will wait for 2 seconds to ensure that signal peaks cross the positive or negative peaks again in order to assure that the hike in signal is not occurred non-deliberately. Then we will check the moving kurtosis value (moving fourth order central momentum value) for a sample window of 10 samples. If the kurtosis value becomes greater than the threshold earlier defined, it can be regarded as an eye blink. Otherwise, the signal hike would be the result of any motion artefacts.

4.2.2 Results

When the eyes are blinked twice there are two peaks after a small delay. The strength of the peaks depends on the blink strength.

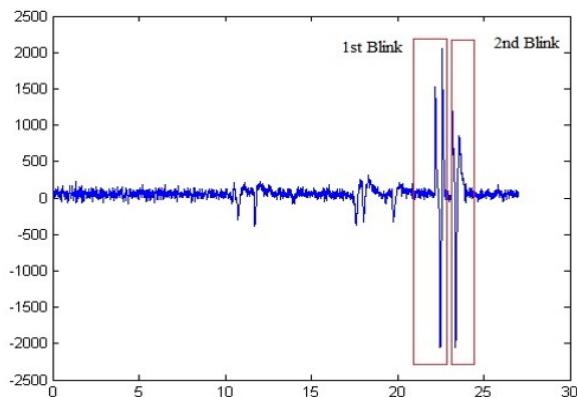


Figure 4.12: two blinks

The below result is observed after a continuous blink.

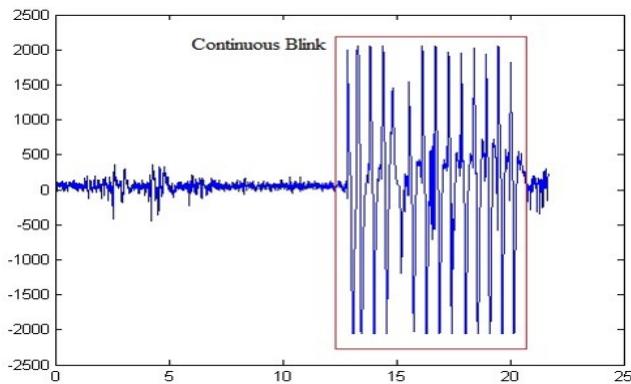


Figure 4.13: Continuous Blinks

Where as this is for motion artefact

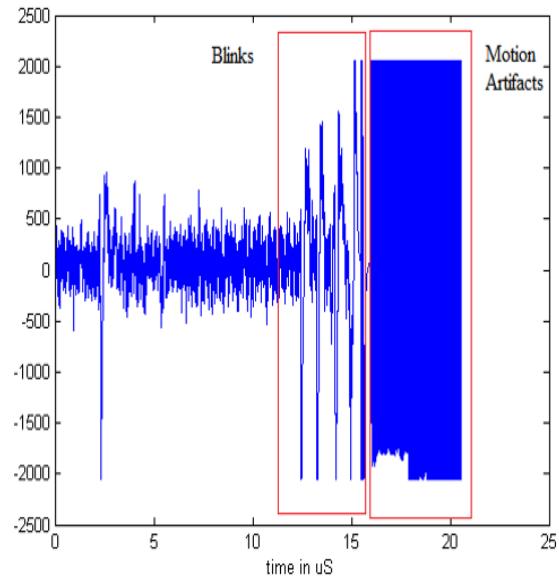


Figure 4.14: motion artifact

And this for Power artifact

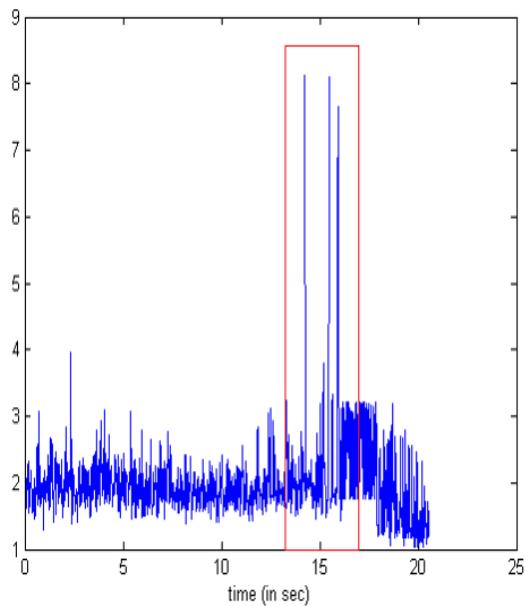


Figure 4.15: Power artifact

After processing with the algorithm motion and power artifacts are explicitly detected and ignored as blinks.

4.3 ECG Signal Analysis

4.3.1 ECG signal Acquired

The above signal was obtained from the output pin of the module. The signal is stable and has very less noise interference.



Figure 4.16: Observed ECG signal

4.3.2 ECG signal Processing

The arrhythmia detection is divided into 4 sections. The ECG data has two go through these 4 sections:[10]

- ECG Preprocessing
- QRS Detection
- Features Extraction
- Arrhythmia Interpretation

Preprocessing

ECG preprocessing was done to remove the DC offset. The raw ECG are preprocessed using a smoothing filter. [10]

The filtered signal $y[n]$ is given by:

$$y[n] = (x[n] + 2x[n - 1] + x[n - 2])/4;$$

where $x[n]$ are the raw ECG signals.

Note: Sampling rate 9600 samples/sec.

QRS Detection

The $y[n]$ filtered signal is differentiated twice and then squared. the final signal then gives the start and end points of the QRS.

[10]

$$\begin{aligned} u[n] &= y[n] - y[n - 1] \\ z[n] &= u[n] - u[n - 1] \\ w[n] &= (u[n])^2 \end{aligned}$$

Note: Sampling rate 9600 samples/sec.

Features Extraction

Once the QRS period is determined, the R points are marked and the cardiac cycle(RR) and the heart rate is obtained[10]

$$HR = (60 * RR) * \text{samplingrate}$$

Note: Sampling rate 9600 samples/sec.

By using a window before each R point, The PR interval and the P-wave duration can also be found observing each beat waveform.[10]

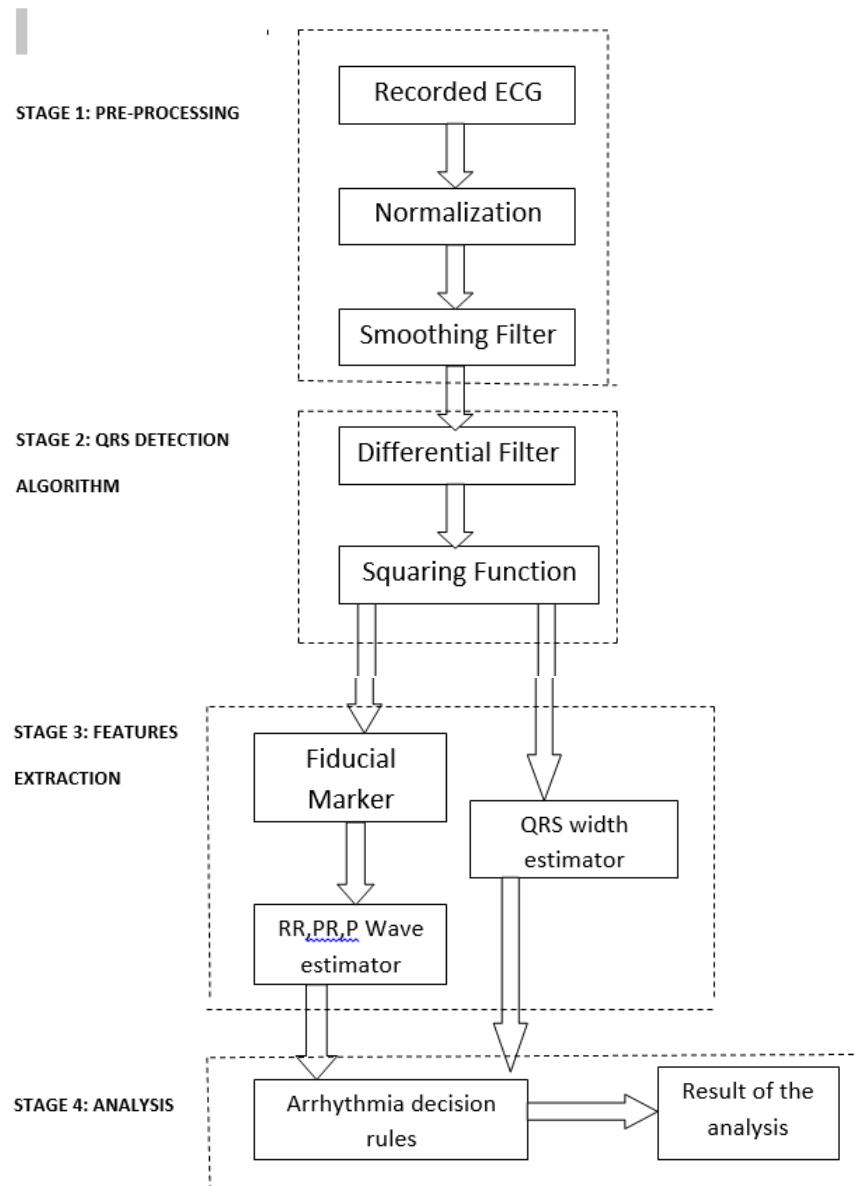


Figure 4.17: Arrhythmia Algorithm

Arrhythmia Interpretation

The main two decision rule was obtained by the below conditions on the basis of the features obtained from the ECG signal[10]

if(($beat[i] \geq 60$ and $beat[i] < 90$) and ($pr[i] > 0.12$ and $pr[i] < 0.2$) and ($qrs[i] \geq .06$ and $qrs[i] \leq 0.12$))

if(($beat[i] > 90$) and ($pr[i] \geq 0.12$ and $pr[i] \leq 0.2$) and ($qrs[i] \geq .06$ and $qrs[i] \leq 0.12$))

Note: Sampling rate 9600 samples/sec.

By using a window before each R point, The PR interval and the P-wave duration can also be found observing each beat waveform.

ECG signal Analysis and Arrhythmia Detection

Raw data has been collected from the ECG ID database. It is collected for the study of ECG signals [11].

The algorithm for Arrhythmia is simulated on XILINX Design Suite.

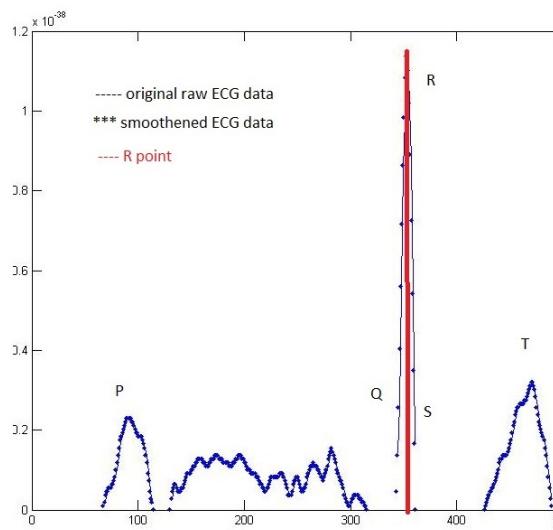


Figure 4.18: Matlab simulation of the preprocessing stage

The above simulation shows the difference in the ECG signal before and after passing through the smoothing filter
The Matlab simulation is done only for the demonstration of the working of the algorithm but the simulation is done exclusively on Spartan ISE suite.

The R point is found by taking the maxima of the data points.

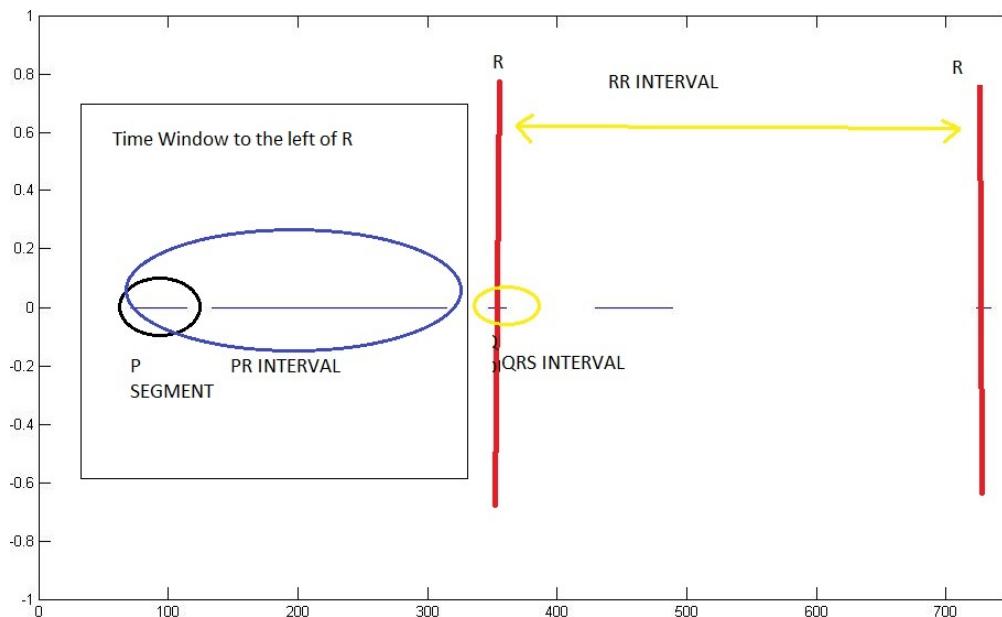


Figure 4.19: Features Extraction

The features are extracted after taking the double differentiation of the smooth signal.

The result will give zero values in the QRS interval, P and T segment interval and NaN values elsewhere. The zero values are measured with a counter and the lowest value counter indicates the QRS interval.

Taking a time window to the left of the R point we can measure the next maxima as the P point and measured the PR interval as these features are required for arrhythmia analysis.

Chapter 5

Real time implementation of Bio-monitoring system

To test our algorithm and to observe the real time limitations of our project, we have decided to implement a live acquisition of ECG and EMG signal. Below given is the block diagram of our implementation.

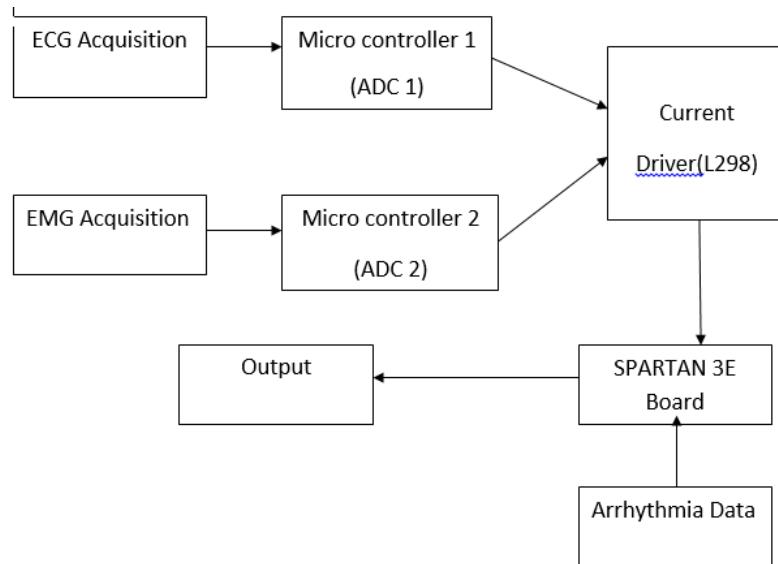


Figure 5.1: Block Diagram of the Implementation of Bio-Monitoring system

The EMG acquisition is done using the pure hardware approach while the ECG is using the module AD8232 to save time. Both these acquisition methods will give the signals in Analog format which has to be converted into

digital for processing in FPGA. FPGA board does not have in built ADC so an outside ADC have to be ensured.

Using ADC IC was faced with difficulties and consumed too much time, so keeping the cost factor intact we used microcontrollers to convert analog data to digital. These data coming out of the digital pins were of 3.2V which was enough voltage but not enough current.

To solve the current issue a current driver had to be included before giving the digital pins of the GPIO pins of the SPARTAN Board.

5.1 ADC using Micro-controller

Due to difficulties faced using an ADC IC, we had to replace it with ATmega328 microcontroller present in Arduino Uno.

The microcontroller has 6 analog inputs of which two are used for EMG and ECG signal inputs respectively. The IO pins give a current of 30-40mA which is not sufficient for the SPARTAN 3E board for processing

5.2 Current driver LN 298

The current from the adc/ microcontroller is not sufficient for the Spartan Board for processing even though it has a voltage of 3-3.3V. To increase the current we used a Current driver IC L298D



Figure 5.2: Ln298 Current driver

5.3 Result

The result is planned to be observed through LCD module already in the Spartan 3E board. The below Diagram shows the presentation of the desired output.

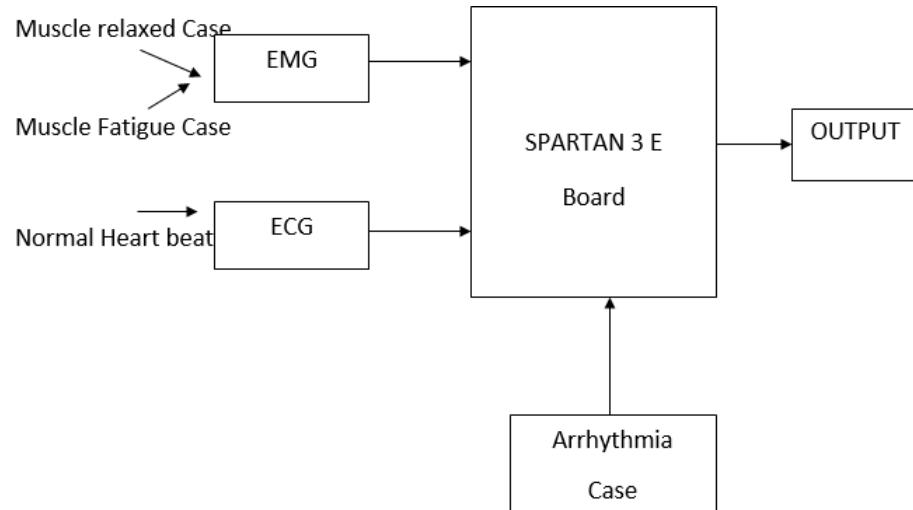
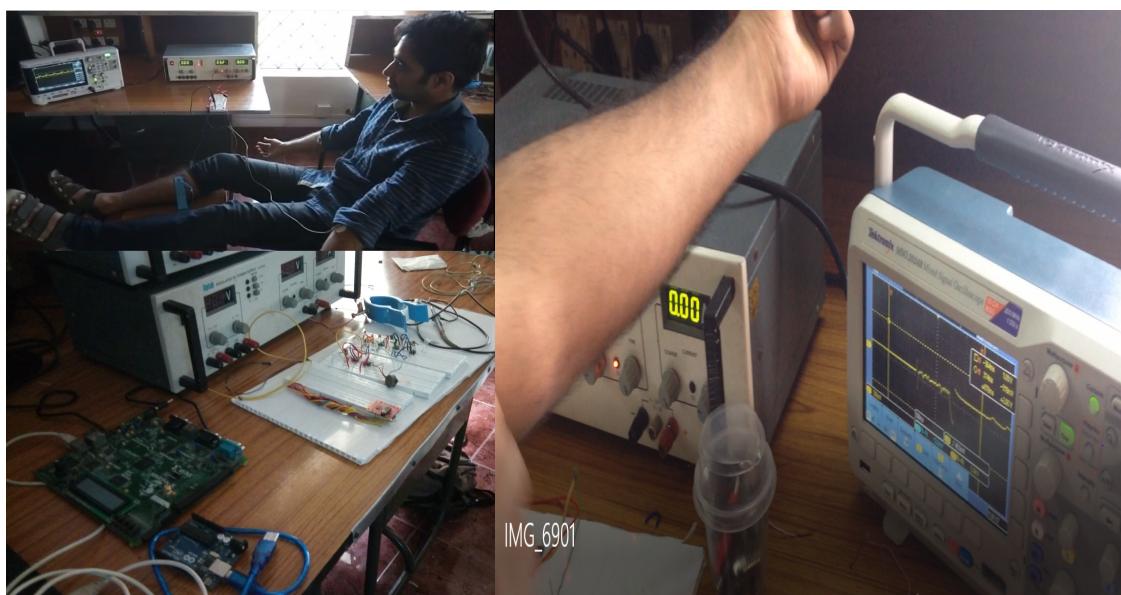


Figure 5.3: Working Plan of Bio Monitoring System



The EMG acquires two case:

- Normal Relaxed EMG signal
- Muscle fatigue

Both these signal are acquired and sent to the FPGA board processed with the respective algorithm and displays the output.

Whereas in the case of ECG, only one case of acquisition is possible and that is Normal Heart beat Analysis. This normal signal will be sent to the FPGA board and processed with its algorithm and display the condition.

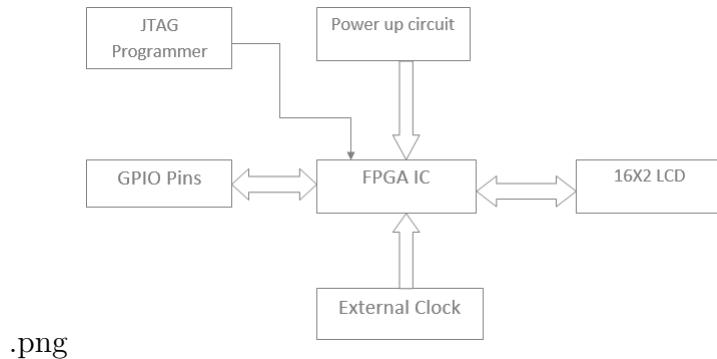
The case of Arrhythmia is practically difficult to acquire, therefore online data of patients with arrhythmia was obtained and processed with its respective algorithm and output is displayed.

Chapter 6

FPGA Board Design

Every FPGA development board consists of some basic indeed sections which includes external clock circuitry, power up circuitry, JTAG programmable hardware and GPIO pins. We have to be accommodated with an additional circuitry for 16x2 LCD display. The external clock frequency used for FPGA IC is 200MHz. The concise block diagram of FPGA development board is given below in figure;

We are using Altera Cyclone-I series IC (EP1C3) in 144 pin TQFP package. This package consists of 104 I/O pins which are more than sufficient for our projects requirements.



.png

Figure 6.1: Block Diagram for Board Design

6.1 Power up Circuit

Altera Cyclone 1 FPGA works on 2.5V supply and IO pins are compatible with 3.3V, 2.5V, 1.8V and 1.5V. The IO compatible voltage can be switched

among these four levels depending upon VCC_{IO} pin voltage. Since our requirement doesn't need multi voltage IO compatibility, we prefer to use 3.3V supply (It can support 2.5V, 3.3V and 5V [12] input signals and can support all the four level voltage compatible outputs). In order to supply 2.5V to the FPGA, we need voltage regulators which provide sharp output so as to ensure the proper working of highly sensitive FPGA ICs. So we use linear drop out voltage regulators, which are suitable for low power applications since it reduces the device count and provides acceptable efficiency for most applications. We prefer series linear voltage regulators due to their comparatively high efficiency compared to other linear voltage regulators.

- **Internal Power Supply for FPGA IC**

The internal power up of the FPGA IC requires 2.5V and it is generated from the DC supply using LM317 IC. The circuit diagram for this power supply generation from a typical DC supply is given in below figure;

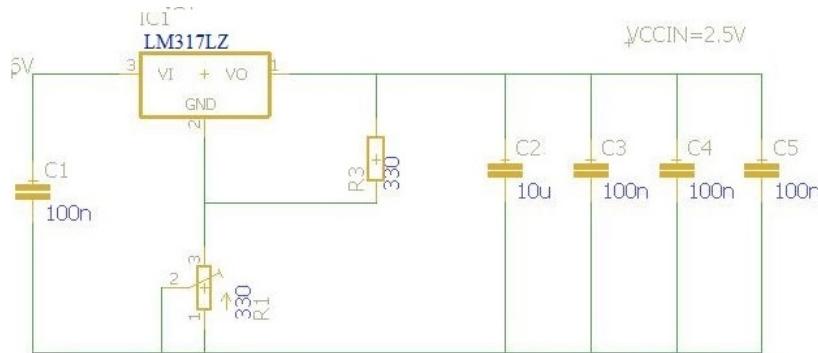


Figure 6.2: Internal Power supply Generation

It is known from the datasheet of LM317LZ that the output voltage is related to the circuit parameters (R_1 and R_3) and adjustable pin (or ground pin) current (I_{ADJ}) as given below [13];

$$V_{out} = 1.25(1 + (R_3/R_1)) + I_{ADJ}(R_3)$$

The typical value of (I_{ADJ}) is 50uA. So we took R_1 as 330 ohms and found out the value of R_3 as 325.7 ohms. We have used potentiometer to accommodate with the slight changes at the output.

The output of the above circuit is connected to VCCINT pin (46th pin) of the FPGA IC with the presence of a shunt capacitance for noise free

environment.

- **Power Supply for I/O Pins, JTAG Programmer and Mode Select**

We have designed a linear dropout power supply of 3.3V from a typical 6V DC power supply in order to power up I/O pins of our FPGA IC, JTAG programmer and to select the mode of operation of FPGA IC by default. The circuit diagram of this power supply is shown in figure below;

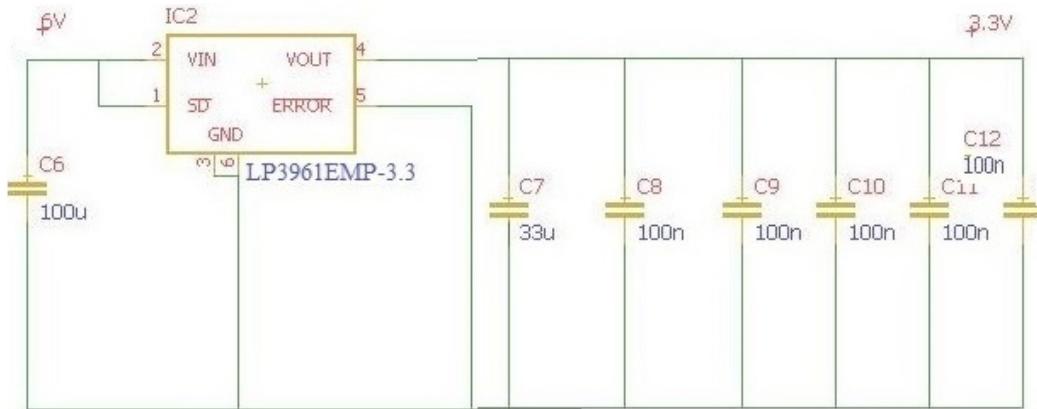


Figure 6.3: Power Supply for IO pins

The output of the IC LP3961EMP-3.3 is exactly 3.3V itself and didn't need to incorporate any additional resistances apart from the output capacitances for noise reduction. The output of the above circuit (3.3V) is connected to the VCCIO1 pin, MSEL0 pin and TMS pin of the FPGA IC (8th, 22nd and 89th pins of the FPGA IC respectively). TMS pin should be connected to 3.3V in order to ensure the proper working of JTAG programming section. The MSEL0 and MSEL1 pins should be connected to 3.3V and ground respectively in order to make the FPGA IC in desired mode of operation.[14]

- **Power Supply for PLL**

The internal circuitry of FPGA IC is very complex and there are almost double the numbers of internal clock signals inside the IC compared to the input clock signals of the FPGA IC. These are generated by circuitry involving PLL and have to be powered up by external power

supply connection.

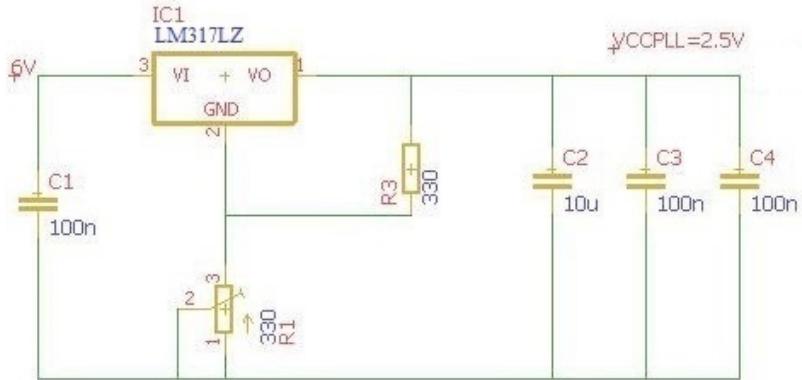


Figure 6.4: Power Supply for PLL

- **Power Up Sequence** Altera Cyclone-I ICs are designed in order to support any possible power up sequences. Hence V_{DDIO} , V_{AND} and V_{DDINT} power supplies can be powered in any order.

6.1.1 Bypass capacitors

There are two main reasons for using bypass capacitors in parallel in the power up circuit. These are:

- To maintain supply voltage to be equal to the pre-defined output if the input becomes less than the corresponding pre-defined output voltage.
- Decoupling capacitors are used to decouple the possible high frequency variation coupled at the output pin of linear voltage regulators

6.2 Clock Circuit

There are four dedicated clock pins in the Cyclone I FPGA IC, namely CLK_0 , CLK_1 , CLK_2 and CLK_3 . We use only one of them ie CLK_0 for our use and feed it with 24 MHz sharp low jitter LVCMOS clock signal. Even though the CLK_0 and CLK_1 pins are of LVDS technology (ie of differential clock technology), the FPGA IC is compatible with single ended clock signal

(ie LVCMOS technology) also. It can be made possible by connecting the CLK_1 pin (17th pin of Altera Cyclone EP1C3) to ground and giving the generated single ended clock signal to the CLK_0 pin (16th pin of Altera Cyclone EP1C3). We have to make the other two clock pins ie CLK_2 and CLK_3 (92nd and 93rd pins of Altera Cyclone EP1C3 respectively)[13]. We used SIT9102AI 243N25E200 for external clock generation and an inverter

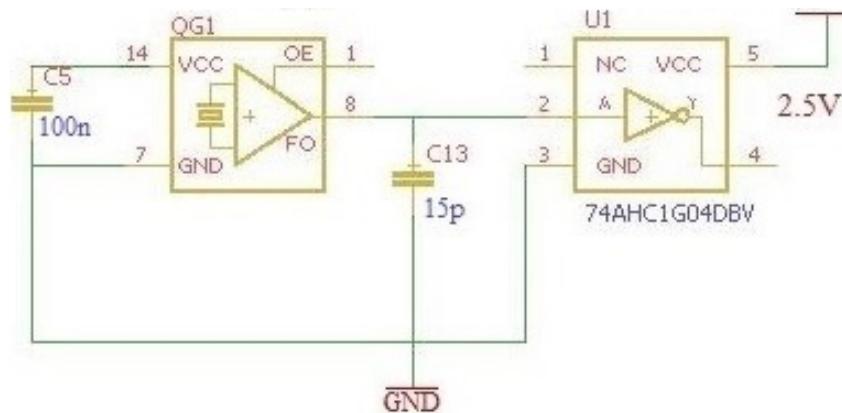


Figure 6.5: External clock

6.3 GPIO circuitry

FPGA altera cyclone-1 IC has around 60 General Purpose Input/Output pins out of which 56 pins are used for our purpose. The board designed customly so as to include 56 pin headers for GPIO use. There are four I/O banks in FPGA altera cyclone-1EP1C3T144C8N which can be independently powered up using 3.3V, 2.5V, 1.8V or 1.5V.



Figure 6.6: GPIO circuitry

The I/O pins are available in both differential and single ended standards, but we make use of only single ended standard which works on 3.3V supply. The advantage of using 3.3V supply is that it can accept input voltages in the range from 2.5V to 5V and the power loss during level conversion from usual 5V standards in outer circuits to I/O voltage standard of FPGA will be minimal compared to the 2.5V and 1.8V cases.

6.4 JTAG circuitry

All Cyclone devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. The JTAG pins support 1.5-V/1.8-V or 2.5V/3.3-V I/O standards.

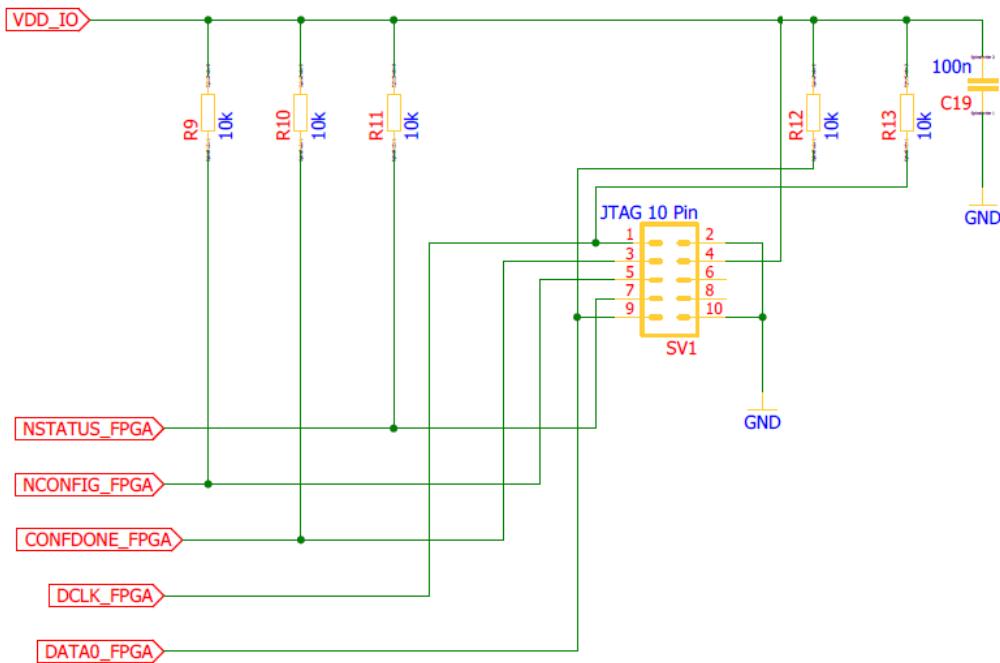


Figure 6.7: JTAG circuitry

We make use of the same supply voltage as that of the GPIO circuitry. JTAG circuitry is used to program the FPGA IC of our board and can be made use to check the FPGA IC in the board.

6.5 Schematic

The schematic was designed solely keeping in mind the object of the project. The power supply, clock circuit, FPGA interfacing and JTAG circuitry was sequentially designed in order. Only if supply voltage is designed first, FPGA board and the remaining parts of the circuit can be powered.

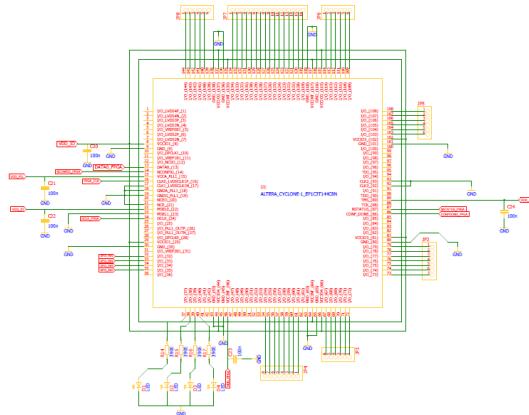
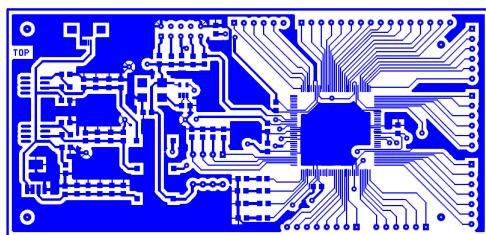


Figure 6.8: Schematic of the FPGA Board

6.6 Layout

This is the top layout of the self designed FPGA board.



Given below is the bottom layout of the self designed FPGA Board.

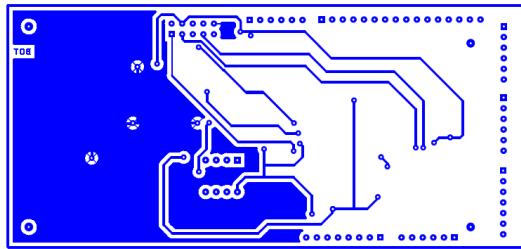


Figure 6.9: Bottom layout

6.7 FPGA Fabrication cost

FPGA Board Cost				
TOTAL no of boards	Layout Design Cost per board(One time cost)	Fabrication Set-up cost(One time)	Board Fabrication Cost per Board	Total cost per Board
1	750	2500	4500	7750
3	750	2500	4500	5433
10	750	2500	4500	4325
>10	750	2500	4500	4045 to 3782
>100	750	2500	3500	< 3532.5

Chapter 7

Conclusion

Studied and acquired three of the main bio signals used in medical diagnosis i.e EMG, ECG, EEG. For EMG signal the moving average value was used to detect muscle fatigue. Using the EEG signal, blinking was detected based on sample value and kurtosis value. And from the ECG Signal Arrhythmia detection was done. Real time acquisition of EMG and ECG signals were done and processed with the Spartan FPGA board. We also designed an FPGA board as per our purpose with external clock, power circuitry, JTAG programmable hardware and GPIO was designed.

The simultaneous processing of the signals shows the flexibility of FPGA boards. It shows that FPGA boards can be designed to meet specific needs not only in medicine but in other fields also. This also reduces the cost of medical equipments thereby reducing the diagnosis cost for patients. Therefore FPGA boards can be the future for applications where simultaneous multi-signal processing is involved.

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