OP AMP Design Project (EE5310)

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1 Problem Statement

Design a two-stage opamp with Miller compensation (dominant-pole), which should be used to make a non-inverting amplifier of gain 2 and a closed-loop -3dB bandwidth of $f_b = 5MHz$ when loaded with a parallel impedance of a resistor $R_L = 2.5k\Omega$ and capacitor $C_L = 10pF$. The phase margin of the closed loop circuit should be 60^o. Minimize the value of Miller capacitors in all loops. Use zero cancelling resistors in series with miller capacitors.

2 Circuit Diagram and Design

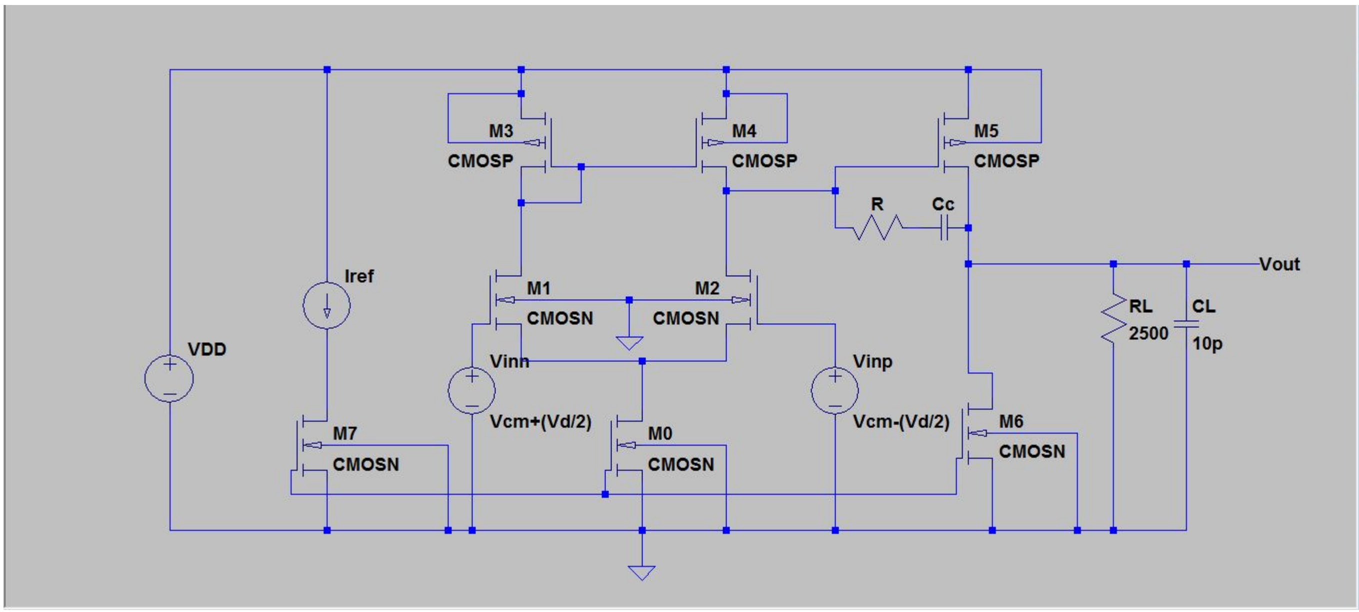

Figure 1: Two-stage opamp with Miller compensation

2.1 Q-1 Circuit Design

The desired phase margin is 60^o. i.e.

$$tan^{-1}(\frac{\omega_u}{\omega_{p1}}) + tan^{-1}(\frac{\omega_u}{\omega_{p2}}) + tan^{-1}(\frac{\omega_u}{\omega_{p3}}) = 120^o \tag{1}$$

Assuming that $\omega_u >> \omega_{p1}$ and $\omega_u << \omega_{p3}$, (1) becomes,

$$tan^{-1}(\frac{\omega_u}{\omega_{p2}}) = 30^o \tag{2}$$

Put $\omega_u = \frac{Gm_1}{2C}$ and $\omega_{p2} = \frac{Gm_2}{C_L}$ in (2).

$$tan^{-1}(\frac{Gm_1/2C}{Gm_2/C_L}) = 30^o \tag{3}$$

Assuming that $Gm_1/Gm_2 = 1/10.8$, we get
$C = 0.08C_L = 0.8pF$

. Assuming a slew rate (SR) of about $20V/\mu s$, the tail current is approximately,

$$I_o = SR \times C = 16\mu A \tag{4}$$

Given, $I_{ref} = I_0/10 = 1.6\mu A$. Now we start for designing the W/L ratios of all the transistors.

$$Gain \times Bandwidth = \frac{Gm_1}{2C} \tag{5}$$

Gm1=0.10048mA/V. Then,

$$(W/L)_1 = \frac{gm_1^2}{2I_{D1}\mu_n C_{ox}} = 15.86 \tag{6}$$

Similarly, $(W/L)_2 = 15.86$

Now we define an input common mode range (ICMR) for the differential amplifier. As an initial guess we assume,

$$ICMR = \{0.8, 1.6\}. \tag{7}$$

Now applying the condition for the transistor M1 to be in saturation at the triode limit,

$$V_{DM1} = V_{GM1} - V_{tn} = 1.067V \tag{8}$$

But, $V_{DM1} = V_{GSM3}$

$$V_{SGM3} = V_{tp} + \sqrt{\frac{2I_{D3}}{\mu_p C_{ox}(W/L)_3}} \tag{9}$$

From (9), we get $(W/L)_3 = 16/3$. As M_4 also need to conduct the same amount of current as M_3, $(W/L)_4 = 16/3$.

Take $V_{D0} = 0.307V$.

From the current expression for M_0 transistor,

$$I_{DM0} = \frac{\mu_n C_{ox} W}{2L}(V_{GSM0} - V_{tn})^2 = 16\mu A \tag{10}$$

We get$(W/L)_0 = 106.667$

We had assumed that $G_{m2} = 10.8 \times G_{m1}$. G_{m2} is essentially the transconductance of M_5, g_{m5}.

We have the relation,

$$\frac{g_{m4}}{g_{m5}} = \frac{I_4}{I_5} = \frac{(W/L)_4}{(W/L)_5} \tag{11}$$

From above, we get $(W/L)_5 = 111.11$
By similar approach,

$$\frac{I_0}{I_6} = \frac{(W/L)_0}{(W/L)_6} \tag{12}$$

gives, $(W/L)_6 = 333.33$. Also,

$$\frac{I_0}{I_7} = \frac{(W/L)_0}{(W/L)_7} \tag{13}$$

gives, $(W/L)_7 = 10$.

Transistor	W/L (µm)	W (µm)	Ad = As (μm^2)	P (µm)
M0	106.667	36	12.96	72.72
M1	15.86	5.71	2.0556	12.14
M2	15.86	5.71	2.0556	12.14
M3	5.33	1.92	0.6912	4.56
M4	5.33	1.92	0.6912	4.56
M5	111.11	40	14.4	80.72
M6	333.3	120	43.2	240.72
M7	10	3.6	1.296	7.92

Figure 2: Table of hand design values.

3 Simulation Results

3.1 Q-2.a) Operating Points from Simulation

Transistor	W (µm)	L (µm)	I_D (µA)	$\lvert V_{GS}\rvert - V_t$ (mV)	g_m mA/V	g_{ds} (µS)
M0	38.4	0.36	14.58	30.19	0.966	3.878
M1	5.71	0.36	7.29	125.356	0.116	1.939
M2	5.71	0.36	7.29	125.356	0.116	1.939
M3	1.92	0.36	7.29	248.712	0.0586	1.842
M4	1.92	0.36	7.29	248.712	0.0586	1.842
M5	40	0.36	160.268	246.12	1.302	42.631
M6	120	0.36	45.112	30.04	3.003	11.99
M7	3.84	0.36	1.6	30.04	0.106	0.4256

Figure 3: Operating Points from Simulation (Q 2.a)

3.2 Q-2.b) Value of other components in the design

M7: (W/L) = 10.667 W = 3.84u
$R = (1/G_{m2})R = 920\Omega$ (from hand calculation)
$R = 768\Omega$ (from back calculation of the simulated value of Gm2) $I_{ref} = 1.6\mu A$ (from slew rate calculation)

3.3 Q-2.c) DC Gain of Op amp

2.c.1) DC gain = 45.9dB = 197.24 v/v (from the back substitution of values in 2a)

$$DCGain = \frac{(G_{m1} * G_{m2})}{((gds3 + gds4)(gds5 + gds6 + (1/RL))} = 44.9dB \tag{14}$$

2.c.2) DC gain = 46.823dB = 219.36 v/v (from simulated plot)

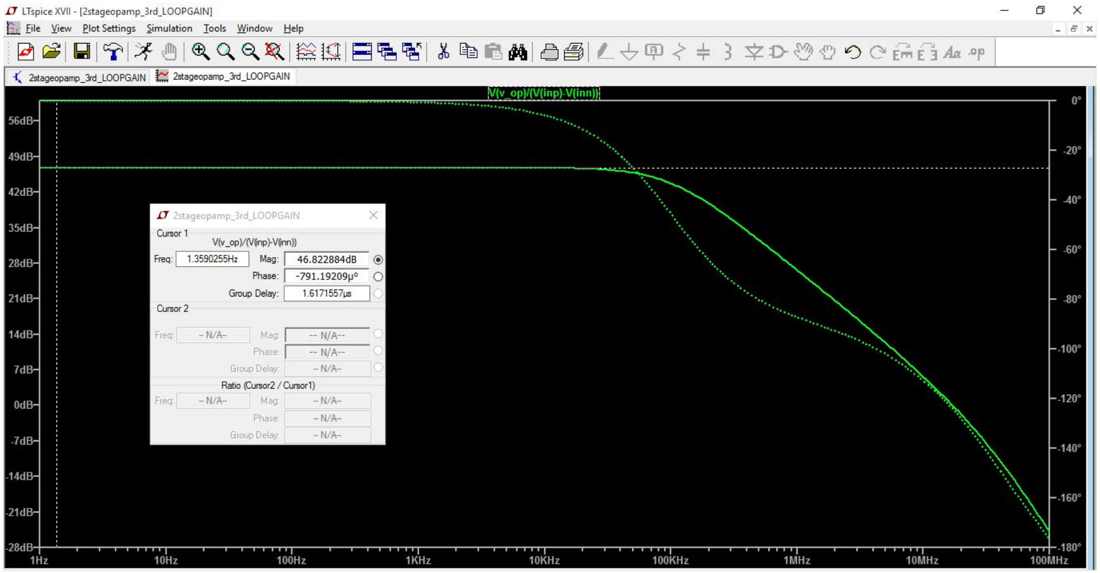

Figure 4: DC gain of the opamp (Q 2.c)

3.4 Q-2.d) Power Consumption

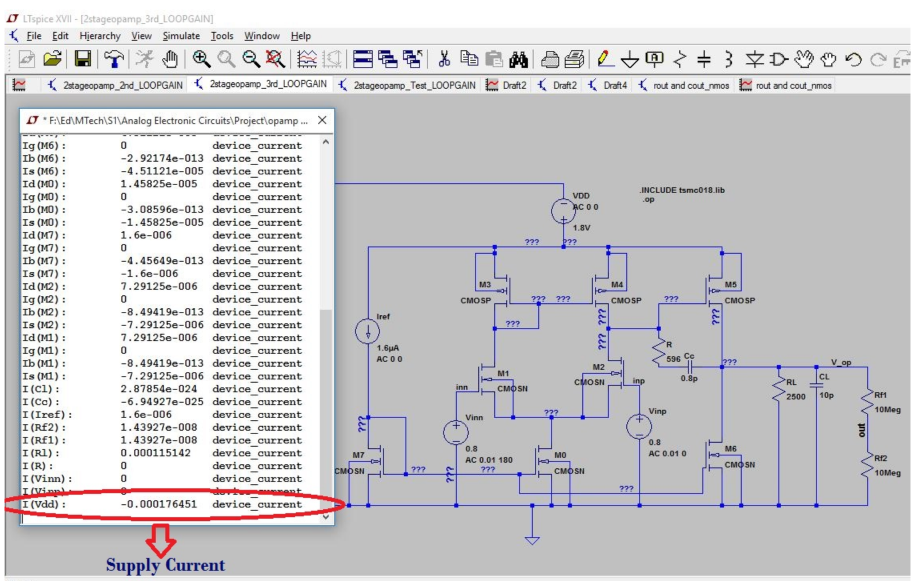

Figure 5: Circuit configuration to check power consumption (Q 2.d)

	Hand Calculated Value	Value obtained from back substitution of data in 2a	Simulated Values
Current drawn from supply (uA)	115.43	176.451	176.451
Power Consumption(uW)	207.774	317.606	317.606

Figure 6: Table for power consumption data (Q 2.d)

3.5 Q-3.a) Loop Gain

3.a.1) Simulated Loop gain (without any parameter indication) Solid line – Indicates Magnitude Dotted Line – Indicates Phase

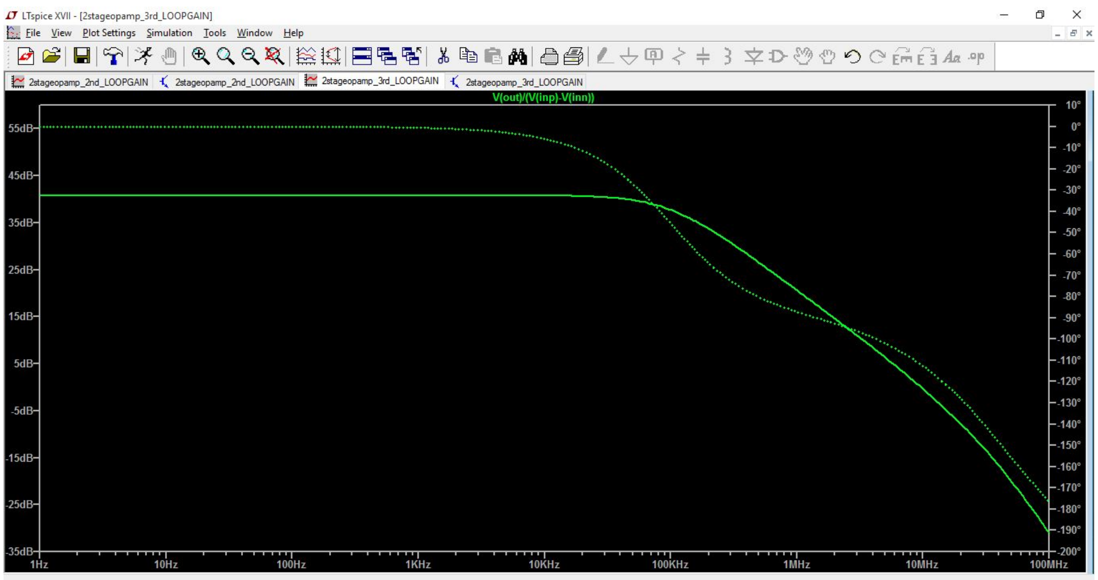

Figure 7: Simulated Loop gain (Q 3.a)

3.a.2) Loop Gain (with PM and unity gain frequency indicated)

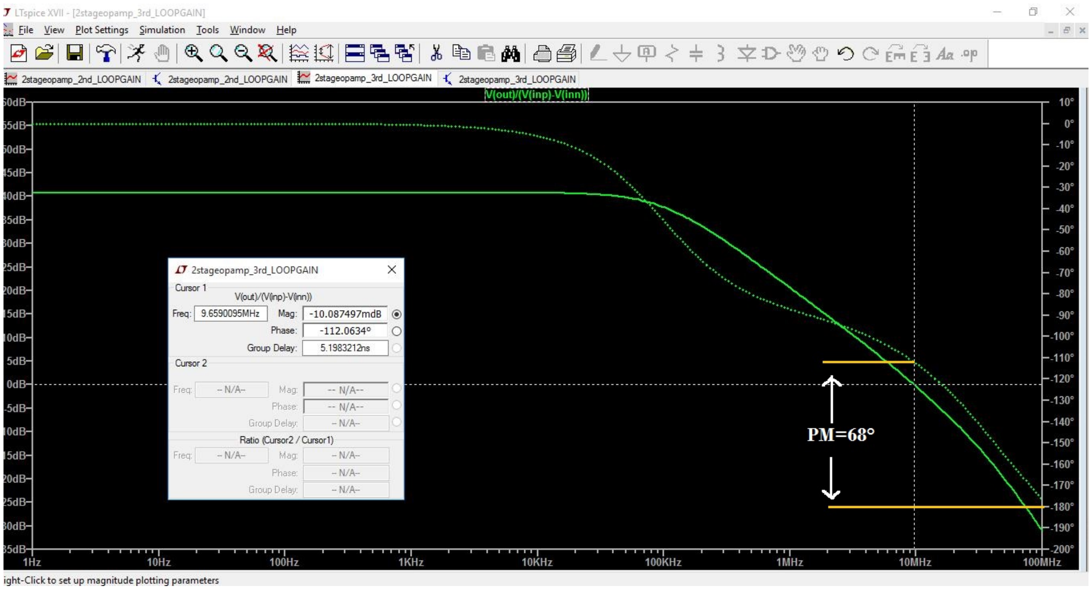

Figure 8: Loop Gain (Q 3.a)

3.6 Q-3.b) Closed Loop Gain

Solid line – Indicates Magnitude
Dotted Line – Indicates Phase
3.b.1) Closed Loop gain (Without any parameters indicated)

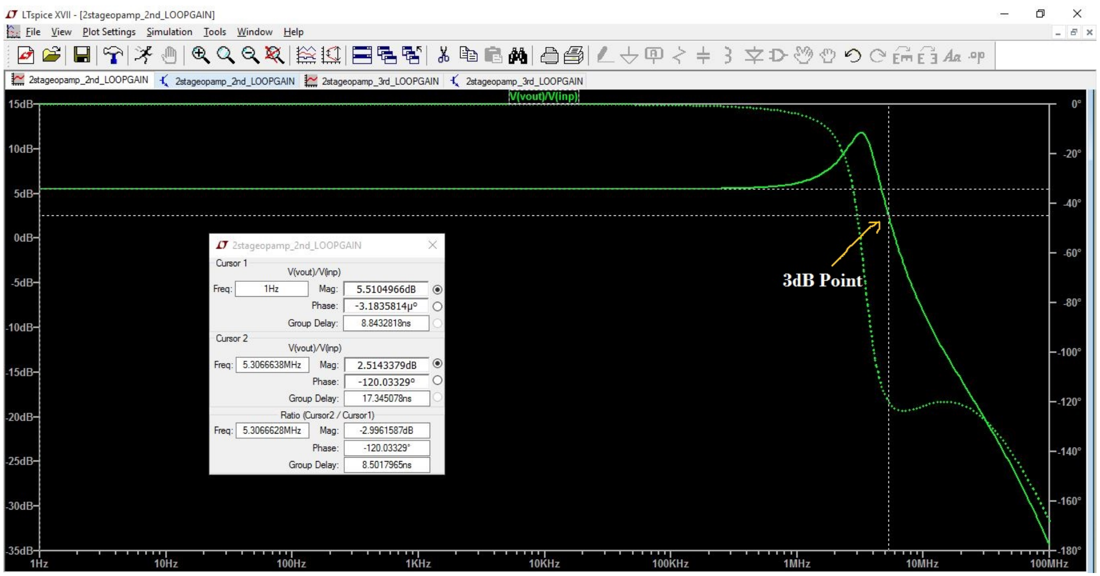

Figure 9: Closed Loop gain (Q 3.b)

3.b.2) Closed Loop Gain (with 3dB Bandwidth and DC gain)
DC Gain = 5.53dB = 1.89v/v 3dB Bandwidth = 5.306MHz

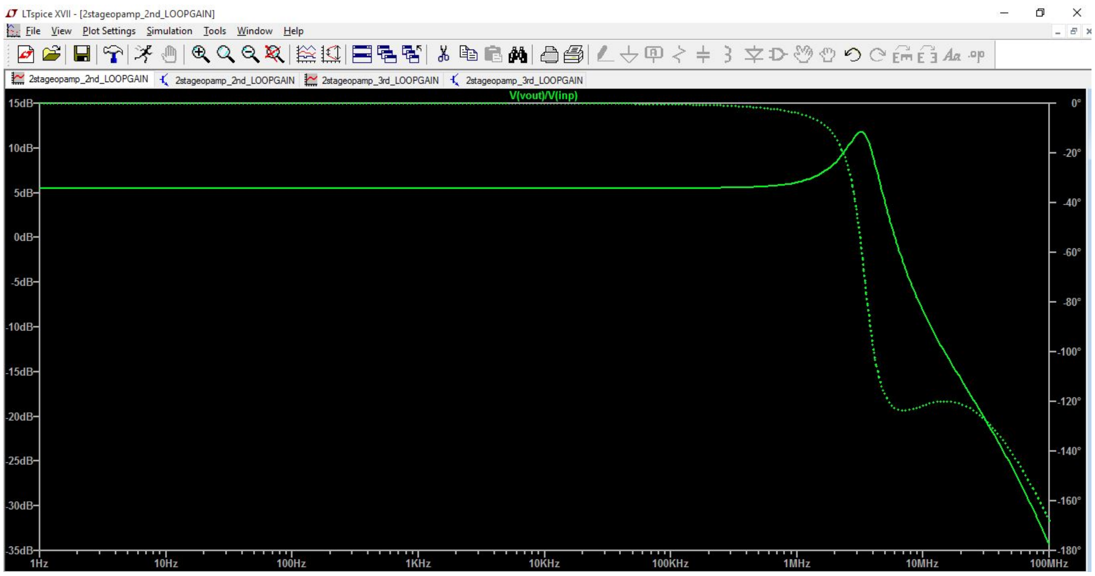

Figure 10: Closed Loop Gain (Q 3.b)

3.7 Q-3.c) Transient response with Differential Step

3.c.1) Rise Transition

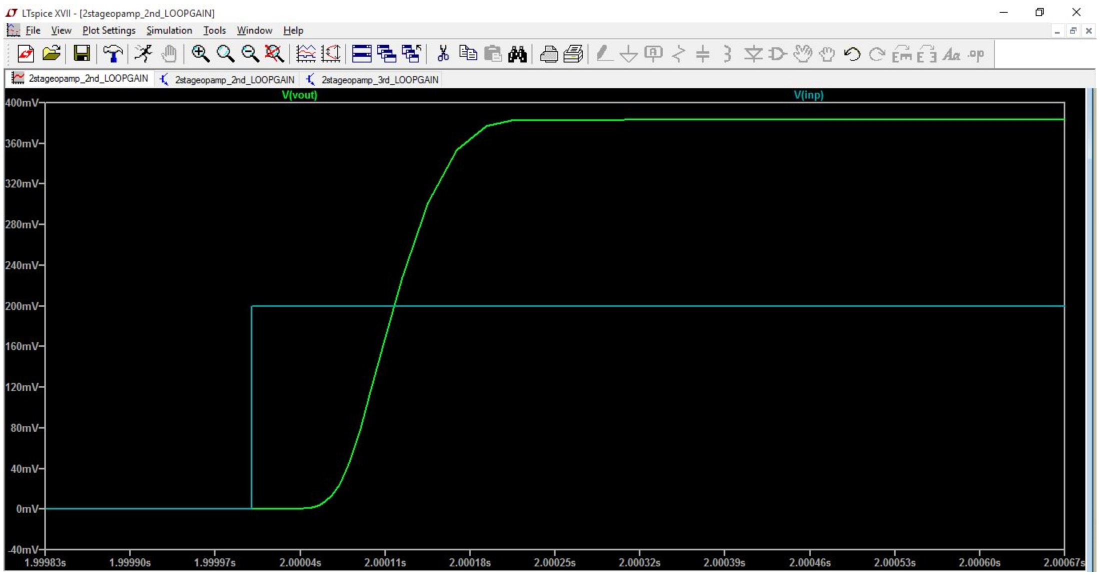

Figure 11: Rise Transition (Q 3.c)

3.c.2) Fall Transition

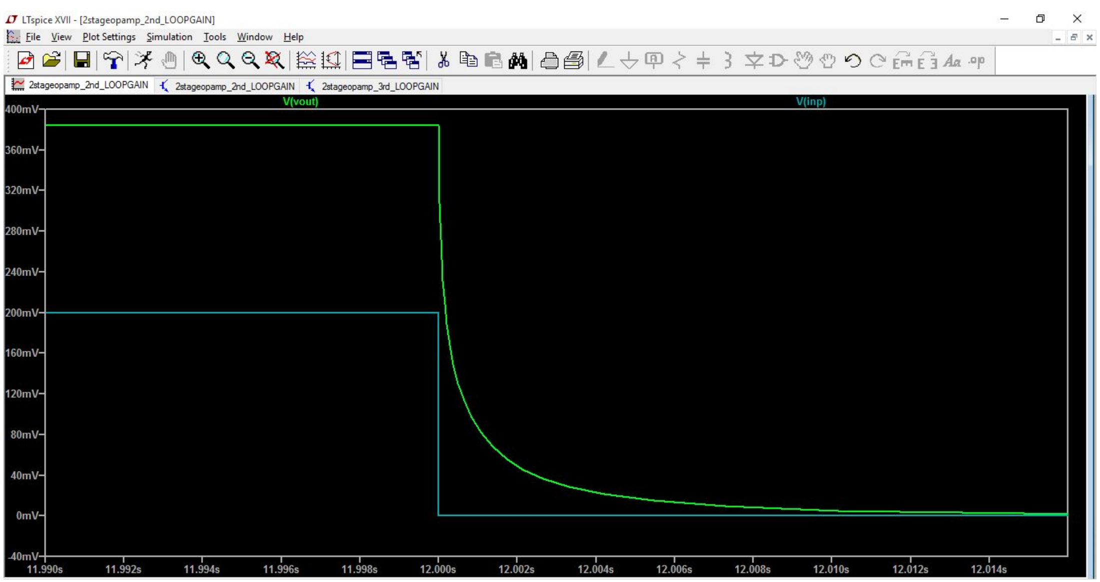

Figure 12: Fall Transition (Q 3.c)