EEE 425
Homework 5

Q1. A full adder is shown in Figure 1. Propagation delays of necessary gates are listed in Table 1.

Answer the following questions:

1. What is the delay of the 1-bit full adder for the S and Cout bits?
2. What is the worst case delay for a 2-bit CRA?
3. What is the worst case delay of a 4-bit CRA?
4. What is the worst case delay of an 8-bit adder if we use the carry bypass architecture with 4-bit units?
5. What is the worst case delay of a 12-bit adder if we use the carry bypass architecture with 4-bit units?

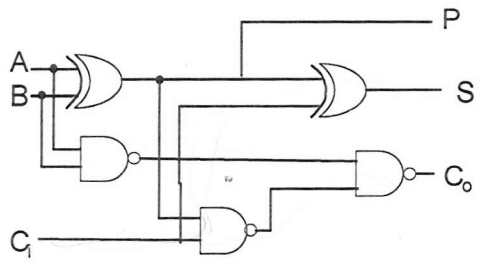


Figure 1

Table 1

Gate	Propagation Delay
NAND2	40ps
XOR	95ps
INV	20ps
2-1 MUX	95ps
NOR2	50ps

(a) $t_S = 95+95 = 190ps$

$t_C = 95+40+40 = 175ps$

(b) $A_0/B_0 \rightarrow C_0 \rightarrow S_1$

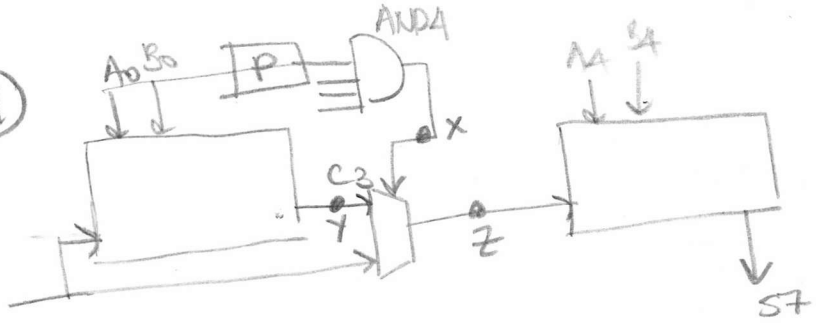
$175+95 = 270ps$

(c) $A_0/B_0 \rightarrow C_0 \rightarrow C_4 \rightarrow C_2 \rightarrow S_3$

175 80 80 95

430ps

(d)



AND4 implement as NAND/NOR 90ps

$A_0B_0 \rightarrow X$ 185ps not critical path

$t_Y = 415ps$

$A_0/B_0 \rightarrow C_0 \rightarrow C_1 \rightarrow C_2 \rightarrow C_3$

175 80 80 80

$t_2 = 510ps$

$t_{total} = 845ps$

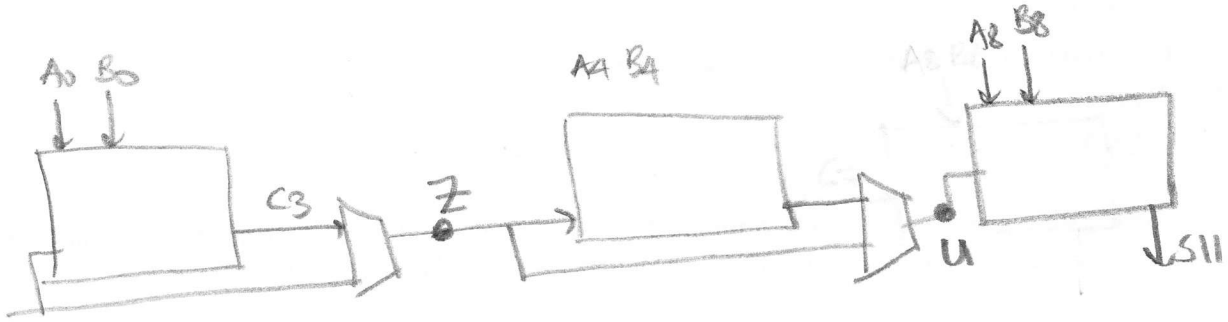
$Z \rightarrow S7$

$C_3' \rightarrow C_4 \rightarrow C_5 \rightarrow C_6 \rightarrow S7$

80 80 80 95

335ps

(e)



$t_Z = 510ps$ $t_U = 605ps$

$U \rightarrow S11$ same as $Z \rightarrow S7$ (in part d) $= 335ps$

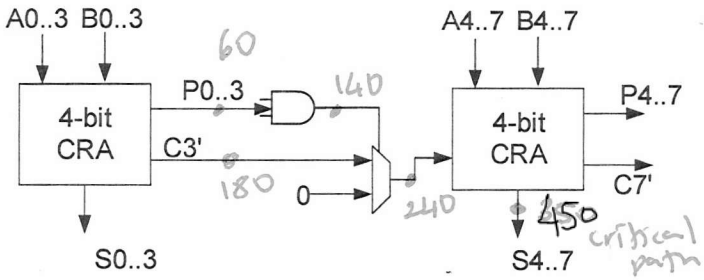
$t_{total} = 940ps$

Q2. The figure shows two 8-bit carry bypass configurations.

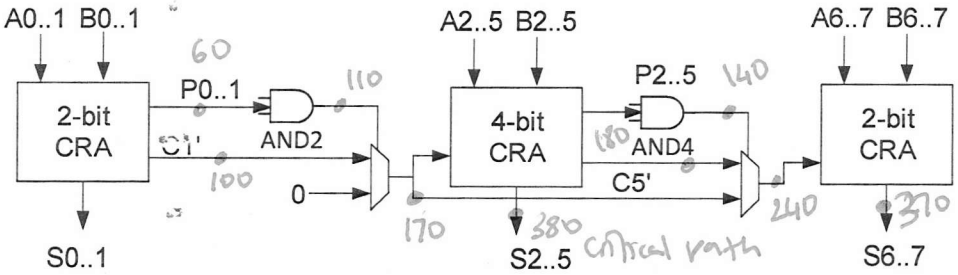
(a) Determine the delay of the 8-bit carry bypass adder given in Figure 2(a)

(b) Determine the delay of the 8-bit carry pass adder given in Figure 2(b)

(c) You are to design a 16-bit adder with the library components given in the table. Determine the configuration with the lowest delay and determine its delay.



(a) 8-bit Carry Bypass with 4-bit CRA blocks



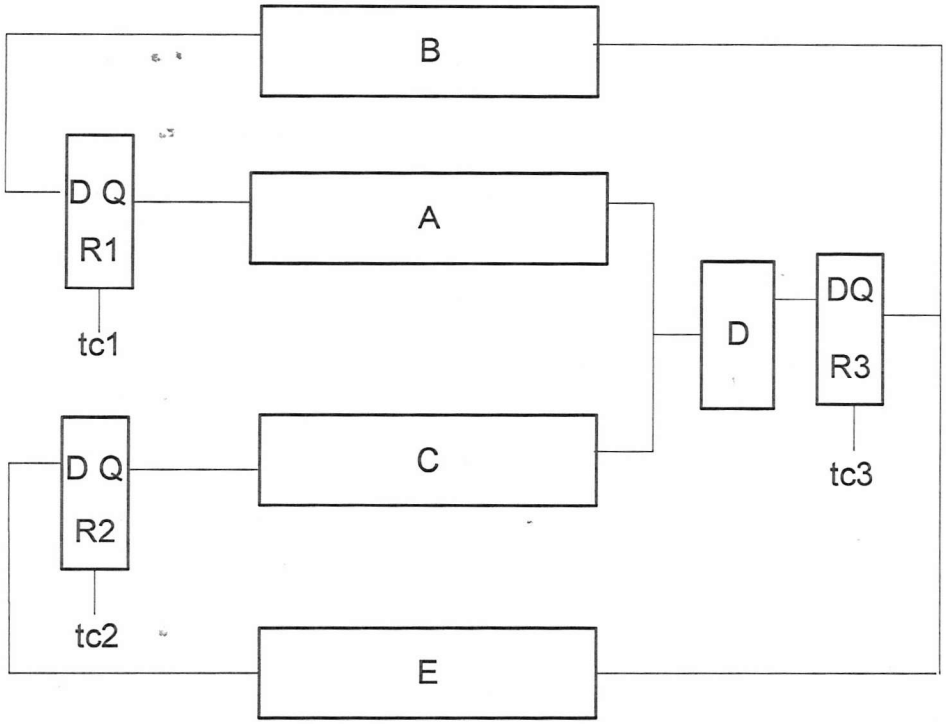
(b) 8-bit Carry Bypass with 2-4-2-bit CRA blocks

Path	Delay
A/B-P	60ps
A/B-Co	60ps
P-S	60ps
Ci-Co	40ps
Ci-S	90ps
MUX	60ps
AND2	50ps
AND4	80ps

Figure 2

Q3 Figure 2 shows a datapath. Registers require 50ps set-up time and 50ps hold time.

(a) Determine minimum clock period under ideal conditions (no skew, no jitter) (5pts).
(b) Determine the maximum clock skew δ_{max} = tc3-tc1 where tc1 and tc2 are in sync (i.e. the clock edge to R3 is delayed compared to clock edge to R1 and R2). Determine the minimum clock period for this skew (10 points).
(c) Determine the maximum clock skew δ_{max} = tc1-tc3 where tc2 and tc1 are in sync (i.e. the clock edge to R1 and R2 is delayed compared to clock edge to R3). Determine the minimum clock period for this skew (10 points).



	Min Delay	Max Delay
R	30ps	50ps
A	100ps	270ps
B	70ps	270ps
C	90ps	200ps
D	20ps	50ps
E	60ps	220ps

Figure 2: Datapath

(a) R1 → R3
T ≥ 50 + 270 + 50 + 50
T ≥ 420ps

(b) tc3 @ ta = tc2
delayed
R3 capture register
R2 → R3
tcd = 30 + 90 + 20 = 140ps
tcd − δ ≥ thold δmax = 90ps

R3 initiation
R3 → R1
T ≥ 50 + 270 + 50 + 90
T ≥ 460ps

(c) $\delta = t_{c1} - t_{c3}$

$t_{c1} = t_{c2}$

R1/R2 capture register

R3 → R2

$t_{cd} = 30 + 60 = 90ps$

$\delta_{max} = 40ps$

For R1 → R3

$T \geq 420 + 40$

$T \geq 460ps$