HW1 Solutions

① Amortized wafer cost

$$= \frac{5000}{0.9} = 5555$$

Dies per wafer

$$N_D = \frac{\pi r^2}{A_D} - \frac{\sqrt{2}\pi r}{\sqrt{A_D}} = 450$$

good dies = $450 \times 0.65 = 292$

⑨ $$IPC = \frac{\frac{5555}{292} + 4^*}{0.85} + \frac{2\times10^6}{4\times10^6}$$

IPC = \$27.59

* If test and packaging cost is taken as \$8, it is fine.

ⓑ IPC reduces by 10% IPC = \$27.49

ⓒ # good dies = $450 \times 0.8 = 360$

$$IPC = \frac{\frac{5555}{360} + 4}{0.85} + 1 = \$23.85$$

better option

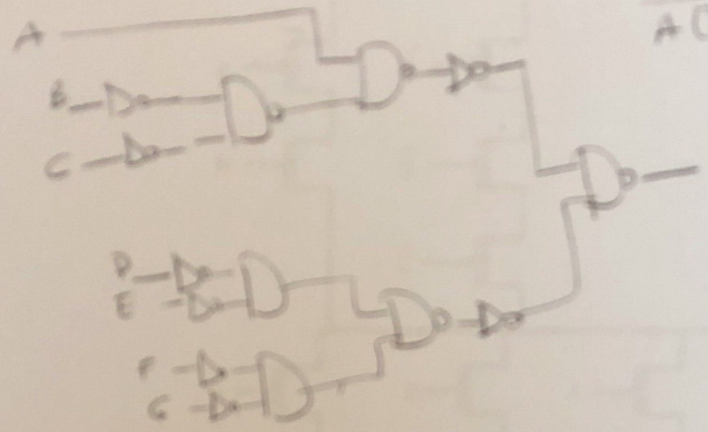
2a $Y = \overline{A \cdot (B+C) \cdot (D+E) \cdot (F+G)}$

mathematical method

$\overline{A(B+C)} + \overline{(D+E)(F+G)}$

$\overline{A}\,\overline{(B+C)} + \overline{(D+E)}\,\overline{(F+G)}$

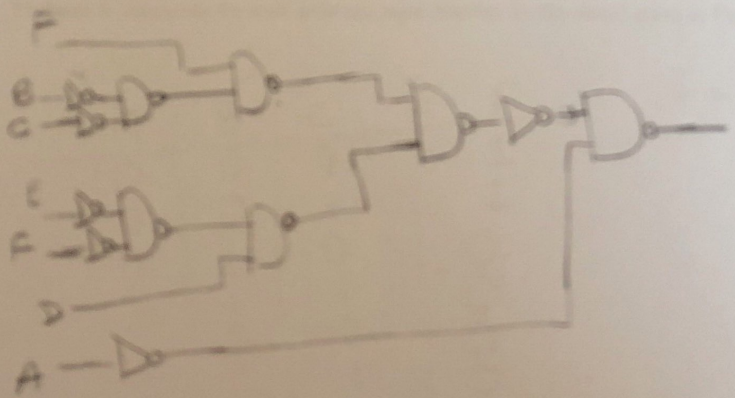
Top level OR implemented as inputs into NAND



b) $Y = A + F(B+C) + D(E+F)$

architectural method

- implement first with 2-input AND/OR gates and replace as you go



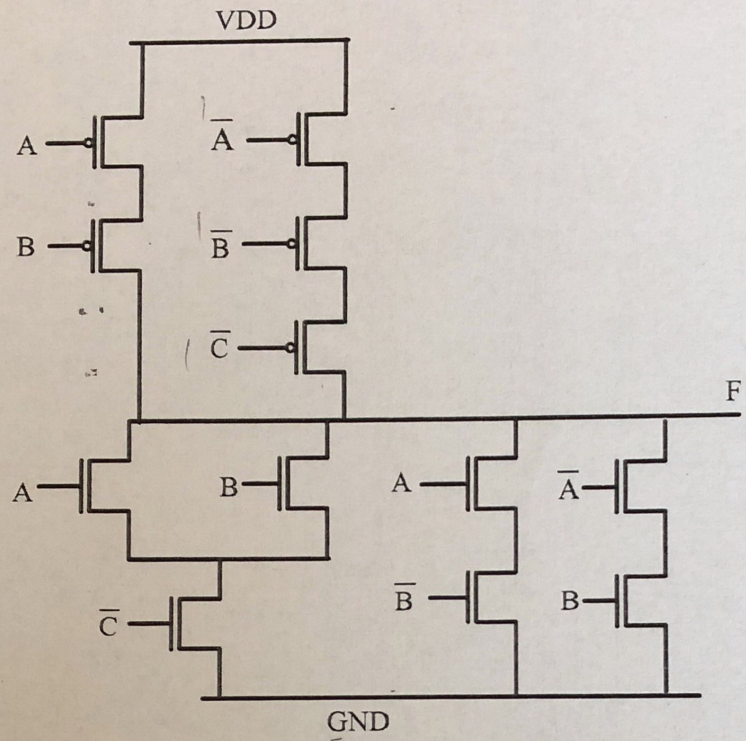


Figure 1: Logic circuit for problem 3

Problem 3. Determine the truth table and logic function for the circuit given in Figure 1.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$F = \overline{A}\,\overline{B} + ABC$