EEE 425/591  
Digital Systems and Circuits  
Homework #1

**Problem 1.** A semiconductor company has the following costs associated with Product X:

* Fixed cost of $200M ($200,000,000)
* Wafer yield of 90%
* Die yield of 65% (65% of dies on a wafer make it to the next level)
* 12-inch wafer manufacturing cost of $5,000 per wafer
* Die size 12mmx12mm
* Testing and packaging cost of $4 per die
* A final test yield of 85%
* Product volume of 400M chips

a) What is the cost per IC (considering both fixed and variable costs)?

b) Suppose that you are a strategic planner for this company and you need to reduce the cost to make profit. Which one is a better strategy? ***The answers should be quantitatively justified to get credit!***

*Strategy 1:* Reduce the fixed operating cost by 20%.

*Strategy 2:* Spend an extra Research and Development cost of $200,000,000 to improve the die yield from 65% to 80%.

**Problem 2.** Implement the following logic functions using only 2-input NAND gates and inverters.

(a)

Y = A·(B+C)·(D+E)·(F+G)

Y = A+F·(B+C) + D·(E+F)

(b)

**Problem 3.** Determine the truth table and logic function for the circuit given in Figure 1.



Figure : Logic circuit for problem 3