EEE 425/591  
Digital Systems and Circuits

Homework #3

Table I: Transistor parameters

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | Vdd = 1.8V | Cu = 1fF (gate, drain, source) |
|  |  |  | Ru=10k |

Q1. You are given the logic function:

The load at the output is 200fF, the input capacitance of a minimum sized inverter is 3fF.

1. Determine the optimum number of stages as if you are designing a buffer (assume the first stage is an inverter)
2. Implement the logic function with the number of stages as close to the number you found in part (a) using standard static logic gates (NAND, NOR, INV) of any fan-in.
3. Size the gates in the critical path to optimize delay.
4. Determine the optimized delay
5. Determine an input switching pattern that would exercise the critical path.

Q2. A logic circuit is given in Figure 1. For this technology, the minimum sized inverter has 3fF of input capacitance.

1. Determine the delay from the input to X and Z assuming all gates are minimum sized.
2. Size the gates to minimize the delay **of the critical path** (only the critical path will be sized).
3. Determine the delay of both paths again.



Figure 1: Logic circuit