Freescale Semiconductor
Application Note

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Programming Audio Applications in the i.MX21

MC9328MX21

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1 Abstract

The MC9328MX21 (i.MX21) processor has two dedicated peripherals for audio applications: Serial Synchronous Interface (SSI) and Digital Audio MUX (AUDMUX). A brief description of these two peripherals follows:

Synchronous Serial Interfaces (SSI):

- Supports generic SSI interfaces for time-slot based communication with synchronous voice codecs
- Time-slot mode supports up to 4 channels for communication among devices Bluetooth voice port, voice codecs, and baseband audio ports
- Supports Philips standard Inter-IC Sound (I^2S) bus for external digital audio chip interface at 44.1 kHz and 48 kHz
- AC'97 Host Controller mode with support for 2 audio channels supporting fixed and variable rate transfers
- Used in conjunction with the Digital Audio Mux (AUDMUX) module to provide flexible audio and voice routing options

Contents

Digital Audio Mux (AUDMUX):

- Supports 2 internal hosts, 1 external host, and 3 external peripheral interfaces
- Flexible audio, voice, and data routing without host processor intervention
- Built-in support for network mode connection of host and peripheral interfaces
- Separate and simultaneous audio paths from hosts to peripherals
- External 4-wire connection to synchronous devices, audio, and voice codecs

In this application note, typical scenarios of audio applications will be discussed. The use of SSI and AUDUMX in these audio applications will also be examined.

2 SSI and AUDMUX Port Arrangement

The i.MX21 processor has two SSI modules. Each SSI module is capable of supporting synchronous (4-wire) or asynchronous (6-wire) serial communication. The AUDMUX, has two internal host ports, one external host port, and three external peripheral ports. The Host Port 1 (HP1) and Host Port 2 (HP2) are connected to the internal SSI1 and SSI2 respectively. The Host Port 3 (HP3) is mapped to the i.MX21 external SAP I/O port. The Peripheral Port 1 (PP1), Peripheral Port 2 (PP2), and Peripheral Port 3 (PP3) are mapped to the i.MX21processor's external SSI1 I/O port, external SSI2 I/O port, and external SSI3 I/O port respectively. Figure 1 illustrates this arrangement.

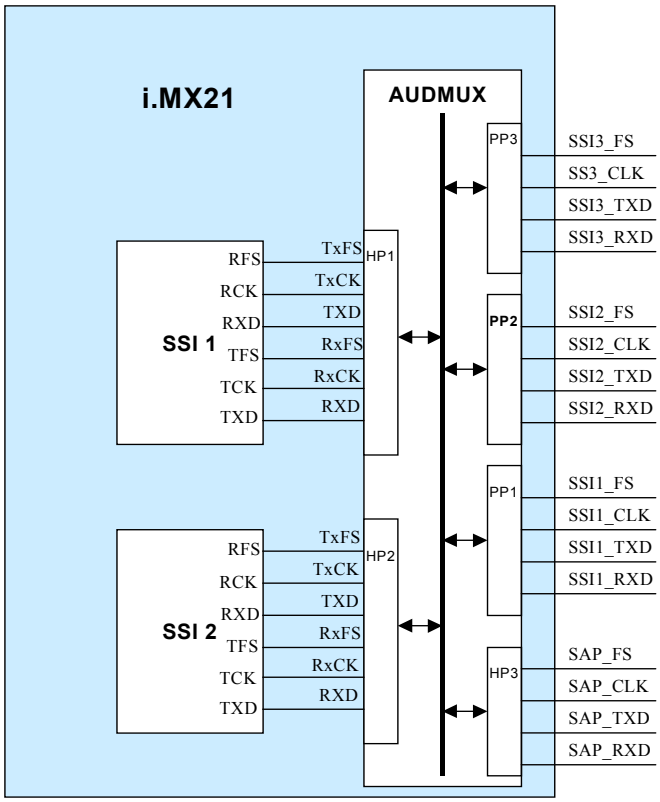

Figure 1. i.MX21 SSI and AUDMUX Port Arrangements

3 Audio Application Scenarios

3.1 Interfacing with an Audio Codec

A typical audio application scenario is to playback and record audio via an external codec. The codec can be configured as the SSI master which provides the bit clock and frame sync to the i.MX21 processor's SSI. Since i.MX21 is capable of performing full-duplex operation (record and playback) at different sampling rates, the i.MX21 SSI needs to be programmed as an asynchronous SSI slave mode. Figure 2 shows the connection between i.MX21 and an external codec. Note that two I/O ports (SSI2 and SSI3 in this example) are required to perform the asynchronous operation.

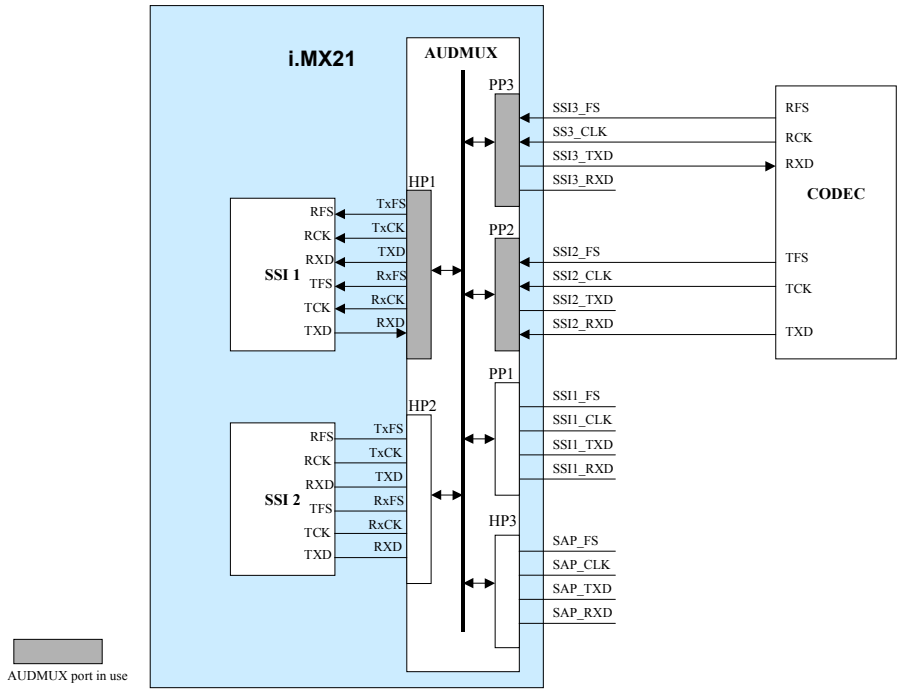

Figure 2. i.MX21 and Audio Codec Connection Example

Given the configuration shown in Figure 2, set the corresponding AUDMUX ports as indicated in Table 1 through Table 3.

Table 1. Host Port Configuration Register 1 (HPCR1 - $10016000)

Name	Settings	Comments
TFSDIR	1	TxFS is output
TCLKDIR	1	TxCLK is output
TFCSEL	4	TxFS and TxCLK from Peripheral Port 2
RFSDIR	1	RxFS is output
RCLKDIR	1	RxCLK is output
RFCSEL	5	RxFS and RxCLK from Peripheral Port 3
RXDSEL	4	Receive data from Peripheral Port 2

Table 1. Host Port Configuration Register 1 (HPCR1 - $10016000) (continued)

Name	Settings	Comments
SYN	0	Asyn Mode
TXRXEN	0	No switch
INMEN	0	Disable
INMASK	0	Ignore when INMEN = 0

Table 2. Peripheral Port Configuration Register 2 (PPCR2 - $10016014)

Name	Settings	Comments
TFSDIR	0	TxFS is input
TCLKDIR	0	TxCLK is input
TFCSEL	0	Ignore when TxFS/TxCLK are input
RFSDIR	0	Ignore
RCLKDIR	0	Ignore
RFCSEL	0	Ignore
RXDSEL	0	Ignore
SYN	1	Syn mode
TXRXEN	0	No switch

Table 3. Peripheral Port Configuration Register 3 (PPCR3 - $10016018)

Name	Settings	Comments
TFSDIR	0	TxFS is input
TCLKDIR	0	TxCLK is input
TFCSEL	0	Ignore when TxFS/TxCLK are input
RFSDIR	0	Ignore
RCLKDIR	0	Ignore
RFCSEL	0	Ignore
RXDSEL	0	Receive from Host Port 1
SYN	1	Syn mode
TXRXEN	0	No switch

3.2 Interfacing with an AC’97 Codec

When connecting i.MX21 with an AC’97 codec, the external AC’97 typically will provide the serial bit clock (12.288 MHz) to the i.MX21 SSI. Based on this serial bit clock, i.MX21 will generate the appropriate frame sync to the AC’97 codec and the SSI will be configured as an SSI synchronous slave operation. Figure 3 shows the connection between i.MX21 and an AC’97 codec.

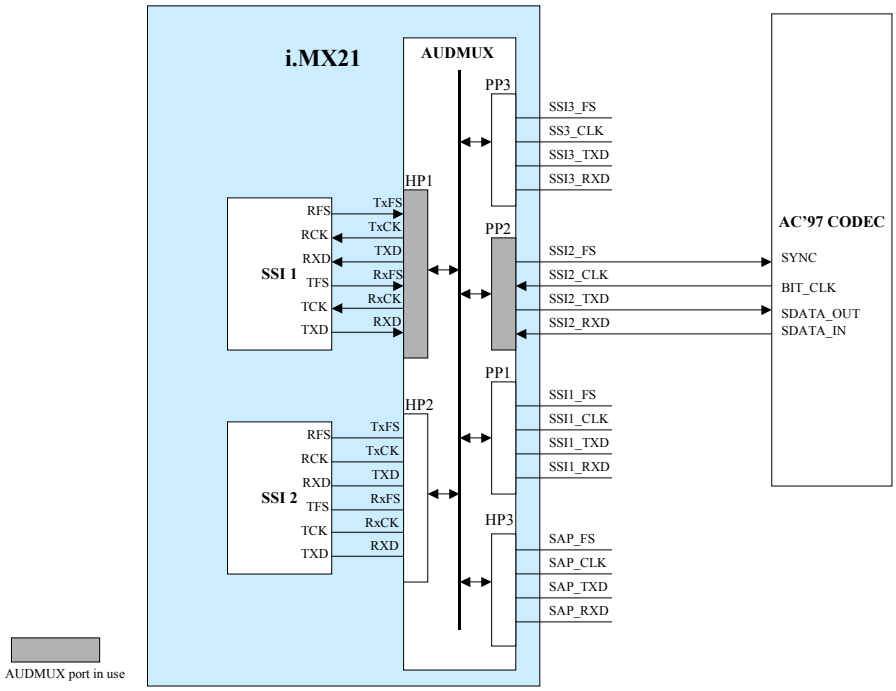

Figure 3. i.MX21 and AC'97 Codec Connection Example

Given the configuration shown in Figure 3, set the set the corresponding AUDMUX ports as indicated in Table 4 and Table 5.

Table 4. Host Port Configuration Register 1 (HPCR1 - $10016000)

Name	Settings	Comments
TFSDIR	0	TxFS is input
TCLKDIR	1	TxCLK is output
TFCSEL	4	TxFS and TxCLK from Peripheral Port 2
RFSDIR	0	Ignore
RCLKDIR	0	Ignore
RFCSEL	0	Ignore
RXDSEL	4	Receive data from Peripheral Port 2
SYN	1	Syn Mode
TXRXEN	0	No switch
INMEN	0	Disable
INMASK	0	Ignore when INMEN = 0

Table 5. Peripheral Port Configuration Register 2 (PPCR2 - $10016014)

Name	Settings	Comments
TFSDIR	1	TxFS is output
TCLKDIR	0	TxCLK is input
TFCSEL	0	TxCLK/TxFS from Host Port 1
RFSDIR	0	Ignore
RCLKDIR	0	Ignore
RFCSEL	0	Ignore
RXDSEL	0	Receive from Host Port 1
SYN	1	Syn mode
TXRXEN	0	No switch

3.3 Interfacing i.MX21 to a Baseband Processor, Codec, and Bluetooth

In Bluetooth smartphone applications, the i.MX21 need to connect with an audio codec, a modem Baseband Serial Audio Port (SAP) and the Bluetooth chipset SSI port. To enable the seamless interface for various audio connections, The i.MX21 AUDMUX port plays a very important role. With the audio codec connection described in Section 3.1, a Bluetooth smartphone configuration is illustrated in Figure 4. Different voice paths in this Bluetooth smartphone system will be discussed individually.

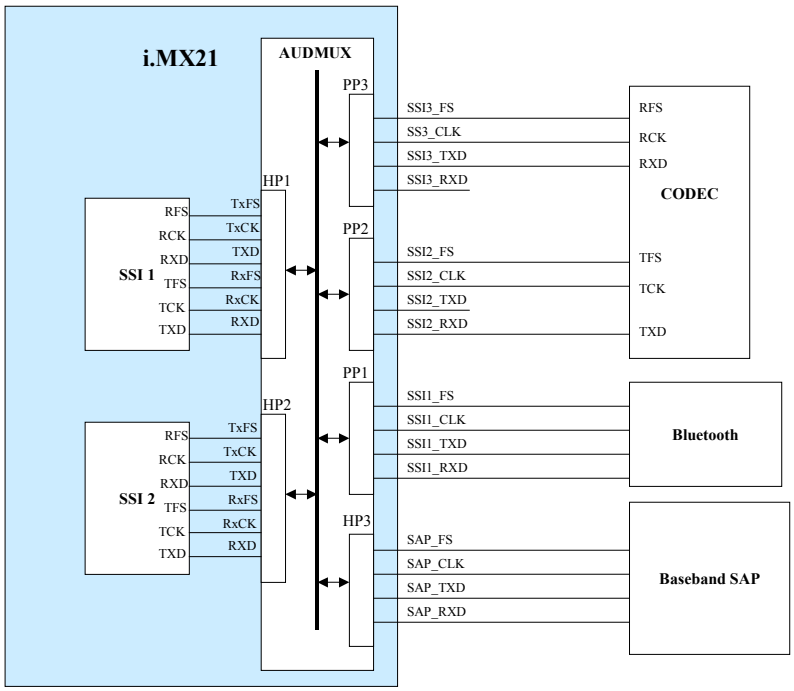

Figure 4. Bluetooth Smartphone Connection Example

3.3.1 Voice Path Between Modem SAP and Bluetooth

In the scenario of the smartphone being a Bluetooth audio gateway connecting with a remote Bluetooth headset, the voice path must be established directly between the Baseband SAP and the Bluetooth SSI. In this case, the Baseband SAP will be the SSI master that provides the SSI frame sync and clock to the Bluetooth SSI.

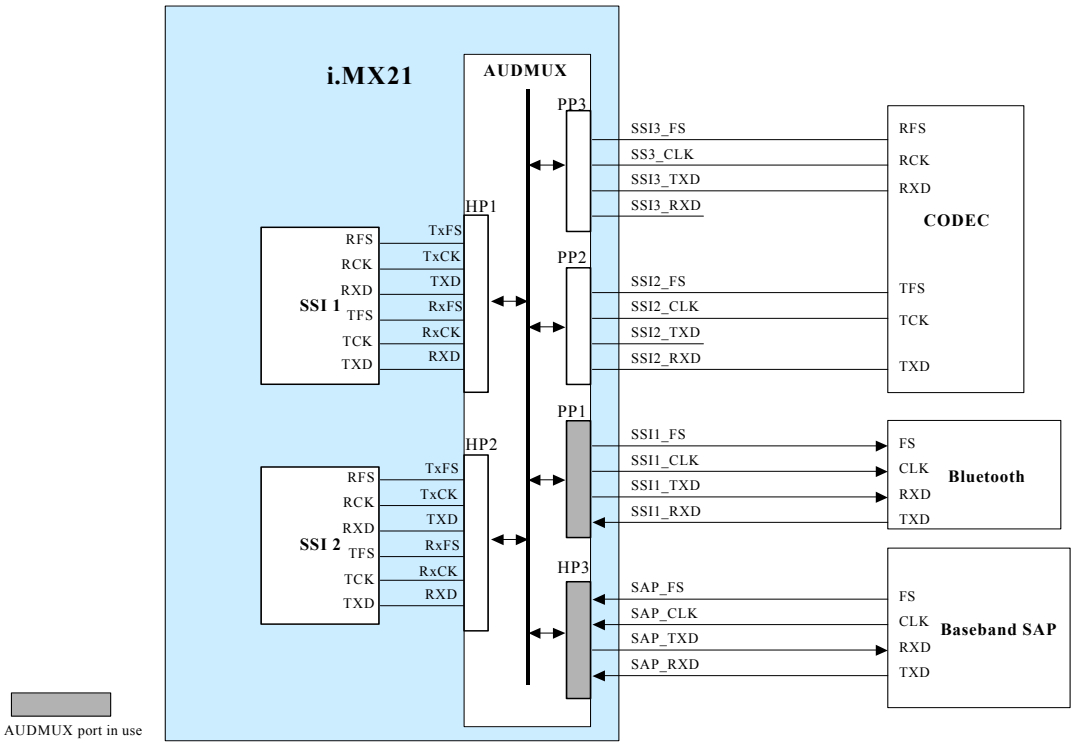

Figure 5. Voice Path Between Baseband SAP and Bluetooth

3.3.2 Voice Path Between i.MX21 and Bluetooth

When the i.MX21 is setup as an SCO voice link with the remote Bluetooth device, the i.MX21 SSI 2 will be the SSI master while the Bluetooth will be the SSI slave. This is illustrated in Figure 6.

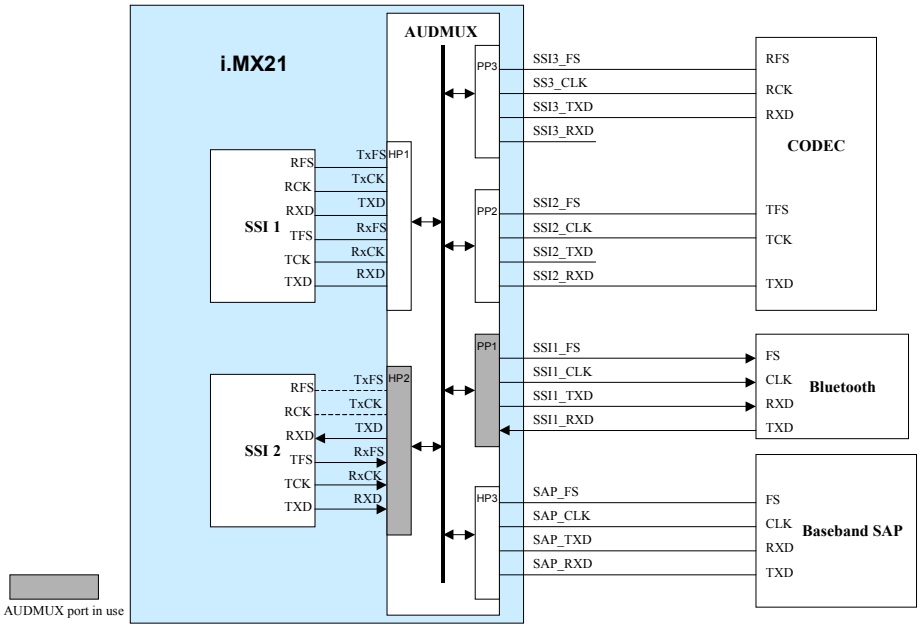

Figure 6. Voice Path Between i.MX21 and Bluetooth

3.3.3 Voice Path Between i.MX21 and Baseband

There will be scenarios (such as voice memo recording and voice recognition) involving the voice path between the i.MX21 and the Baseband. In this case, the Baseband will be the SSI master while the i.MX21 will be the SSI slave. This scenario is illustrated in Figure 8.

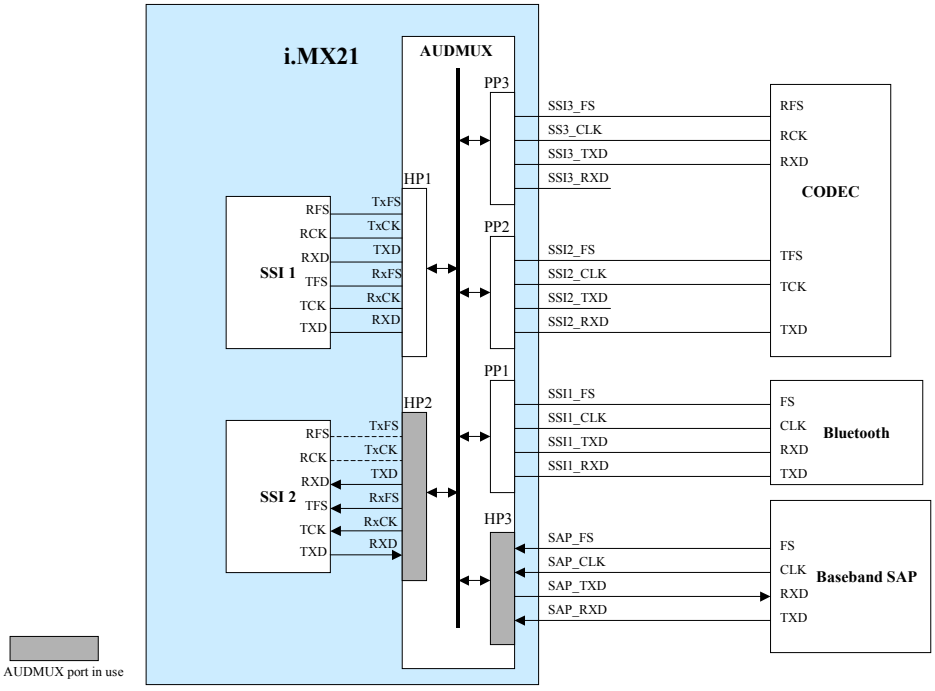

Figure 7. Voice Path Between i.MX21 and Baseband

3.4 Tx/Rx Switching

In a typical SSI network mode configuration, only one of the devices will be the master which provides frame sync and clocks. Other devices will act as the SSI slaves. Since the hardware connections are being fixed, it is not possible to perform an on-the-fly master/slave role change. However, the i.MX21 AUDMUX provides a Tx/Rx switching mechanism to support this.

Figure 8 shows a SSI network connection of 3 devices. Device 1 acts as the SSI master while Device 2 and the i.MX21 act as SSI slaves. The SAP_TXD pin is an output pin from i.MX21 to Device 1. During the allocated time slot, i.MX21 will provide data to Device 1. In other time slots, i.MX21 SAP_TXD will be tri-stated. Similarly, the SAP_RXD pin is an input pin such that time slot data from Device 1 can be sent to i.MX21.

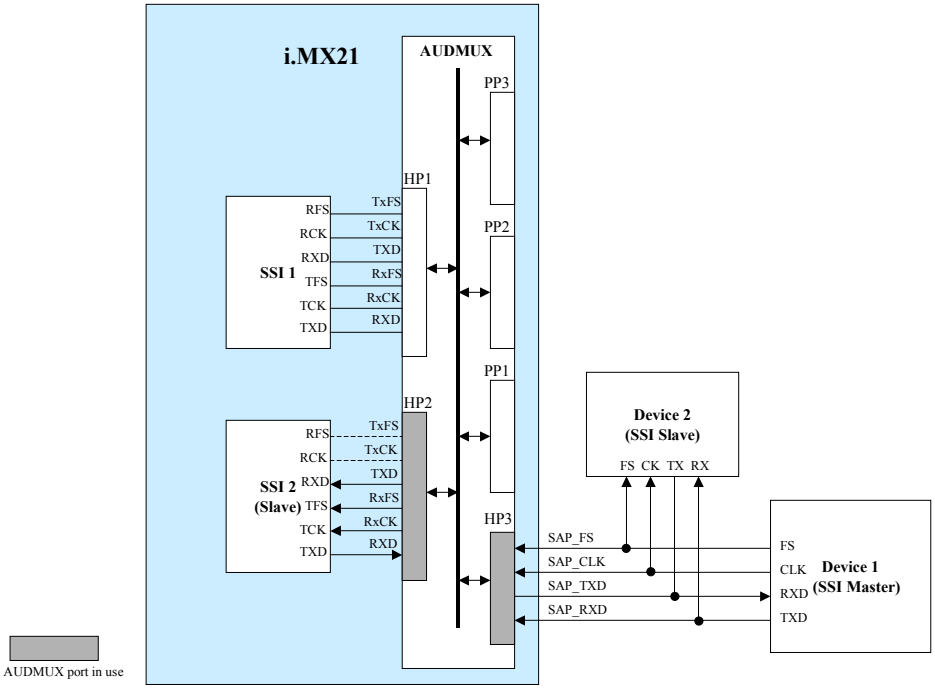

Figure 8. SSI Network Mode with 3 Devices

When the i.MX21 is set to become the SSI master and Device 1 is no longer active, i.MX21 needs to provide the frame sync and clocks to Device 2. Additionally, since the hardware connection is being fixed, i.MX21 needs to send data from the SAP_RXD pin to the RX pin of Device 2 and receive data from TX pin of Device 2 to SAP_TXD. With the help of the Tx/Rx switching feature, the role switching can be performed easily.

As indicated in Figure 9, the Tx/Rx switching is enabled at Host Port 3 (HPCR3:TXRXEN = 1). The SAP_TXD pin now becomes an input pin (previously it is an output pin) which can receive data from Device 2 TX pin. Similarly, the SAP_RXD pin now becomes an output pin (previously it is an input pin) which can send data out to Device 2 RX pin.

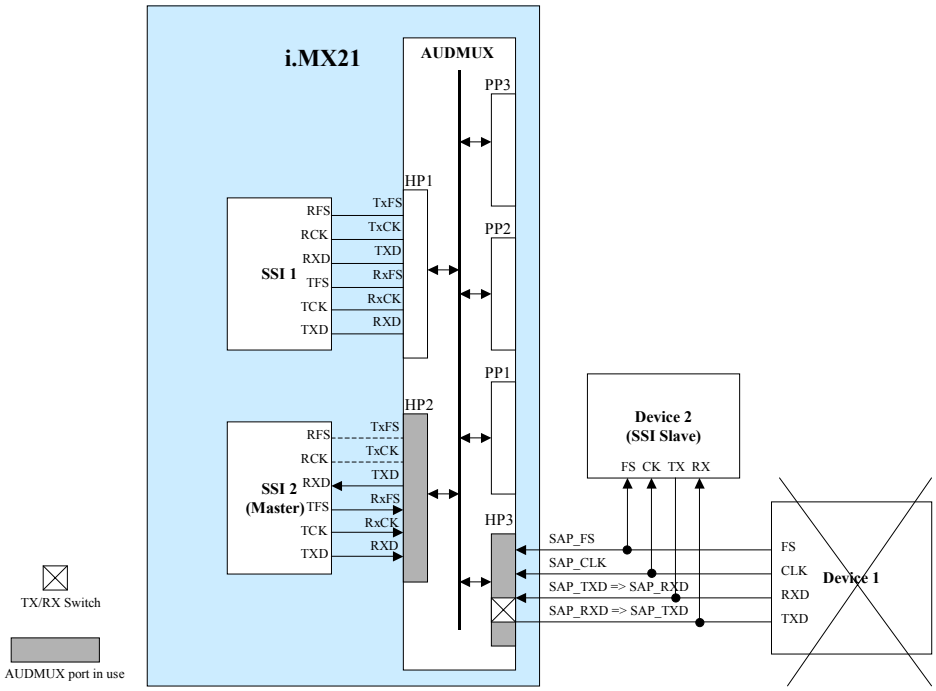

Figure 9. Tx/Rx Switching a Host Port 3

3.5 Internal Network Mode

Network mode is where a master SSI is connected to more than one slave SSI device. The communication occurs in a time-slotted frame. In the internal network mode, the AUDMUX host port can receive the signals from i.MX21 internal SSI ports or external ports. These received signals are ANDed together to form the output.

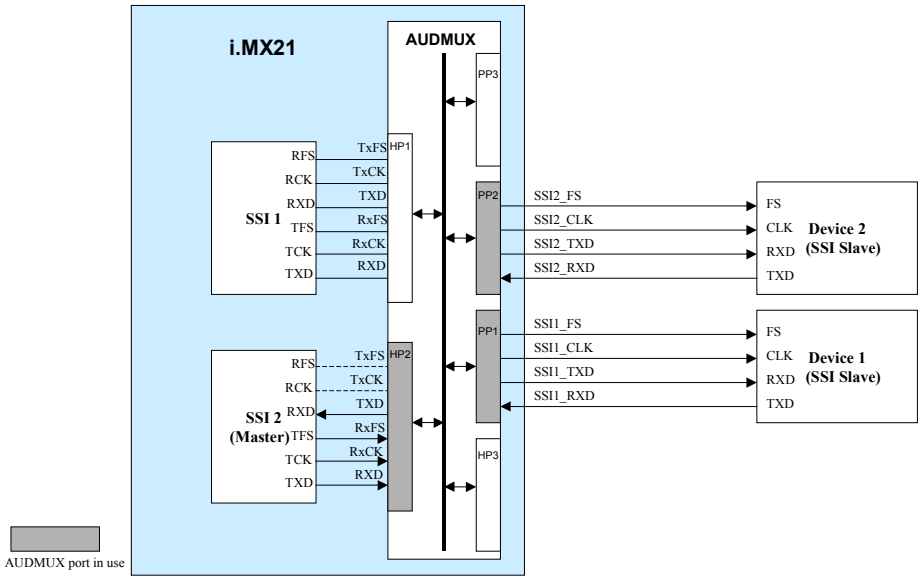

Figure 10. i.MX21 Connecting to Two External Devices in SSI Network Mode

Figure 10 shows the i.MX21 SSI2 as the SSI master driving two external devices connected at two external AUDMUX ports. Suppose the system is configured as an SSI network with 4 time-slots. Device 1 and i.MX21 will communicate in the first time slot while Device 2 and i.MX21 will communicate in the second time slot. The remaining two time slots are idle. Figure 11 illustrates the timing of this sequence.

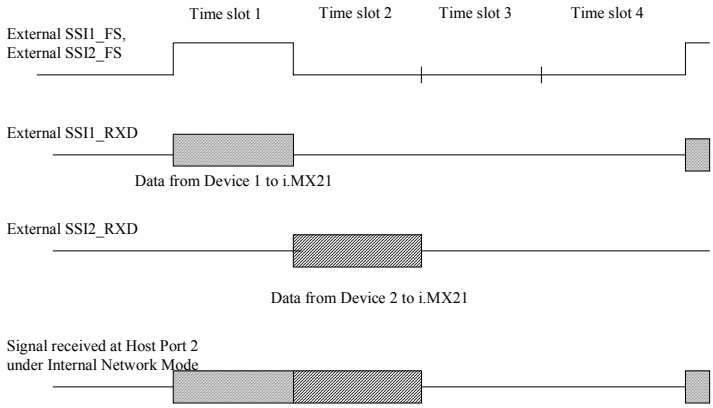

Figure 11. Internal Network Mode Timing Diagram Example

For the i.MX21 internal SSI2 to receive data from external Device 1 and Device 2, the AUDMUX Host Port 2 must be configured to the internal network mode bit and mask correctly. Table 6 provides the settings for this example.

Table 6. Host Port Configuration Register 2 (HPCR2 - $10016004)

Name	Settings	Comments
INMEN	1	Enable Internal Network Mode
INMASK	0xE7	Bit 3 and Bit 4 are set to 0, Bit 1 set to 1 (self port), others set to 1

4 Conclusion

The i.MX21 provides a very flexible connection for audio applications. The AUDMUX enables a programmable interconnection for voice, audio, and synchronous data routing among the internal SSI modules and external SSI devices. Hard-wired re-configuration are not required and resources can be effectively shared in different configurations.

5 References

The following documents can be used for additional information:

1. *MC9328MX21 Applications Processor Reference Manual* (order number: *MC9328MX21*RM)

For this and other technical documents about the i.MX21 products, go to www.freescale.com/imx.

6 Revision History

This revision is for the purpose of applying the Freescale template and does not include technical content changes.

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