CSU11026 Assignment 2

Using continuous assignments, write a Verilog

module Circuit_2 (Out_1, Out_2, Out_3, A, B, C, D);

for the circuit specified by the following Boolean functions:

$$Out\_1 = (A + B')C'(C + D)$$

$$Out\_2 = (C'D + BCD + CD')(A' + B)$$

$$Out\_3 = (AB + C)D + B'C$$