

## CSU11026 Assignment 5

Write a verilog dataflow description of a four-bit binary adder–subtractor

module AdderSub (sum\_diff, carry, A, B, select)

first output should be a 4 bit sum or difference, second is the carry.

The first two inputs should be the 4 bit numbers to add and the final input is a select which tells the module whether to add (zero) or subtract (one).

Verilog uses the bit length of the operands to determine how many bits to use while evaluating an expression. In the case of the addition operator, the bit length of the largest operand, including the left-hand side of an assignment, shall be used.

The tricky part of this problem is to get the carry bit right for subtract!