

## CSU11026 Assignment 4

Write a Verilog dataflow description

```
module BCD_Adder (Sum, Carry_out, Addend, Augend, Carry_in);
```

of a four-bit binary coded decimal adder.

Begin by writing a four bit binary adder module. Instantiate this twice in your binary coded decimal module and use structural verilog to provide the outputs.