KATHIR S

ELECTRONICS ENGINEER

Aspiring VLSI Design Engineer with strong knowledge in RTL design, functional and assertion-based verification, and physical design concepts including synthesis, STA, floorplanning, placement, and routing. Skilled in Verilog/SystemVerilog, EDA tools, and digital design flows. Eager to contribute to semiconductor innovation in a dynamic organization, while also bringing hands-on experience in embedded systems development and microcontroller-based applications.

CONTACT

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kathirr0805.github.io/Portfolio/#
itz.kathir2005@email.com

Coimbatore , India

SKILLS

- RTL Design
- VLSI Testing
- Physical Design
- Embedded Systems
- Internet of Things

TOOLS

- Vivado/Cadence
- Arduino IDE/STM32 IDX
- Matlab/Simulink
- Altera/Questa
- OpenROAD/Qflow

PROGRAMMING

- HDL Languages
- Embedded C
- Python
- Scripting
- C/C++

EXPERIENCE

VLSI DESIGN INTERN
PRO V LOGIC

Worked on RTL design and front-end verification for semiconductor applications.
Implemented functional verification, assertion-based verification, and FPGA prototyping.

ELECTRONICS ENGINEER INTERN
LEARN ELECTRONICS INDIA

Developed comprehensive tutorial content on VLSI and Verilog, assisting students in mastering front-end chip design concepts.
Created hands-on FPGA projects and authored technical blogs focusing on RTL design methodologies and best practices.

VLSI DESIGN AND SOC PROTOTYPING INTERN
QMOS TECHNOLOGIES

Implemented VHDL-based designs on Xilinx FPGA platforms, achieving 100% functionality in hardware testing.
Gained hands-on experience in SoC prototyping and hardware-software co-design.

CERTIFICATIONS

SYSTEM DESIGN THROUGH VERILOG — NPTEL
Completed an 8-week intensive course on Verilog, securing 85%.

VLSI PHYSICAL DESIGN WITH TIMING ANALYSIS — NPTEL
Learned concepts of physical design with Timing Analysis, securing 63%.

VLSI FOR BEGINNERS — NIELIT
Learned fundamental RTL design and VLSI design methodologies.

INTERNET OF THINGS — NOVITECH
Completed 30 days course covering cloud platforms and IoT projects.

EMBEDDED FOR BEGINNERS — NIELIT
Learned fundamental Embedded designs & System Design methodologies.

PROJECTS

MIPS PROCESSOR THROUGH VERILOG
Designed an efficient 16-bit single-cycle MIPS processor optimized for high-speed execution. Developed optimizations to enhance speed and power efficiency of the 16-bit MIPS processor.

RISC-V IMPLENTATION THROUGH VERILOG
Designed and verified a 32-bit RISC-V processor, focusing on instruction decoding, ALU operations, and control unit design.Created test benches to validate pipeline stages and optimize performance.

AXI TO APB BRIDGE
Designed an AXI to APB bridge enabling efficient communication between AXI masters and APB peripherals.Implemented protocol conversion logic ensuring reliable and synchronized data transfer.

SMART AUTOMATION USING IOT
Developed a smart home automation system using ESP8266. The system lists all home appliances , allowing users to select and control them. When an appliance is turned on, the ESP8266 triggers the relay, automating the appliance.

EDUCATION

2008-2022

SGMHSS School
HIGHER SECONDARY
I completed my schooling at SGMHSS, achieving 92.83% in 12th grade and 94.2% in 10th grade under the Tamil Nadu Board of Education.

2007 - 2010

Anna University Regional Campus
BE - ECE
I am currently in my final year of BE in ECE at AURCC with a CGPA of 8.52 and no arrears, focusing on VLSI and IoT technologies.