PIN CONFIGURATIONS

Pin Assignments for DE10-Lite

Signal	FPGA Pin	Description	I/O Standard
`clk`	`PIN_P11`	50MHz clock (MAX10_CLK1_50)	3.3V LVTTL
`reset_n`	`PIN_B8`	Push-button KEY0 (active-low)	3.3V Schmitt
`echo`	`PIN_V10`	GPIO_0 (Ultrasonic sensor echo)	3.3V LVTTL
`trigger`	`PIN_W10`	GPIO_1 (Ultrasonic sensor trigger)	3.3V LVTTL
`ir_sensors[0]`	`PIN_V9`	GPIO_2 (IR sensor for slot 1)	3.3V LVTTL
`ir_sensors[1]`	`PIN_W9`	GPIO_3 (IR sensor for slot 2)	3.3V LVTTL
`ir_sensors[2]`	`PIN_V8`	GPIO_4 (IR sensor for slot 3)	3.3V LVTTL
`ir_sensors[3]`	`PIN_W8`	GPIO_5 (IR sensor for slot 4)	3.3V LVTTL
`servo_pwm`	`PIN_V7`	GPIO_6 (Servo PWM control)	3.3V LVTTL
`red_led`	`PIN_A8`	LEDR0 (Red LED for "Full" status)	3.3V LVTTL
`green_led`	`PIN_A9`	LEDR1 (Green LED for "Available")	3.3V LVTTL

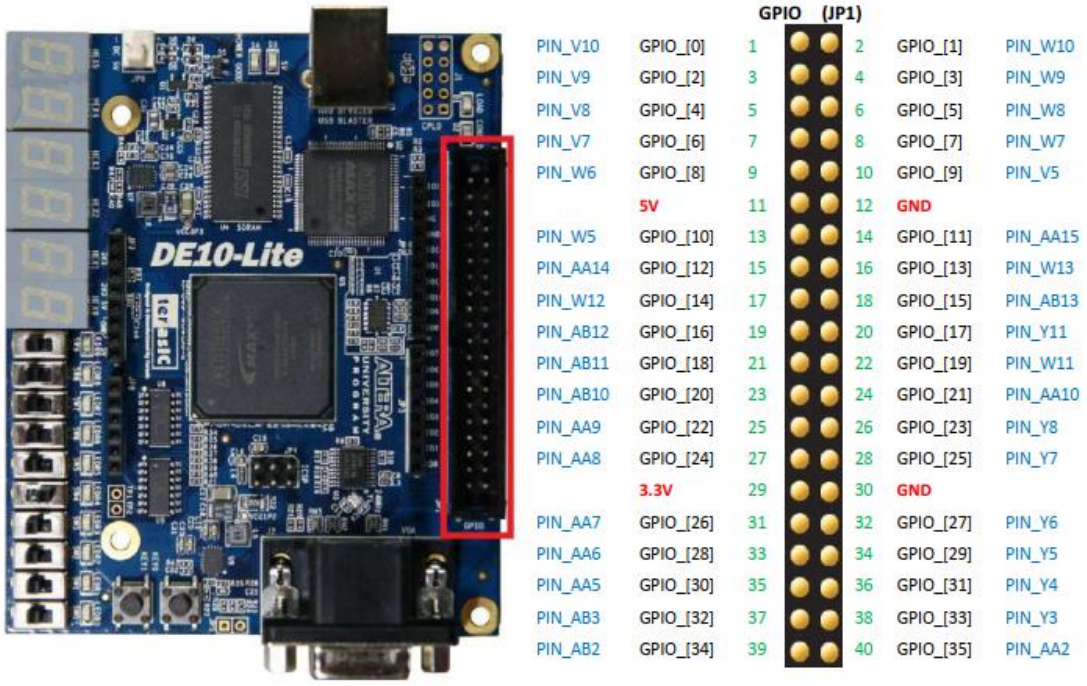

Figure 3-18 I/O distribution of the expansion headers

Table 3-3 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY0	PIN_B8	Push-button[0]	3.3 V SCHMITT TRIGGER"
KEY1	PIN_A7	Push-button[1]	3.3 V SCHMITT TRIGGER"

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTL