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Software-defined radio with flexible RF front end for satellite maritime radio applications

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Abstract This paper presents the concept of a software-defined radio with a flexible RF front end. The design and architecture of this system, as well as possible application examples will be explained. One specific scenario is the operation in maritime frequency bands. A well-known service is the Automatic Identification System (AIS), which has been captured by the DLR mission *AISat*, and will be chosen as a maritime application example. The results of an embedded solution for AIS on the SDR platform are presented in this paper. Since there is an increasing request for more performance on maritime radio bands, services like AIS will be enhanced by the International Association of Marine Aids to Navigation and Lighthouse Authorities (IALA). The new VHF Data Exchange Service (VDES) shall implement a dedicated satellite link. This paper describes that the SDR with a flexible RF front end can be used as a technology demonstration platform for this upcoming data exchange service.

Keywords Software-defined radio · AIS receiver · VHF data exchange services · Satellite radio applications · Flexible RF front end

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1 Introduction

Software-Defined Radios (SDRs) are becoming an important part of communication technologies to increase flexibility, data throughput and scientific output. Many satellite communication systems, either providing high-throughput data links in GEO-stationary orbit or earth observation satellites in low earth orbit, use flexible radio systems in which baseband-algorithms are implemented in software. The main advantage of these radios is the possibility to update the baseband processing systems and to improve the performance while the satellite is in space and operating. Another benefit of SDRs is the reduction in cost and size, since most data processing can be done in a single chip. Even if these kinds of SDRs have a modular architecture, all systems are designed for one particular service, like AIS receivers or UHF/S-Band transceivers for telemetry and telecommand. This is caused by the RF front end of those systems, since the main part of it is analog and limited to a specific frequency range. The DLR Institute of Space Systems is working on this topic developing a first prototype for a new type of SDRs, which allows a high modularity and flexibility in baseband processing, as well as variable frequency ranges. In this paper, we propose a concept and design for an SDR platform with a flexible RF front end system for satellite- and land-based RF-applications with focus on the implementation of an AIS receiver. Section 2 describes the fundamental architecture of the SDR platform. The technical specification and general performance of the core elements, the RF-Transceiver and Baseband Processor, are presented in Sect. 3. Section 4 describes the AIS service as a maritime radio application example. This first application example is implemented and analyzed regarding its feasibility and performance. The evaluation of the embedded AIS receiver solution is given in Sect. 5.

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Moreover, the developed radio platform shall be used as a technical demonstration testbed for new maritime standards like VHF data exchange services. The general concept of VDES will be discussed in Sect. 6 and it describes how the SDR platform can be used to analyze and verify those services. The final conclusions and an overview of further investigations are given in Sect. 7.

2 Design concept and hardware architecture

Most SDRs are implemented in digital signal processors (DSP) or into field programmable gate arrays (FPGA). The definition of SDR is basically related to the signal processing and their algorithms for a specific service, like AIS for maritime surveillance. The advantage of such processing implementations is the possibility to update and change single parts of the signal processing chain, since they are realized in software.

Commercially available, state-of-the-art SDRs are mainly limited to their operational frequency range and bandwidth [3–5]. This is caused by the (mostly analog) circuits of the RF front end. Figure 1 represents the architecture with the fundamental blocks to realize an SDR with a flexible RF front end. The following section describes the concepts and architecture of a new type of SDRs for either satellite- or land-based RF-applications, with a high flexibility for signal processing, as well as operable frequency ranges from 70 MHz up to 6 GHz. Additional up- and down conversion is feasible with an extended design, but is not part the presented approach. To simplify the system of Fig. 1, the RF-Transceiver and the RF front end should be investigated in a common part. Since the RF-Transceiver does not provide the RF-performance, e.g., transmitting power, on its own to operate applications in space, an additional RF front end becomes essential. The additional RF front end will later be separated from the SDR-Board (see Fig. 2), into a specified extended design, adjusted to missions in space. The RF-Transceiver can be driven in time division duplex (TDD) or frequency division duplex (FDD) configuration and features two independent receiving- and transmitting chains with multiplex RF-input and RF-outputs. This configuration results in 2 × 3 differential inputs and 2 × 2 differential outputs. This setup allows the operation of up to six additional receiver front ends or antennas and up to four additional front ends for the transmission unit. Due to the FDD configuration, the RF-Transceiver is able to receive and transmit simultaneously (full duplex). The baseband processor will capture and provide data from/to the RF-Transceiver and realize the system control and monitoring. Figure 2 shows a 3D hardware model of the first prototype for the SDR platform.

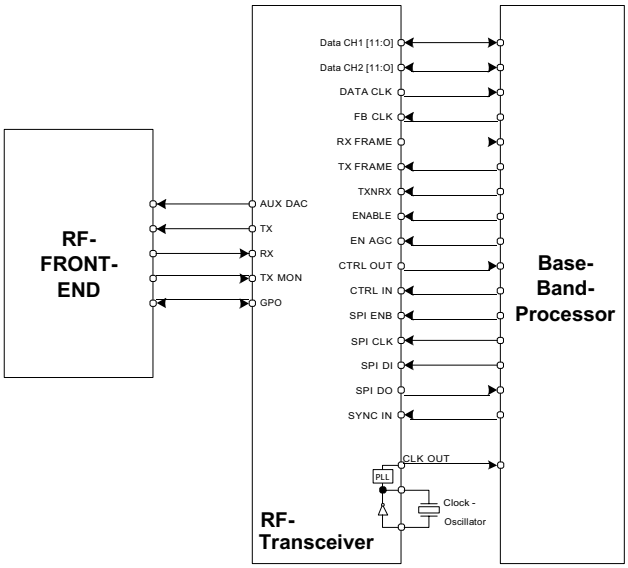

Fig. 1 Basic design of the software-defined radio with flexible RF front end

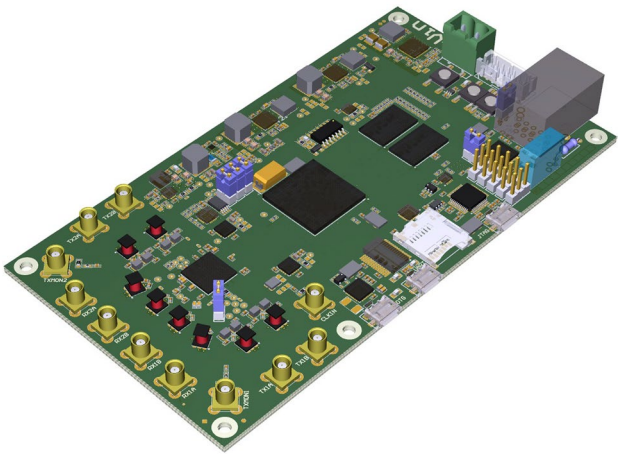

Fig. 2 Illustration of the first SDR prototype

The prototype contains interfaces, like USB or Ethernet, for debugging and system analysis. These interfaces and other units (e.g., power distribution) will partially be replaced in the further development process, since they will not be used in space.

3 Technical specification

This section describes only the technical specification of the two basic elements, the baseband processing- and RF-Transceiver unit. The additional RF front end can be designed for a specific application and their requirements, or can be designed generic for different frequency bands to

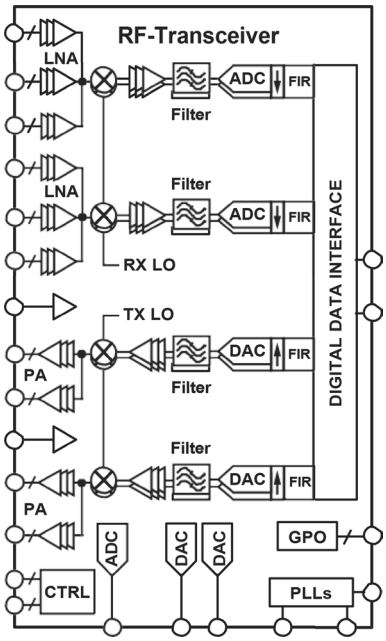

Fig. 3 Functional block diagram of the RF-Transceiver

Table 1 Features of the RF-Transceiver unit

Description	Value/quantity
Operable frequency band	70 MHz–6.0 GHz
Local oscillator	Fully integrated fractional-N synthesizers
Local oscillator resolution	2.4 Hz Maximum LO step size
ADC/DAC	12 Bit sigma-delta, up to 640 MSPS
Receivers	2 × 3 Differential or 2 × 6 single-ended inputs
Adjustable RX-gain	Manual and automatic gain controlled
Noise figure	<2 dB @ 800 MHz
Transmitters	2 × 2 Differential outputs
TX-attenuation	0.25 dB Step size, 86 dB range
Tunable channel bandwidth	<200 kHz–56 MHz
Type of operations	TDD and FDD
Digital interface	CMOS/LVDS
Self-calibration	DC-Offset-calibration, quadrature-calibration
Digital filters	128 Complex taps for RX- and TX-chain
Enable state machine	(ENSM) for real time controlling

support the up to six receiver inputs and four transmitter outputs of the RF-Transceiver.

3.1 RF-Transceiver unit

The RF-Transceiver is a fully integrated wide-band transceiver. Figure 3 shows a block diagram with all

Table 2 General specification of the RF-Transceiver unit [2]

Parameter	Min	Typ	Max	Unit
Receiver specification				
Center frequency	70	–	6000	MHz
Gain	0	–	73	dB
Gain step	–	1	–	dB
RSSI range	–	100	–	dB
RSSI accuracy	–	2	–	dB
Noise figure	2	–	3.8	dB
Third input intermodulation intercept point	−18	–	−14	dBm
Local oscillator leakage	−122	–	−95	dBm
Quadrature gain error	–	0.2	–	Percent
Quadrature phase error	–	0.2	–	Degrees
Input return loss	–	−10	–	dB
Transmitter specification				
Center frequency	70	–	6000	MHz
Attenuation	0	–	90	dB
Attenuation step	–	0.25	–	dB
Maximum output power	6.5	–	8	dBm
Third output intermodulation interceptpoint	17	–	23	dBm
Carrier Leakage (40 dB Attenuation)	−32	–	−30	dBc
Noise floor	−157	–	51.5	dBm/Hz
Output return loss	–	−10	–	dB
LO Synthesizer specification				
LO frequency step		–	2.4	–
Integrated phase noise (100 Hz to 100 MHz)	0.13	–	0.59	rms

fundamental segments implemented in the RF-Transceiver Unit.

The 2 × 2 Transceiver uses two independent transmitter- and receiver chains, which can be used in TDD and FDD mode. Each of the receiving chain contains low-noise amplification elements, an IQ-demodulator, analog and digital filters, as well as an analog digital converter (ADC).

The transmitting chain contains almost the same components as the receiver chain, with the exception of the digital analog converter and the amplification section at the output. A detailed description of the RF-Transceiver is given in the application example section of this paper. The complete receiving chain, including all elements and their functionality, is explained and configured to the application specification. Table 1 gives a brief overview of the RF-Transceiver features. The RF-Transceiver performance depends on the operational frequency band, as well as on the RF-application specification. For this reason, only a general specification for the receiver, the transmitter and the local oscillator synthesizer of the RF-Transceiver can be given. Those details are listed in the following Table 2.

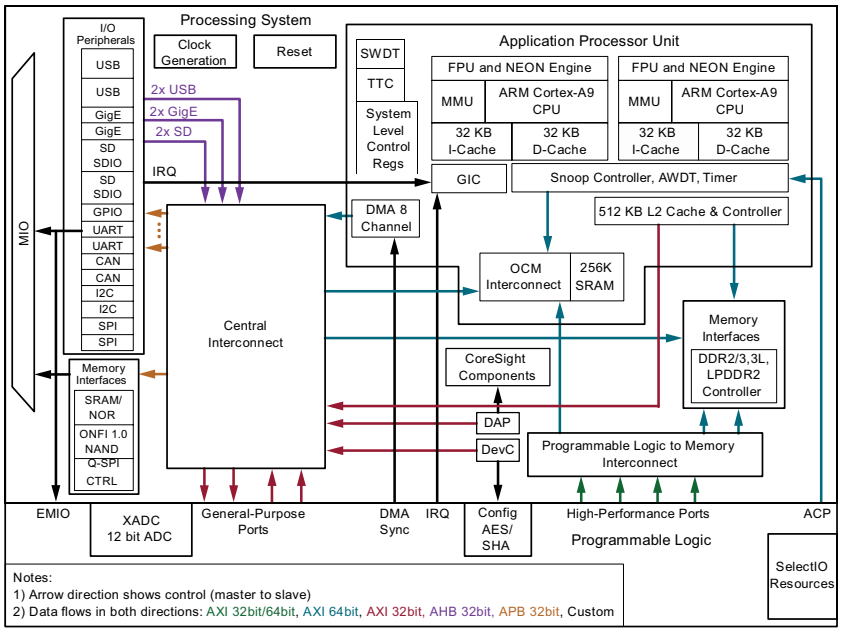

Fig. 4 Block diagram of the baseband processing unit [1]

Table 3 Specification of the Zynq SoC, separated into the processing system and the programmable logic [1]

Description	Type/quantity
Processor extensions	NEON Single/double precision floating point for each processor
L1 Cache	32 KB instruction, 32 KB data per processor
L2 Cache	512 KB
On-chip memory	256 KB
Memory interfaces	DDR3, DDR3L, DDR2, LPDDR2, 2x Quad-SPI, NAND, NOR
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI 4x 32b GPIO, 2x USB 2.0 (OTG), 2x Tri-Mode Gigabit Ethernet, 2x SD/SDIO
Flip-flops	106,400
LUT	53,200
Logic cells	85 K logic cells
BlockRAM (Mb)	560 KB
DSP slices	220

For detailed performances separated analysis needs to be done on the dedicated frequency band and RF-application.

3.2 Baseband processing unit

The baseband processing system (BBS or BBP) is based on a System On A Chip (SoC). The chosen Xilinx Zynq SoC consists of a processing system (PS), including an application processing unit, interconnects and memory interfaces, as well as a programmable logic (PL) comparable to a FPGA structure. The advantage of such chip technologies is that it is very fast, multiple and complex signal processing can be performed in the high-efficient FPGA fabric, while the data post-processing and interfacing to the system can be handled by the processing system. The SoC block diagram is given in Fig. 4. The SoC comes with a Dual ARM Cortex-A9 MPCore, which can be operated up to 667 MHz. Connected to the SoC is a hybrid memory architecture with volatile and non-volatile memory options. A detailed list of supported memory interfaces is given in Table 3. Digital interfaces are realized in form of a UART-Controller which can be expanded to any serial interface like RS-232, RS-422 or RS-485.

As can be seen in Fig. 4 and Table 3, there are several other digital interfaces which can be used to interact with the processing system.

Table 3 gives a brief overview of the basic specifications of the SoC processing system and programmable logic. An interconnection, implemented into the PS, allows the connection

of system resources using AXI point-to-point channels for communicating addresses, data, and response transactions between master and slave clients. The AXI-Interface manages multiple transactions and is designed for low-latency paths, as well as high-throughput and cache coherent data paths. Due to the 64-bit AXI-Interface, it is possible to push and capture data between the DDR memory (DDRM), connected to the PS, and the RF-Transceiver, which is interfaced to the PL. The SDR platform runs with an operating system in the processing system, which can be booted in secure or non-secure mode. The filesystem or image of the operation system can be implemented into a static memory, like NAND-, NOR flash or SD card. The BBS can select and load between different memory sources. The general boot sequence can be separated into two stages. An internal BootROM stores the stage-0 boot code, which configures the ARM processor and a First Stage Bootloader (FSBL). The FSBL is responsible for the initialization of the PS configuration, the peripherals and downloading the bitstream into the programmable logic. Afterward, it loads the second stage bootloader into the DDR, which starts the booting of the operation system. A fallback is featured by the FSBL and allows booting a golden backup-image, if the updated image is damaged or a failure due to the booting sequence occurs. In case of a corrupted image, the FSBL falls back to the BootROM and searches for the next bootable image.

4 Maritime radio application examples

As a first application example, the maritime mobile service is used to demonstrate the performance of the SDR platform. This first application is an AIS receiver implemented in C/C++, running on the PS. The architecture of the AIS receiver and interfaces to the hardware of the RF-Transceiver is described, and dedicated test cases are executed to analyze the performance of the embedded AIS receiving system.

4.1 Maritime mobile services

The AIS services are allocated in the VHF maritime mobile band between 156 and 162.025 MHz. AIS uses two major channels (AIS1 and AIS2) with a carrier frequency at 162 MHz and a frequency offset of ±25 kHz. The transponder on a vessel is categorized into two classes.

Class A transponders are intended for commercial shipping vessels and transmit with an output power of 12.5 W. They are mandatory on all vehicles of more than 300 gross tonnages, on ships engaged on international voyages and on certain passenger ships, which are subject to the SOLAS convention [14]. Class B transponders transmit with 2.5 W and are used on all vessels where a class A AIS transponder is not mandatory [8]. Table 4 gives a summary of the physical layer specification for the AIS 1, AIS 2 and AIS long range (Channel 75 and 76) in the maritime mobile band. The frequency channels are regulated by the International Telecommunication Union (ITU) and the International Maritime Organization (IMO). AIS is primarily used to improve the safety of vessels and to avoid collisions. Moreover, AIS provides information about a ship, such as identification details, the speed over ground, the position and the course. This information is exchanged between other nearby vessels and coast stations (typically limited to a range of 60 nautical miles, due to the earth's curvature). AIS uses Self-Organizing Time Division Multiplex.

Table 4 Definition of maritime mobile band specifications (physical layer)

Description	Value	Unit
AIS carrier frequency	162	MHz
AIS channel 1 frequency (AIS1)	161.975	MHz
AIS channel 2 frequency (AIS2)	162.025	MHz
AIS long-range carrier frequency	156.8	MHz
AIS channel 75 frequency	156.775	MHz
AIS channel 76 frequency	156.825	MHz
Transmitted power class A	12.5	W
Transmitter power class B	2.5	W
Modulation scheme	GMSK	–
BT product on receiver	≈0.4	-
BT product on transmitter	≈0.5	-
Baud rate	9600	Baud

Access (SO-TDMA), where cells can reach a range of 20–200 nautical miles [8]. SO-TDMA is a big challenge to capture data from space, since the satellite-based AIS antenna has a much larger coverage, than the single TDMA zones. This results in overlapping received signals from different cells, where vessels can transmit simultaneously (as seen in the first time slot of Fig. 5). One solution to this issue could be to reduce the beam width of the antenna, and thereby to decrease the coverage area. This case has already been analyzed and tested by DLR Bremen and demonstrated on the DLR satellite AISat [9]. The high gain helical antenna, used on AISat, cannot achieve a smaller coverage than 200 nautical miles. To reach a smaller coverage area an antenna needs a half power beam width of less than 5 ° in a low earth orbit. Due to the wavelength of approximately two meters, an antenna array which can further improve the gain and beam width angle is hardly realizable on a small satellite. Another solution to this problem lies in post-signal processing, with complex algorithms to reconstruct the single AIS messages of different SO-TDMA-Cells [10]. Since those algorithms are very complex, high computing power is required. The proposed

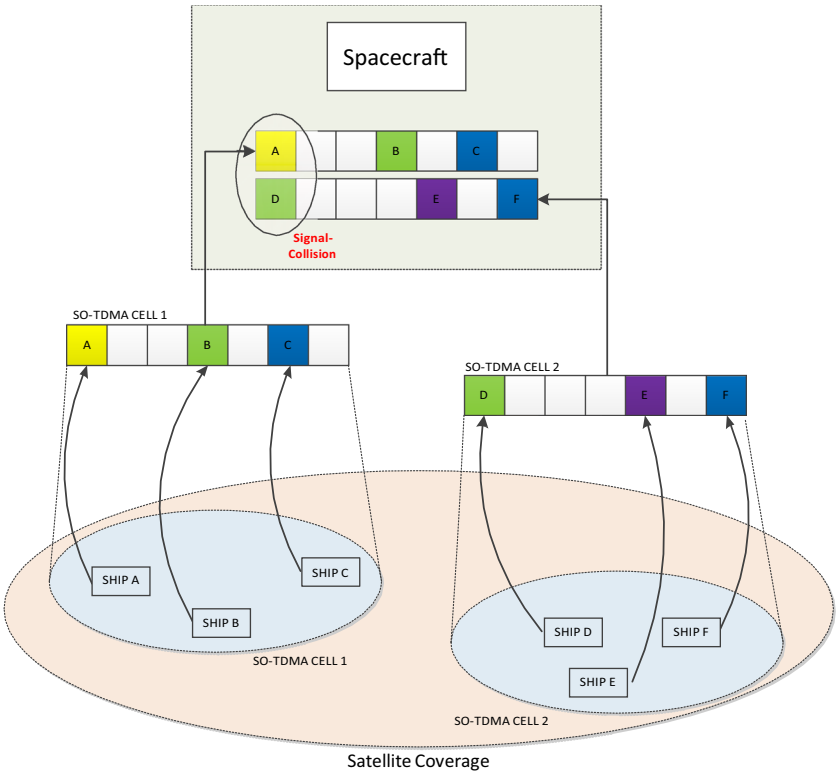

Fig. 5 AIS signal collision due to multiple captured SO-TDMA cells

SDR platform is a high-performance transceiver system that allows to implement and validate those algorithms. As already described in the beginning of this section there are two long-range AIS channels (75 and 76) available, which are only used for broadcast transmission from vessels. AIS long-range channels have almost the same specification as the AIS1 and AIS2 but are transmitted on a different carrier frequency (refer Table 4). Those channels have been specified in the ITU-R M.1371 recommendation for satellite-based AIS detection. The major benefit of using channel 75 and 76 for vessel detection from space is that the amount of transmitters needed is limited, compared to AIS 1 and AIS 2 and, therefore, the probability of signal collisions is low. Currently, there are no well-known commercial receivers available, nor a state-of-the-art receiver that is able to receive on all four channels. The DLR SDR approach is capable of tuning the RF front end configuration in software to enable AIS data processing for AIS1, AIS2, channel 75 and channel 76. This advantage can be used to increase the number of detected vessels by switching between those channels when the satellite collects signals over the sea (AIS 1 and AIS 2) and near to the coast, where the vessel density is very high (long-range AIS).

4.2 Design and implementation of an AIS receiver

The AIS receiver algorithm is running on a Linux operating system and is written and implemented in C-Code. The complete signal processing flow, beginning with the captured RF-signal on the RF-Transceiver RX-input to the final demodulated and decoded data, is given in the block diagram shown in Fig. 6. The following section describes the design, implementation and functionality of the embedded AIS receiver on the SDR platform. For a better overview, the signal processing flow is separated into the related modules.

RF-Transceiver The received signal is primarily amplified by a stack of low-noise amplifiers (LNAs). Afterward, the signal is mixed into the baseband, and then re-amplified by a transimpedance amplifier (TIA). The baseband signals receiving path is also composed of two programmable analog low-pass filters, followed by a 12-bit ADC. The digitized signal is then passed through four stages of digital decimating filters. Each of the four decimating filters can be bypassed.

The 3 dB corner frequency for each low-pass filter can be configured by the baseband processor, via SPI interface. LNA, Mixer and the TIA are adjustable and driven by the gain control modes. A threshold detector is placed between the TIA and the halfband filters, as well as behind the ADC. These detectors react nearly instantaneously to a low- or peak power event and read the overall gain. The configurations for the overall gain are given in a programmable gain table. Each receiving chain has its own gain table, which is used by the gain control modes. The sampling rate for the captured IQ-baseband data is set to 0.480 MSPS, which includes an

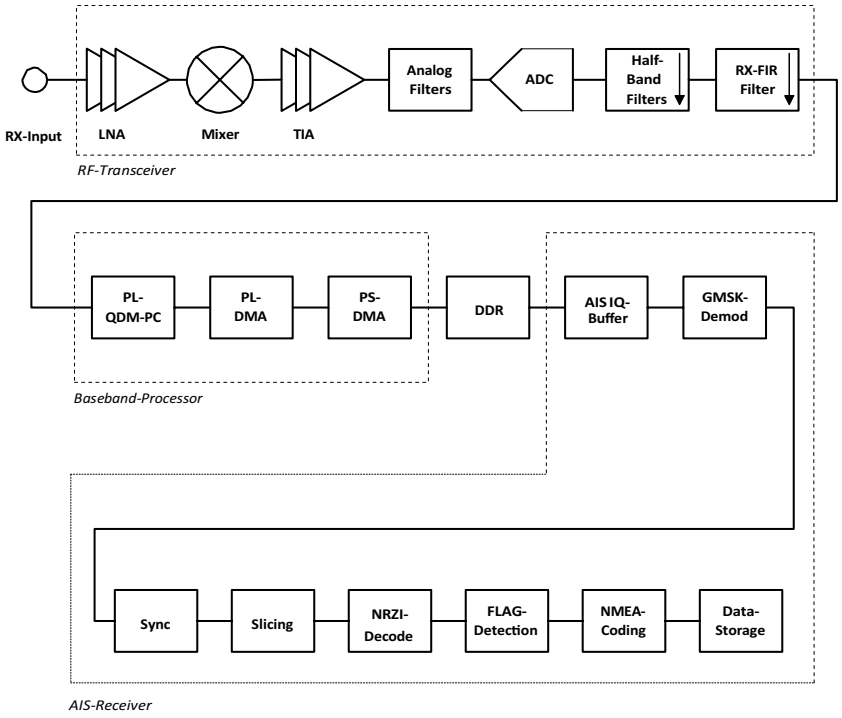

Fig. 6 Detailed block diagram of the AIS receiver

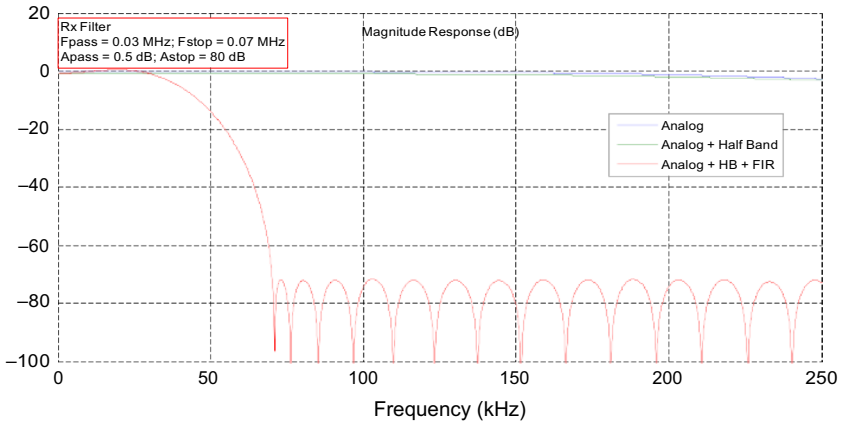

Fig. 7 FIR downsampling and channel isolation filter designed for AIS

Table 5 Configuration of the RF-Transceiver unit for the AIS receiver application

Description	Value/quantity
Type of operations	TDD–RX1
Automatic gain control	Slow attack
Local oscillator frequency	162 or 156.8 MHz
Analog channel bandwidth	200 kHz
ADC sample rate	16 MSPS
FIR Filters	128 complex taps
FIR 3 dB-frequency	30 kHz
Decimation factor	4
Sample rate	0.48 MSPS

oversampling factor of 50 to the AIS baud rate of 9600 bits per second. The last filter stage of the RF-Transceiver is used to achieve a sample rate of 480 KSPS and isolate to the AIS 1 and AIS 2 channels, which are modulated 25 kHz around the carrier, resp. the baseband (0 Hz). To ensure that just the AIS signal will be demodulated, the FIR filter should be designed as narrow as possible. According to the maximum numbers of 128 coefficients, the filter in Fig. 7 is designed.

As can be seen in Fig. 7, the overall filter characterization for the RF-Transceiver is designed for an 3 dB-frequency of 30 kHz and achieves an attenuation of −80 dB at 70 kHz. The RF-Transceiver configuration for the AIS receiver application is summarized in Table 5.

Baseband processor This application uses the Linux drivers to configure the RF-Transceiver via SPI interface and receive the captured baseband signal. The baseband signal is already IQ-demodulated, so the AIS demodulation algorithm can operate with the given complex values. These are written to an allocated buffer in the DDRM. The buffer allocation procedure is done by the Linux driver of the RF-Transceiver and contains an extensive multiple buffer architecture to improve the gathering of high-speed data. The reference design for the RF-Transceiver is implemented into the programmable logic and contains the interface to the RF-Transceiver, several self-calibration algorithms, as well as a direct memory access (DMA) module, which allows the transmission between the RF-Transceiver and the DDRM. The DMA core is essential since the DDRM is not directly connected to the PL.

AIS receiver The AIS receiver application requests a buffer using the Linux driver to read data from the RF-Transceiver. After the buffer is allocated, the AIS receiver gets the IQ-data from the request buffer size and starts the signal processing. If the whole buffer is processed, the application polls a new buffer with IQ-samples. The demodulation and decoding process of the AIS application is described related to the given blocks in Fig. 6.

- GMSK-Demodulation

- The disadvantage of a conventional minimum shift keying (MSK) is that the transition between the two AIS channels happens instantaneously. This effect causes a broad power spectrum and needs to be reduced. Therefore, a gaussian pulse shaping filter is implemented in the MSK. The bandwidth delay product (BT) for an AIS receiver is recommended to be 0.4 (refer Table 4) by the ITU and IMO.
- Synchronization
- The synchronization block uses cross-correlation to detect the training sequence in the AIS data packet and synchronize the data rate. An enable signal is set after the training sequence has been found and sustains the signal processing.
- Slicing
- The slicing block down-converts the frequency-demodulated baseband signal to the AIS baud rate. Moreover, the amplitude will be normalized to -1 and $+1$. This decision is required for the NRZI-decoding in the next block.
- NRZI-Decoding
- This module converts the previously decided signal to return to zero signal. The output data are now fully digital and contains only values with a logical one or zero.
- FLAG-Detection
- The decoded data packet contains a Start-Flag and an End-Flag (HDLC-Flag). The detection of this flag is required to select the final AIS message. The HDLC-Flag is also used to calculate the check sum and verify the validity of the AIS message.
- NMEA Decoding
- AIVDM/AIVDO is a two-layer protocol which converts the NRZI decoded data into a readable ASCII format. The outer layer is the NMEA 0183 Standard for communication between navigation and GSP systems on vessels and a terminal.
- Data sorage
- Finally the AIS message will be saved as a text file in the DDR memory and SD card. Additionally, the decoded bits are available over the serial interface and get streamed over a LAN socket.

5 Evaluation of the embedded AIS receiver

The evaluation of the embedded AIS receiver is assessed based on the receiving performance of dedicated transmitted signals over an adjustable RF path. Those AIS signals were generated in software (via Matlab), beginning with an ASCII format to the final baseband samples. A signal generator is converting those samples into an analog waveform and modulates the signal to the specific carrier frequency. The output of the signal generator is connected to RX1 of the RF-Transceiver inputs. The major goal of the performance evaluation is to analyze the receiver sensitivity for AIS1, AIS2 and long-range AIS. Due to the specification of the AIS channels (refer Table 4), the modulated carrier frequency of the signal generator will be changed from 162 to 156.8 MHz after every test case series. Since the RF-Transceiver has a build in automatic gain control, the sensitivity is measured for hard attack mode. Note that the given values of received messages do not relate to the maximum transmitted messages of each test case. The quantity of received messages is given in percent and depends on the maximum number of correctly computed AIS messages at a certain input power level. A further enhancement of the input power does not increase the number of correct demodulated AIS messages.

5.1 Test case 1

Fully allocated slots in one SO-TDMA cell A message was transmitted on channel 1 (AIS1 or 75) and channel 2 (AIS2 or 76) simultaneously every 26.67 ms. This case represents a typical scenario for a high-density cell, e.g., north sea, where all slots are allocated.

Table 6 shows a summary of the transmitted, 60-s-long test signal in ASCII. The transmitted IQ-signal components

Table 6 Demodulated AIS messages for test case 1

Cell	Time	Channel	Message
C00	0.0000	A	!AIVDM,1,1,,A,@ q7:0q < 2::TESTA:01:01:01,0*1A
C00	0.0000	B	!AIVDM,1,1,,B, < r>NWCWo::TE STB:01:01:02,0*68
C00	0.0267	A	!AIVDM,1,1,,A,J9OivcaH::TE STA:01:01:03,0*04
C00	0.0267	B	!AIVDM,1,1,,B,KOnhSPEC::TE STB:01:01:04,0*02
C00	0.0533	A	!AIVDM,1,1,,A,WAaSvcaH::TE STA:01:01:05,0*06
C00	0.0533	B	!AIVDM,1,1,,B,KDAp24EC::TE STB:01:01:06,0*67
…			

AIS channel 1 and channel 2 were transmitted simultaneously every slot

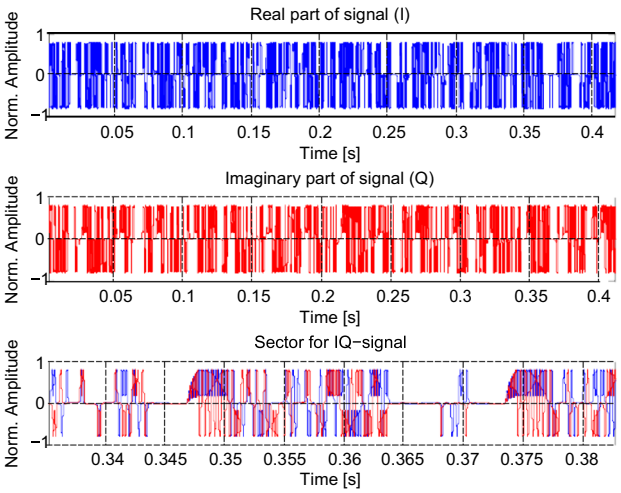

Fig. 8 Transmission of generated IQ-waveform for Test Case Nr. 1

(in baseband), as well as a dedicated sector view, are given in Fig. 8. Figure 9 illustrates the sensitivity of the receiver for AIS1, AIS2 and long-range AIS, over the input power at the receiver.

There were no sensitivity differences between each AIS channel detected. The maximum quantity of received messages will be reached at an input level of −113 dBm. The minimum signal input power to compute AIS messages from the transmitted test signal is −117 dBm.

5.2 Test case 2

Test case 2 represents partially allocated slots in one SO-TDMA cell. A message was transmitted alternating between channel 1 and channel 2 every 53.33 ms.

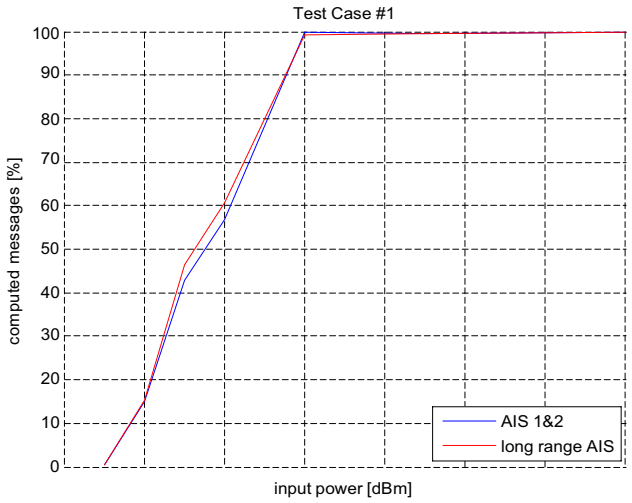

Fig. 9 Receiver sensitivity for Test Case Nr. 1

Compared to test case 1 there is a pause time without transmission, where the AGC of the RF-Transceiver will rapidly increase the gain, since there is only noise at the receiver input. This test was done to verify the AGC-behavior at fast/high signal variations. Table 7 contains the first ASCII format messages of the transmitted test signal and Fig. 10 shows the IQ-waveform.

This test signal is also 60 s long, but contains only a quarter of AIS messages compared to the previous test case.

This scenario represents areas with lower vessel density, which could appear on an open sea section like the Atlantic Ocean. Figure 11 shows the results for the receiver sensitivity for AIS1, AIS2 and AIS channel 75 and 76.

The receiver is able to compute AIS signals at a level of around −117 dBm, which is almost the same value as the results of the previous test case 1. The maximum quantity of received and correctly computed AIS messages will be reached at an input power level of −112 dBm. Comparing the receiver sensitivities of the first and the second scenario, it can be shown that the AGC can handle simultaneously transmitted signals, as well as burst transmission messages (test case 2) for each carrier frequency.

5.3 Test case 3

Test case 3 also represents allocated slots, but for *multiple* SO-TDMA cells. Messages from three different cells are transmitted every 26.67 ms. For better results, only channel 1 (AIS1 and channel 75) is used for transmission. This scenario represents satellite-based AIS detection, where multiple cells with a high density of ships are covered by the AIS antenna.

An example of the transmitted AIS signal is given in Table 8. The message order is derived from a 60-s satellite

Table 7 Demodulated AIS messages for test case 2

Cell	Time	Channel	Message
C00	0.0000	A	!AIVDM,1,1,,A,@ q7:0q < 2::TESTA:01:01:01,0*1A
C00	0.0533	B	!AIVDM,1,1,,B, < r>NWCWo::TE STB:01:01:02,0*68
C00	0.1067	A	!AIVDM,1,1,,A,J9OivcaH::TE STA:01:01:03,0*04
C00	0.1600	B	!AIVDM,1,1,,B,KOnhSPEC::TE STB:01:01:04,0*02
…			

AIS channel 1 And 2 were transmitted every fourth slot

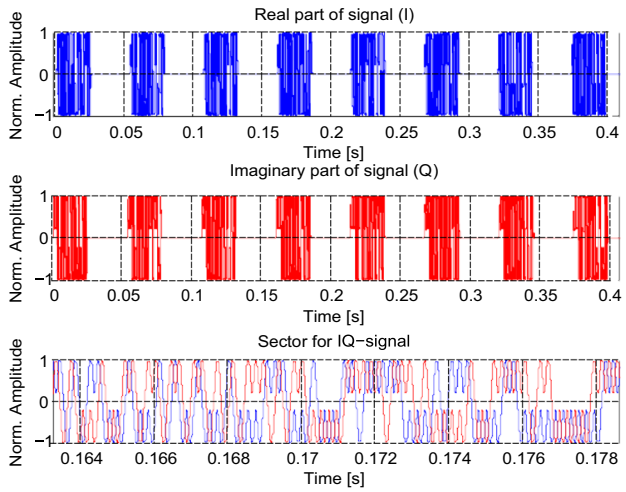

Fig. 10 Transmission of generated IQ-waveform for Test Case Nr. 2

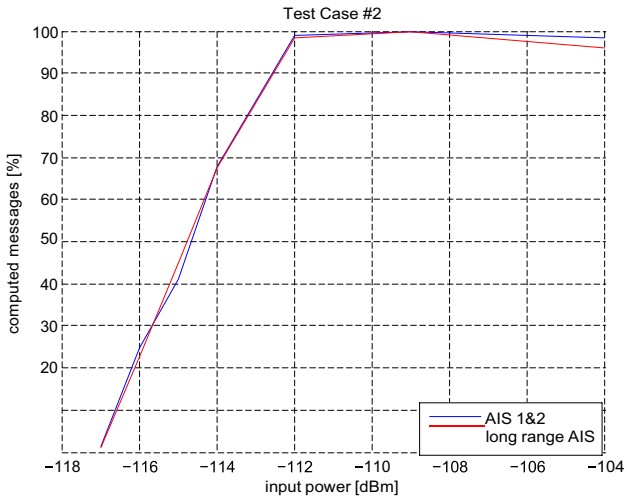

Fig. 11 Receiver sensitivity for Test Case Nr. 2

Table 8 Demodulated AIS messages for test case 3

Cell	Time	Channel	Message
C00	0.0000	A	!AIVDM,1,1,,A,139O;:3F > b@ HDVh0P00:,0*08
C01	0.0000	A	!AIVDM,1,1,,A,13b4OJ1IbHh77?v0P01‘, 0*1C
C02	0.0000	A	!AIVDM,1,1,,A,18Uigf3Qc5@ BHgv0P004,0*2A
C00	0.0267	A	!AIVDM,1,1,,A,139jWE‘VEW > ‘Q?v0P0 07,0*55
C01	0.0267	A	!AIVDM,1,1,,A,13@FAqrN- DreoP6F0P005,0*28
C02	0.0267	A	!AIVDM,1,1,,A,13a > 59jVEWAM- 5bJ0P003,0*56
C00	0.0801	A	!AIVDM,1,1,,A,17bU < -:13sbHh77?v0P0 ,0*1B
C02	0.0801	A	!AIVDM,1,1,,A,13bPJHSs::90KlmpO:v0, 0*1C

AIS channel 1 were transmitted partial from one or more cells

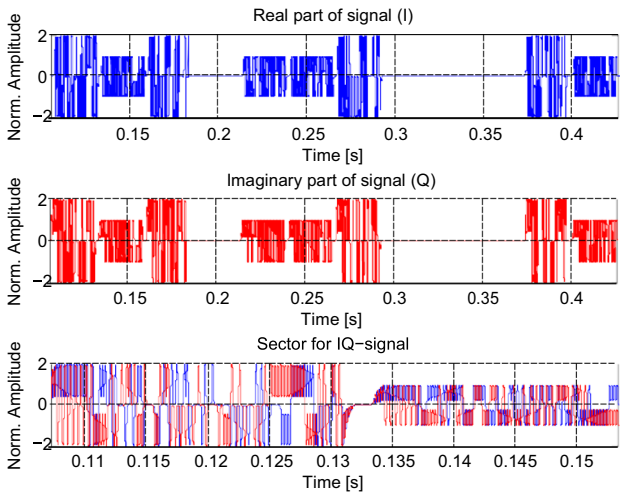

Fig. 12 Transmission of generated IQ-waveform for Test Case Nr. 3

path over an area with three cells, where different numbers of vessels are located.

To optimize the scenario for a realistic satellite pass, several interferences like the path losses between ship and satellite, Doppler frequency and time shifts have been added to the generated baseband AIS signal. The collision, or the overlapping of signals from different cells, can be seen in Fig. 12. To distinguish the differences between a collide message and a single AIS message, a section view of the transmitted IQ-signal can be seen in subplot *Sector*

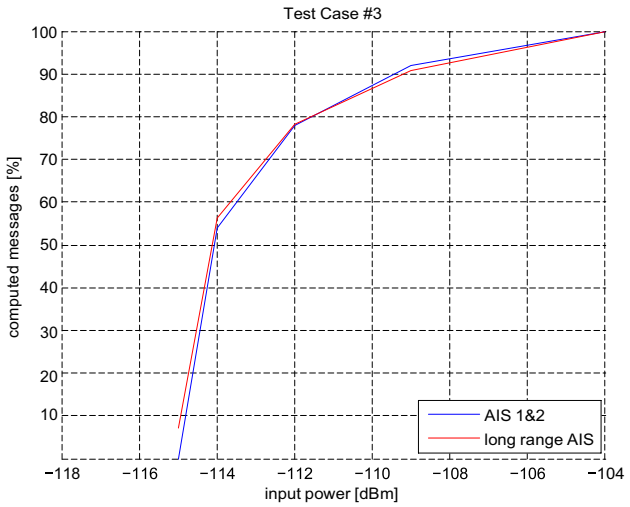

Fig. 13 Receiver sensitivity for Test Case Nr. 3

for IQ-signal in Fig. 12. The sectional view shows not only a difference between the amplitudes, but also highlights that the whole signal has been manipulated due to the signal collision.

Figure 13 shows the receiver sensitivity for the satellite-based scenario. The number of correctly computed AIS messages, compared to the number of transmitted AIS signals, is less than 10 percent, whereas also single, non-overlapping, messages were transmitted. So the actual number of extracted overlapping messages is much lower than the total number of collected signals. To verify the receivers RF-performance, the sensitivity for such signals shall be analyzed like the previous test scenarios. Compared to the first and second test case, a difference can be observed in the dynamic range. The minimum input power required to receive a message is ascertained by a level of −115 dBm. The maximum number of computed messages is reached at −105 dBm. No significant difference in the RX-sensitivity between both transmitted AIS services can be seen.

The extraction of collided AIS signals is a big challenge in satellite-based AIS detection and the post-processing to decrypt and extract those signals from each other becomes very complex and requires a lot of computing resources. A proposed solution for on-board post-processing via beam forming and the implementation of a multi-antenna system is given in [11]. The described algorithm implements several diversity techniques and is capable to extract various numbers of multiple overlapping AIS signals. Such a receiver system requires many resources and becomes difficult to implement on small satellites. Additionally, as already described earlier in this paper, a multi-antenna system in VHF is hard to realize due to the large dimension of the antennas.

6 Radio testbed for VHF data exchange services

In recent years, the use of AIS has increased significantly, particularly due to the use of Application Specific Messages (ASM), which is causing the network overloading of the AIS channels, jeopardizing the proper functionality of safety monitoring systems associated with the AIS. VDES is a proposed solution where additional maritime channels could be used to exchange the VHF data and protect the original function of AIS. This section describes the actual definition of VDES and it will be described how the SDR platform can be used to analyze the VDES service.

The concept of the VDES system has been introduced and proposed by a ITU-R Working Party 5B (WP5B), several administrations and the IALA. VDES shall contain terrestrial and a satellite services, which are complementary to each other. A system overview of VHF data exchange services is given in Fig. 14.

The associated frequency allocation for the extended maritime band with VDES is given in Fig. 15. The previous described SDR platform shall be used to implement and analyze the VHF data exchange services. Since there is no concrete transmission scheme protocol determined, various numbers of system parameters can be explored to design a suitable air interface for VDE services. This transaction requires a detailed trade-off and cross checking against the major VDES requirements. Alagha et al. [12] outlines some of these aspects and gives a detailed example and performance analysis with a DVB-S2X standard, as a baseline for the air interface of VDES. DVB-S2X is an extension of the DVB-S2 specification that provides additional technologies and features to enhance the efficiency and performance of DVB-S2 [15]. DVB-S2 itself has already been tested and implemented into the same SoC baseband processor as by [13]. The resource utilization for DVB-S2, based on the case study of [13] and the reference design of the RF-Transceiver, is given in Table 9.

Based on these analyses, an implementation of the recommended DVB-S standard and their algorithm into the programmable logic of the SDR seem feasible. A detailed analysis and implementation of DVB-S2X on the presented SDR approach is mandatory.

7 Conclusion and further investigations

In this paper, the basic concept and architecture of a software-defined radio with a flexible RF front end has been presented. The general configuration and, in particular, the performance and benefits of the SoC baseband processor and RF-Transceiver unit have been analyzed and demonstrated. Equivalent SDR platforms are already available as a combination of development boards for the Zynq baseband

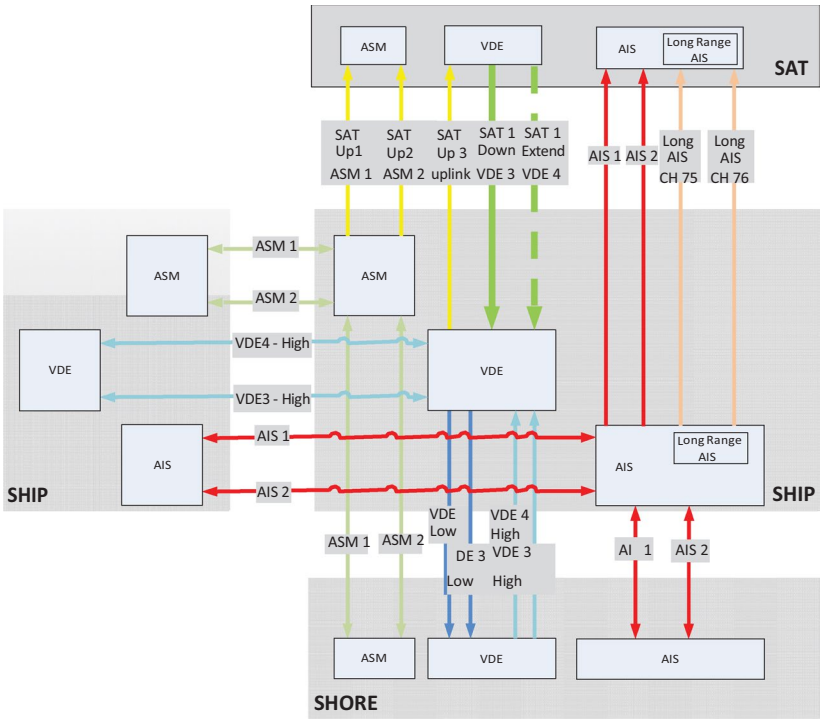

Fig. 14 VHF data exchange service system overview (refer [12])

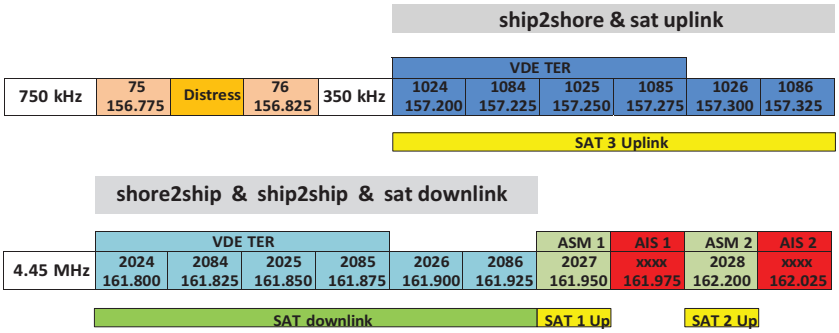

Fig. 15 Frequency allocation for the extended maritime mobile services

Table 9 Expected utilization of the programmable logic of the SoC with an implemented DVB-S standard

Resources	Shortcut	In use	Available	Utilization
DVB-S2 core				
Look up tables	LUTs	1487	106,400	1.5 %
Flip-flops	FF	2812	53200	5.3 %
Extensible block RAM	BRAMs	0	140	0.0 %
Programmable DSP Slices	DSPs	24	220	11.0 %
Reference design				
Look up tables	LUTs	20,002	106,400	18.8 %
Flip-flops	FF	12,644	53,200	23.77 %
Extensible block RAM	BRAMs	8	140	5.7 %
Programmable DSP slices	DSPs	69	220	31.6 %

Overall				
Expected	LUT	FF	BRAMs	DSP
Resources	21489	15456	8	83
Utilization	20.1 %	29.1 %	5.7 %	37.7 %

processor and the RF-Transceiver [16]. Moreover, a manufacturer like [17] has developed radios based on the same RF-Transceiver like the presented approach. All those commercial SDRs with an equivalent architecture were developed for non-specific environments, e.g., laboratory and offices and are basically designed for terrestrial applications. The SDR platform presented in this has been modified in size, weight, interfaces and performance to provide an initial position for further optimization to improve the usage on a small satellite in space. Furthermore, the design is optimized for detailed analysis of the signal behavior, either analog or digital.

To illustrate the usability, an AIS receiver has been implemented and evaluated as a first application example. The embedded AIS receiver solution has been discussed and the receiver sensitivity characterized. The RF-Transceiver is capable to receive and recover very low power signals at a level of around −117 dBm, so that the AIS receiver algorithm can correctly demodulate and decode AIS messages. Moreover, the ongoing development of a new standard in the maritime frequency bands, the VHF data exchange service, has been discussed. On the basis of [13], it has been demonstrated that the algorithms of digital video broadcasting standard for satellites (DVB-S2), which for example can be used in an extended version as an air interface of VDES, can be implemented into the baseband processor.

The intention of the presented SDR platform approach is to summarize different RF payloads, e.g., the already presented AIS in VHF, the Automatic-Dependent Surveillance (ADS-B) for airborne tracking in L-Band or spectral monitoring for different frequency bands, into a common design and decrease the mechanical dimensions, overall weight and power consumption. Furthermore, this SDR could be used as a communication subsystem on satellites and due to the high flexibility, either in baseband processing or operational frequency band, it can support standards for different ground stations. This advantage allows increasing the connectivity to the satellite and improves the amount of transmitted data.

Since this SDR approach is to be used as a satellite-based radio platform, it has been mentioned that there will be further investigations to develop a reliable system for the environmental conditions in space. The usage in space is the major driver to develop a customized SDR platform, since the commercial available radios with an equivalent architecture are not designed for the harsh conditions in space and not suitable for small satellites. Therefore, a next step in this project is to identify the general radiation behavior for a low earth orbit mission. Based on this study, a compromise of cost and reliability is to be done. Afterward, the presented design and architecture is going to be modified and improved. This re-design shall include the possibility to evaluate the radiation characteristics in particular for the fundamental components of the system, the RF-Transceiver and the SoC baseband processor, which are not available in a radiation-hard version.

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