NCTFET device and its applications in future VLSI

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Abstract:

NCTFET is a novel semiconductor device that has attracted considerable attention from the scientific fraternity since it offers the possibility of relaxing the fundamental limitations of conventional CMOS technology. The concept combines two concepts: ferroelectric materials for negative capacitance and tunnel field effect transistor (TFET) architecture. This device targets two major issues of VLSI: reducing power consumption with proper performance at low voltage levels.

Thus, the negative capacitance effect is introduced into the gate stack of the NCTFET by adding a ferroelectric layer that amplifies the gate voltage and leads to a subthreshold swing below the thermal limit of 60 mV/decade. This would enable NCTFETs to operate at lower supply voltages and significantly impact power dissipation. However, TFET architecture based on band-to-band tunneling allows one to achieve ultra-low leakage currents that contribute significantly to energy efficiency. We

have simulated all this in T-CAD. NCTFETs, being properly poised shortly for VLSI applications, will be a very critical enabler for ultra-low-power computing systems; they will become part and parcel of high-end wearable electronics, Internet of Things (IoT) devices, and advanced data centers. They will suit next-generation processors, memory technologies, as well as 3D integration, promising impressive energy efficiency while maintaining scalability. Nevertheless, NCTFETs would offer an opportunity for

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more power-efficient and high-performance computing architectures in an emerging application space like neuromorphic computing and artificial intelligence hardware. At present with further device scaling into the sub-10nm regime, NCTFETs are a promising route forward to extend Moore's Law as well as cater to the imminent challenges of future VLSI technology.

Keywords: Negative Capacitance Tunnel Field Effect Transistor (NC-TFET), CMOS technology, ferroelectric, T-CAD, Internet of Things (IoT).

1. Introduction

Since the semiconductor industry is vigorously pushing toward greater performance and lower power consumption, new bottlenecks have emerged from the traditional MOSFETs. While in recent years low-power, high-efficiency devices have not only grabbed much importance in consumer electronics but also crucial applications like wearables, IoT, and energy-efficient processors, novel transistor designs that break away from this paradigm are emerging. The Tunnel Field-Effect Transistor, using band-to-band tunnelling as a conduction mechanism, is one of the most promising alternatives and provides more advantages in ultra-low-power operation.

However, the subthreshold swing SS that TFETs experience causes them to have limitations in reducing this swing, which becomes a hindrance to their switching speed and efficiency at low voltages. A very recent breakthrough in this problem has been the development of a Negative Capacitance TFET (NC-TFET) that exhibits elements of TFET principles in combination with negative capacitance from ferroelectric materials. Integration will further improve TFETs, thus enabling quicker switching with less power consumption. Superior electrostatic control, very low voltage, and energy-efficient factors are guaranteed to make NC-TFETs highly prominent in the future of semiconductor devices.

It provides a detailed perception of NC-TFETs and encompasses some parts of their working mechanisms, structure, material selection, difficulties in their manufacturing, and applications in the shifting scenario of the semiconductor landscape.

2. Basics of Tunnel Field Effect Transistor (TFET)

2.1 Working Principle of TFET

In a TFET, quantum mechanical band-to-band tunneling mediates current flow through the device, in contrast to thermionic emission over a barrier, which is what dominates conventional MOSFETs. This mechanism affords subthreshold swings less than 60 mV/decade, a limit present in MOSFETs due to the Boltzmann distribution [1].

2.2 Band-to-Band Tunneling (BTBT)

The BTBT mechanism at the heart of TFET operations involves electrons in the valence band of the source region, influenced by a strong electric field and hence tunnel into the conduction band of the channel region. Since the gate voltage controls the width of the tunnel barrier, it makes it narrow, thereby controlling the tunneling current through the drain [2] Fig [1].

2.3 TFET Advantages

- **Low Subthreshold Swing (SS):** The subthreshold swing of below 60 mV/decade achieved by TFETs makes them a reality for ultra-low power switching.
- **Low Off-State Leakage:** TFETs are observed to have significantly lower off-state leakage current since it is based on tunneling rather than thermal emission.

2.4 TFET Challenges

- **Low ON-Current (ION _{ON} ON):** Generally, MOSFETs suffer from an inherently low ON-current as compared to their TFET counterparts since their tunneling probability is bounded by the width of the tunneling barrier and it cannot be easily reduced [3].
- **Material Constraints:** In contrast to MOSFET, TFETs rely on materials with very small band gaps and high tunneling efficiency, thereby limiting the scope of material choice.

3. Negative Capacitance Effect

Negative capacitance is the behavior of some ferroelectric materials that respond oppositely to the conventional expectation, that is, an increase in charge on the capacitor results in a reduction in voltage. This phenomenon is due to the intrinsic characteristics of ferroelectric materials, which yield non-linear polarization curves. Using Hafnium Zirconium Oxide (HZO), Lead Zirconate Titanate (PZT), or Barium Strontium Titanate (BST) as ferroelectric material, NC-TFETs take benefit from negative capacitance for the magnification of the gate voltage. In traditional transistors, the gate capacitance forms a voltage divider between the gate and the channel. By integrating a negative capacitance element into the gate stack, this divider is altered to provide voltage amplification at the channel. Essentially, the ferroelectric layer reduces the overall capacitance of the gate, which enhances the electrostatic control of the gate on the channel, thus enabling this device to switch at lower voltages. This is an important aspect in bringing down the subthreshold swing below the 60 mV/dec limit, thereby helping it to switch fast and utilize less power [4] Fig [2].

Such incorporation of negative capacitance into the gate stack of a TFET will lead to what is called NC-TFET-the enhancement in both power efficiency and switching speed.

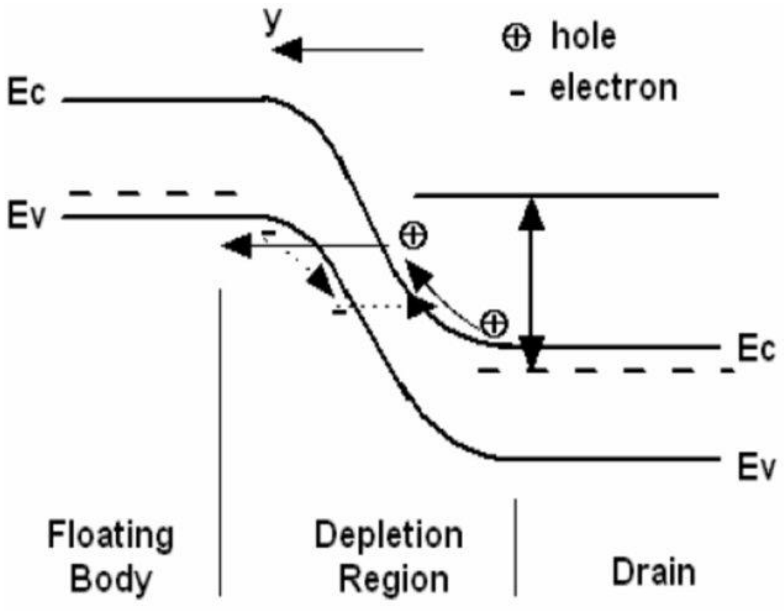

Figure 1: Band-to-Band Tunneling in TFET [10]

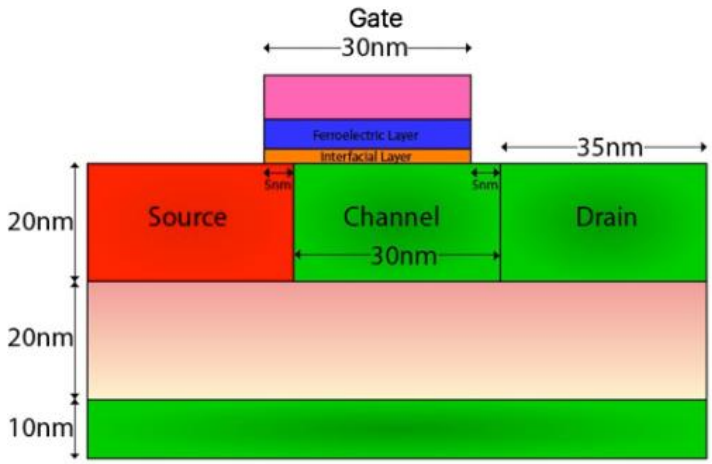

Figure 2: Negative Capacitance Effect in NC-TFET [11]

4.1 NC-TFET Device Architecture

The NC-TFET device structure is an extension of the conventional TFET with the significant difference being the inclusion of a ferroelectric material in the gate stack, which provides a layer that enables the generation of negative capacitance effects and thereby amplifies the control exerted by the gate on the channel [5] Fig [3].

4.1.1 Key Components of NC-TFET

1. **Source**: In the NC-TFET, the source region is heavily doped with p-type or n-type material, depending on the nature of the transistor being considered. Such heavy doping guarantees that the carrier will be available at the right energy level available for tunneling.

2. **Channel:** A thin channel of NC-TFET is formed using a narrow bandgap material to increase the probability of tunneling. Materials that can be used in the channel include

    - Silicon-Germanium (SiGe) has a smaller bandgap compared to silicon, which makes it easier for easier tunneling.
    - III-V compounds such as Indium Arsenide (InAs) or Gallium Antimonide (GaSb) have low band gaps but high mobility and efficient tunneling.

3. **Drain**: The source to drain is highly doped with the opposite type of carrier compared with the source; n-type for p-TFETs, and p-type for n-TFETs. A large voltage difference is created between the source and the drain to enhance tunneling through the bandgap process.

4. **Gate**: An NC-TFET gate typically consists of a high-k dielectric layer, combined with a ferroelectric material. The negative capacitance due to the ferroelectric material enhances the gate voltage and thus the electrostatic control over the channel. The channel's conductance is modulated by the gate and consequently controls the tunneling of charge carriers from the source to the drain.

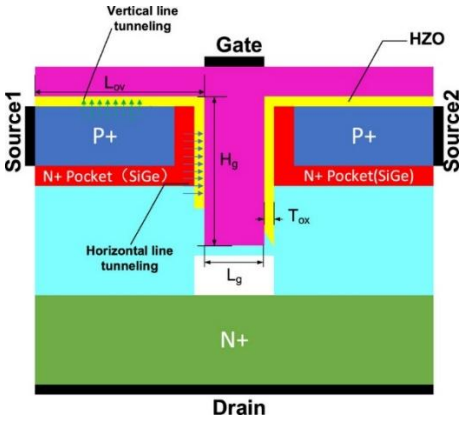

Figure 3: NC-TFET Device Structure [12]

4.1.2 Materials for Negative Capacitance

The choice of ferroelectric material is critical in achieving the negative capacitance effect as desired in NC-TFETs. Among the commonly used ferroelectric materials:

- **Hafnium Zirconium Oxide (HZO):** This is due to the reason that HZO retains all the benefits of being compatible with existing CMOS processes besides having the advantage of scaling down to smaller technology nodes.
- **Lead Zirconate Titanate (PZT):** PZT is one ferroelectric material that has been a focus for much research, even though it suffers from poor integration issues with more sophisticated semiconductor processes; it possesses good negative capacitance.

- **Barium Strontium Titanate (BST):** BST possesses good ferroelectric properties and therefore is used extensively in RF and memory applications.

Therefore, these materials should be engineered with great care in a manner that shows stable negative capacitance over a wide range of voltages and temperatures so that the NC-TFET works efficiently under various use cases.

5. Theoretical Benefits of NC-TFET

The integration of negative capacitance into TFETs introduces many advantageous concepts, especially concerning device performance and power efficiency.

5.1 Reduced Subthreshold Swing (SS)

It has been known that conventional MOSFETs are limited by the subthreshold swing of 60 mV/decade; this indicates that each drop in the gate voltage by 60 mV lowers the drain current by an order of magnitude. This restriction becomes a real challenge in designing devices that have to switch at lower voltages for low-power electronics. NC-TFETs can exploit negative capacitance to achieve subthreshold swings below 60 mV/decade. This finally leads to higher switching speeds and lower voltage operation, hence making NC-TFET suitable for ultra-low power applications Fig [4].

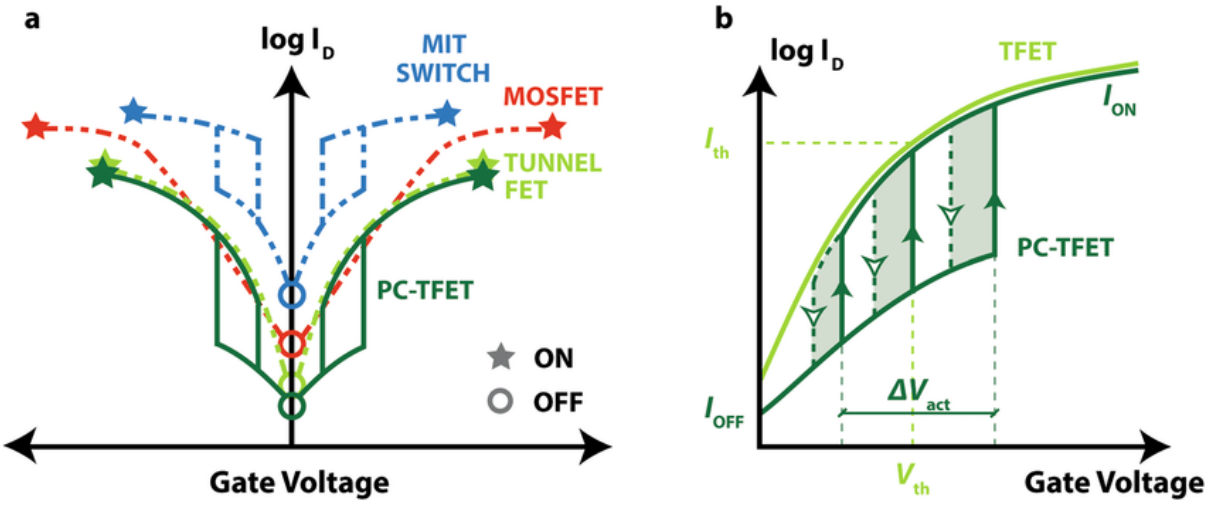

Figure 4: Subthreshold Swing Comparison between MOSFET, TFET, and NC-TFET [13]

5.2 Lower Power Consumption

One of the most attractive features of NC-TFETs is their ability to be operated at ultra-low supply voltages, VDD_{DD}DD. The superior electrostatic control provided by the ferroelectric material enables a device to turn on or off at much lower gate voltages, which translates directly to less power consumption. As such, NC-TFETs are extremely attractive for application regimes in which energy efficiency is paramount, such as portable and battery-powered devices [6].

5.3 Enhanced Scalability

SCEs become a dominant issue as the semiconductor devices are scaled down further. SCEs degrade the transistor performance as the ability of the gate in the control of the channel reduces due to the diminution of the length. NC-TFETs provide improved SCE immunity due to amplified gate control and hence have a brighter prospect for scaling into future technology nodes.

6. NC-TFET Fabrication and Process Integration

6.1 Challenges in Fabrication

Although theoretically attractive, the NC-TFET has various fabrication challenges that make its practical implementation difficult [7].

- **Ferroelectric Deposition:** High-precision deposition of a ferroelectric material is necessary when the ferroelectric material used in NC-TFET should be deposited uniformly and with reliable performance. Ferroelectric material thin films such as HZO need to be deposited using atomic layer deposition or other advanced techniques compatible with CMOS fabrication.
- **Material Stability:** The ferroelectric material must be stabilized in the negative capacitance values regardless of the long-term operation conditions such as temperature and voltage. Hence, this demands careful engineering so that the latter is long-term stable and reliable.

6.2 Integration with CMOS Processes

Another important aspect is the compatibility of NC-TFETs with traditional CMOS manufacturing processes. As the existing HZO material has been under strong development for advanced CMOS nodes, NC-TFETs can be added to the existing production lines with very minimal process modifications. They are a promising technology for future semiconductor products with less time and cost compared to adopting an entirely new device architecture [8].

7. Applications of NC-TFET

Since NC-TFETs can function at very low voltages and consume much less power, they are suitable for a wide range of applications Fig [5].

- **Wearable Devices:** NC-TFETs could be implemented to increase battery life in wearable electronics, so these devices can operate longer with similar performance levels.
- **Internet of Things (IoT):** IoT devices are often placed in an energy-constrained environment, which will make the low-power operation of NC-TFETs highly beneficial in prolonging the lifetimes of devices.
- **Ultra-Low-Power Microprocessors:** NC-TFETs can be incorporated into next-generation processors. Those are designed for low-power consumption. Among them are those in mobile computing, sensors, and medical implants.
- **Medical Devices:** High power and significant heat dissipation are critical for biosensors and medical implants. The ability to operate very efficiently NC-TFETs makes them optimal candidates for such applications wherein long-term performance and negligible interference with biological tissues are of great concern.

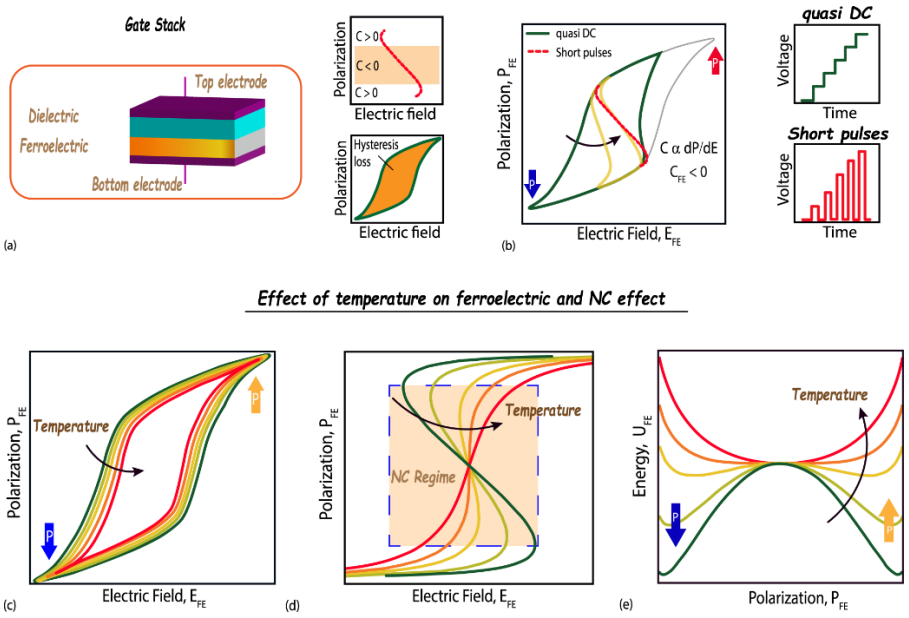

Figure 5: Power Efficiency in NC-TFET Applications [14]

8. Future Prospects and Research Directions

Whereas promising advancements in the NC-TFETs are indicated; however, several areas require more research and development also [9].

- **Optimizing Ferroelectric Materials:** Research is still going on with ferroelectric material that has more robust negative capacitance properties, in particular with the scaling of devices down to even smaller technology nodes.
- **Device Modeling:** It requires more complex models to predict the behavior of NC-TFETs under different situations, assuring reliable and predictable functionality for various applications.
- **Thermal Stability:** For stable negative capacitance in NC-TFETs, the ferroelectric materials have to be proven to withstand a range of temperatures, which is one of the biggest hurdles for practical use in stressed applications.

9. Conclusion

NC-TFET devices are a breakthrough in the development of transistor science, holding the path for scalings of MOSFETs with fundamental limitations. The combination of quantum mechanical tunneling with the negative capacitance effect in the NC-TFET realizes superior subthreshold swing together with reduced power consumption in a qualitatively different way from limited scalabilities. These features make the NC-TFET device the frontrunner in ultra-low-power electronics for future small-portable to large-scale integrated circuits applications. As the study regarding ferroelectric materials and the method of their fabrication advances, NC-TFETs will be seen more frequently in future semiconductor technology.

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