Chapter 1

Methodology

This research is divided into three parts as follows:

1. Research and timeline
2. Design of different system
3. Implementation and testings

This research will be developed using the following timeline.

Timeline Date	Objectives
By 15 April 2023	Designs of UART systems
By 22 April 2023	Designs of I2C and SPI systems
By 29 April 2023	Research designs of CPU Architecture
By 13 May 2023	Designs of CPU Architecture Implementations
By 20 May 2023	Designs of Interconnected systems

Table 1.1: Research Timeline Table (will be updated as progressed)

1.1 Requirements

1.1.1 Hardware and Software Requirements

Hardware and software requirements are as follow

1. Arrow Deca FPGA Development Board
2. Intel Quartus Prime Lite Software
3. ModelSim Lite simultation Software

1.1.2 Skill Requirements

The following skills are required.

1. VHDL Programming
2. Computer Organization and Designe for RISC-V ISA

3. Micro-controller Peripheral Design
4. Micro-controller Communication Design
5. Assembly for RISC-V ISA

1.2 Functional Block Diagram for Micro-controller

The detail block diagram for the micro-controller designed in this research is as follows

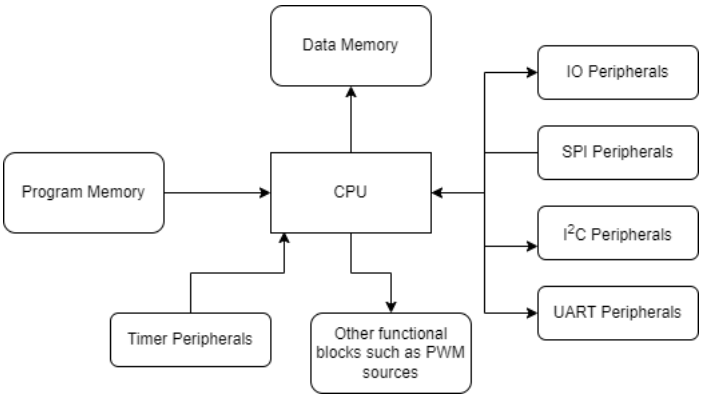

Figure 1.1: Functional Block Diagram for Micro-controller

1.3 Functional Block Diagram for CPU

The detail block diagram for the CPU designed in this research is as follows

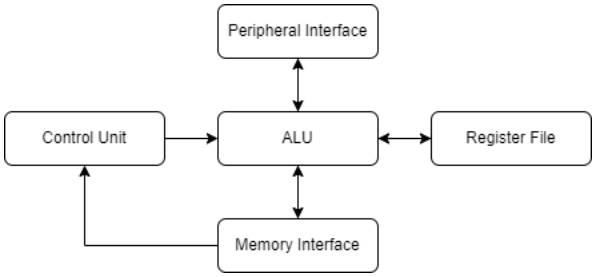

Figure 1.2: Functional Block Diagram for CPU