Chapter 1

Introduction

1.1 Introduction to the Project

This research explores the design and implementations for a micro-controller based on open-source RISC-V RV32E Instruction Set Architecture(ISA). This research concerns with detail designs of the CPU and peripherals, along with detail documentation for each module.

This project emphasizes on modularity with extensibilty on desired hardware and instruction sets. This research will be published on GitHub repository.

1.2 Project Background

On the web, a lot of projects and processors based on the popular RISC-V ISA can be found. However, only little information about detail implementations about the ISA is provided. This poses a challenge for students and researchers who want to explore implementation about the ISA.

In order to provide simple yet detailed implementation of the ISA, this research is introduced. Many open-source projects utilized Verilog HDL. This research will use VHDL, which is an industrial standard.

1.3 Aims and Objectives

This research is proposed for construction of RISC-V Hardware using VHDL and implemented on FPGA.

The objectives of this research are as follow.

1. To build a complete microcontroller, yet simple enough to follow, based on RISC-V RV32E ISA using VHDL.
2. To offer detail documentation of the implementation of the hardware
3. To offer hardware extension for future developement
4. To offer assemble for firmware creation
5. To offer implementation support for hardware designers to build their own hardwares based on the required projects

1.4 Expected Outcomes

The expected outcomes of the research are as follows

1. The CPU must work based on the specified ISA, in this case, RICS-V RV32E ISA
2. The CPU must be tested

3. The overall micro-controller must have standard peripherals and they must be tested
4. The documentation of all of the hardware implements must be provided
5. The research will be published on GitHub Repo

Chapter 2

Literature Review

Chapter 3

Methodology

This research is divided into three parts as follows:

1. Research and timeline
2. Design of different system
3. Implementation and testings

This research will be developed using the following timeline.

Timeline Date	Objectives
By 15 April 2023	Designs of UART systems
By 22 April 2023	Designs of I2C and SPI systems
By 29 April 2023	Research designs of CPU Architecture
By 13 May 2023	Designs of CPU Architecture Implementations
By 20 May 2023	Designs of Interconnected systems

3.1 Requirements

3.1.1 Hardware and Software Requirements

Hardware and software requirements are as follow

1. Arrow Deca FPGA Development Board
2. Intel Quartus Prime Lite Software
3. ModelSim Lite simultation Software

3.1.2 Skill Requirements

The following skills are required.

1. VHDL Programming
2. Computer Organization and Designe for RISC-V ISA
3. Micro-controller Peripheral Design
4. Micro-controller Communication Design
5. Assembly for RISC-V ISA

3.2 Functional Block Diagram for Micro-controller

The detail block diagram for the micro-controller designed in this research is as follows

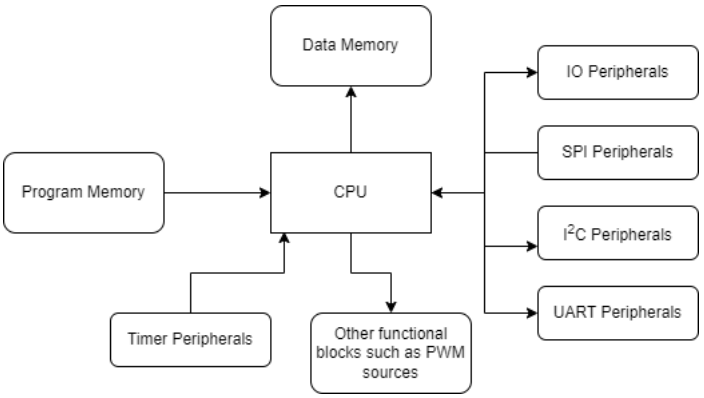

Figure 3.1: Functional Block Diagram for Micro-controller

3.3 Functional Block Diagram for CPU

The detail block diagram for the CPU designed in this research is as follows

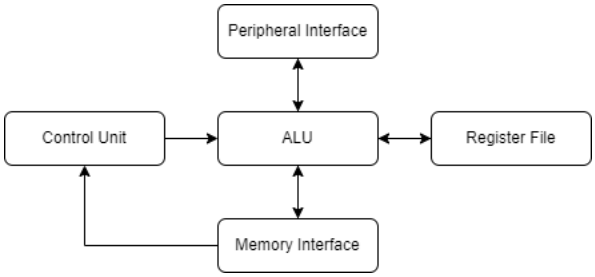

Figure 3.2: Functional Block Diagram for CPU

Chapter 4

Conclusion