\*注意port有沒有需要接(隨用法而改變)

1. 固定值

IDELAYE2 #(

.CINVCTRL\_SEL("FALSE"), // Enable dynamic clock inversion (FALSE, TRUE)

.DELAY\_SRC("DATAIN"), // Delay input (IDATAIN, DATAIN)

.HIGH\_PERFORMANCE\_MODE("FALSE"), // Reduced jitter ("TRUE"), Reduced power ("FALSE")

.IDELAY\_TYPE("FIXED"), // FIXED, VARIABLE, VAR\_LOAD, VAR\_LOAD\_PIPE

.IDELAY\_VALUE(32), // Input delay tap setting (0-31)

.PIPE\_SEL("FALSE"), // Select pipelined mode, FALSE, TRUE

.REFCLK\_FREQUENCY(200.0), // IDELAYCTRL clock input frequency in MHz (190.0-210.0, 290.0-310.0).

.SIGNAL\_PATTERN("DATA") // DATA, CLOCK input signal

)

IDELAYE2\_inst\_0 (

.CNTVALUEOUT(5'b0), // 5-bit output: Counter value output

.DATAOUT(FlashRdataL\_test\_d0), // 1-bit output: Delayed data output

.C(1'b0), // 1-bit input: Clock input

.CE(1'b0), // 1-bit input: Active high enable increment/decrement input

.CINVCTRL(1'b0), // 1-bit input: Dynamic clock inversion input

.CNTVALUEIN(5'b0), // 5-bit input: Counter value input

.DATAIN(FlashRdataL\_test0), // 1-bit input: Internal delay data input

.IDATAIN(1'b0), // 1-bit input: Data input from the I/O

.INC(1'b0), // 1-bit input: Increment / Decrement tap delay input

.LD(1'b0), // 1-bit input: Load IDELAY\_VALUE input

.LDPIPEEN(1'b0), // 1-bit input: Enable PIPELINE register to load data input

.REGRST(1'b0) // 1-bit input: Active-high reset tap-delay input

);

1. 用counter

IDELAYE2 #(

.CINVCTRL\_SEL("FALSE"), // Enable dynamic clock inversion (FALSE, TRUE)

.DELAY\_SRC("DATAIN"), // Delay input (IDATAIN, DATAIN)

.HIGH\_PERFORMANCE\_MODE("FALSE"), // Reduced jitter ("TRUE"), Reduced power ("FALSE")

.IDELAY\_TYPE("VAR\_LOAD"), // FIXED, VARIABLE, VAR\_LOAD, VAR\_LOAD\_PIPE

.IDELAY\_VALUE(0), // Input delay tap setting (0-31)

.PIPE\_SEL("FALSE"), // Select pipelined mode, FALSE, TRUE

.REFCLK\_FREQUENCY(200.0), // IDELAYCTRL clock input frequency in MHz (190.0-210.0, 290.0-310.0).

.SIGNAL\_PATTERN("DATA") // DATA, CLOCK input signal

)

IDELAYE2\_inst (

.CNTVALUEOUT(cnt\_value), // 5-bit output: Counter value output

.DATAOUT(DOUT), // 1-bit output: Delayed data output

.C(F200M), // 1-bit input: Clock input

.CE(1'b0), // 1-bit input: Active high enable increment/decrement input

.CINVCTRL(1'b0), // 1-bit input: Dynamic clock inversion input

.CNTVALUEIN(CNTVALUEIN), // 5-bit input: Counter value input

.DATAIN(DIN\_pre), // 1-bit input: Internal delay data input

.IDATAIN(1'b0), // 1-bit input: Data input from the I/O

.INC(1'b0), // 1-bit input: Increment / Decrement tap delay input

.LD(1'b1), // 1-bit input: Load IDELAY\_VALUE input

.LDPIPEEN(1'b0), // 1-bit input: Enable PIPELINE register to load data input

.REGRST(1'b0) // 1-bit input: Active-high reset tap-delay input

);