1st NEI Workshop
On

DESIGNING OF CMOS ANALOG CIRCUITS

June 11- 22, 2012

Organized by

Network of Engineering Institutions (NEI)

A consortium of four premier institutes:

The LNM Institute of Information Technology (LNMIIT), Jaipur
Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), Gandhinagar
Mody Institute of Technology and Science (MITS), Lakshmangarh
Yashwantrao Chavan College of Engineering (YCCE), Nagpur

Hosted by

Dhirubhai Ambani Institute of Information & Communication Technology, Gandhinagar

Introduction

The Network of Engineering Institutions (NEI) has been founded with a collaborative effort of the participating institutions, to promote cutting edge research in the field of VLSI for achieving indigenous chip designing and fabrication capabilities in India. The cooperative research program envisages a network of engineering colleges, universities and other institutes, coupled to a networked panel of experts, who would be responsible for continuous monitoring and guidance of the research program.

To promote the idea, every year the NEI will organize two workshops on specialized areas of VLSI designing and semiconductor technology. The first workshop in this series will be held at Dhirubhai Ambani Institute of Information & Communication Technology, Gandhinagar during June 11-22, 2012.

This short term workshop will offer, along with stimulating lectures by renowned experts in this area, a rare opportunity to gather hands-on experience in designing of CMOS analog circuits. The program will also provide a forum for professional interaction between VLSI experts, faculties, researchers, and students, which would hopefully lead to useful research collaboration amongst the participating institutions in due course of time.

Course Contents

1. Physics of Semiconductor Devices (Lecture - 18 hours):

Band theory, Continuity equation, P-N junction: zero and reverse bias, forward bias, capacitance, Metal-semiconductor contacts, MOS capacitor, BJTs & MOSFETs.

2. CMOS Analog Circuit Design (Lecture - 35 hours, Lab - 15 hours):

The main objective of this course is to learn how to analyze and design CMOS analog amplifier circuits. The emphasis will be on circuit design, and in every phase of the course, the learner will be expected to design, on paper as well as in simulation, the circuits discussed in the lectures.

This course will broadly cover the following topics: MOS transistors: physics, modeling and layout; Common-source amplifier: current source load, diode load, frequency response, design; Cascode amplifier, Common-gate and common-drain amplifiers; Differential amplifier: dc and ac analysis, design; Current mirrors: basic, cascode, active, advanced; Opamps: one stage, two stage, CMFB, design; Stability and compensation, Parameter variations, Advanced amplifiers: high slew-rate, rail-to-rail, low power; Advanced Topics: D/A Converters, Types of Noise and its statistical characteristics, circuit representation, introduction to RF Design.

Evaluation Scheme

All registered participants of the workshop will receive a *Certificate of Participation* at the end of the workshop. PhD students (Category 1a and 1c, in Table-I) will be graded through regular exams and will receive a transcript at the end of the workshop.

Speakers

Prof. R. Sharan (Distinguished Professor LNMIIT, Ex-professor IIT Kanpur)

Prof. Dipankar Nagchoudhuri (DA-IICT, Ex-professor IIT Delhi)

Prof. Dinesh Sharma (IIT Bombay)

Prof. Chetan Parikh (DA-IICT, Ex-professor IIT Bombay)

Prof. Subhajit Sen (DA-IICT)

Who can attend?

The workshop will be useful for PhD scholars, faculties from engineering colleges/technical institutions/universities, and M.S./M.Tech./M.Sc./B.Tech. students, who are interested in enriching knowledge in CMOS analog circuit design and Solid state devices. The program will also be helpful for engineers from industry and research organizations who want to have a savor of modern trends in CMOS analog circuit design.

Workshop Fees

Note: Accommodation is not included in the following fee. The fee includes food (lunch & dinner) and tea & snack (twice daily)

Table-I

Occupation	Category No.			Workshop Fee (If registration & DD received by 31st March 2012)	Workshop Fee (If registration & DD received by 15th April 2012)	Workshop Fee (If registration & DD received by 30th April 2012)	Workshop Fee (If registration & DD received by 15th May 2012)	Workshop Fee (If registration & DD received by 31st May 2012)
PhD Student	1a	NEI member institutions	Enrolled under *NEI's PhD program for VLSI*	Free	Free	Free	Free	Free
	1b		Not enrolled under *NEI's PhD program for VLSI*	Free	Free	Free	Free	Free
	1c	Non-NEI institution	-	Rs. 10,000	Rs. 11,000	Rs. 12,000	Rs. 14,000	Rs. 16,000
Faculty	2a	NEI member institutions	-	Free	Free	Free	Free	Free
	2b	Non-NEI institution	-	Rs. 10,000	Rs. 11,000	Rs. 12,000	Rs. 14,000	Rs. 16,000
B.Tech. or M.Tech or M.Sc. Student	3a	DA-IICT*	-	Free	Free	Free	Free	Free
	3b	NEI member institutions (except DA-IICT)	-	Rs. 10,000	Rs. 11,000	Rs. 12,000	Rs. 14,000	Rs. 16,000
	3c	Non-NEI institution	-	Rs. 20,000	Rs. 21,000	Rs. 22,000	Rs. 24,000	Rs. 26,000
Industry or Research Organization	4	-	-	Rs. 25,000	Rs. 26,000	Rs. 27,000	Rs. 29,000	Rs. 31,000

* These students will have to become volunteers

After 31st May 2012, only on-site registrations will be considered, subject to availability of seats.

Food and Accommodation

Food (Tea & snacks, lunch and dinner) will be provided to all registered participants. The workshop fee includes the cost of food. The workshop fee does NOT include accommodation. Accommodation needs to be arranged on your own; information about nearby hotels is provided on the website http://nei.daiict.ac.in/

Traveling Allowance

Traveling allowance will NOT be provided to the participants.

How to apply

Send a filled-in registration form (attached herewith) or downloaded from the link: http://nei.daiict.ac.in/ along with the appropriate fee (indicated in Table-I) in the form of DD in favour of **Network of Engineering Institutions**, payable at Gandhinagar, to the postal Address given in this form. Your registration will be accepted, provided there are enough seats available. A decision will be emailed to you regarding the same. Incase your registration is not accepted due to unavailability of seats, your DD will be returned to you by courier.

Contacts

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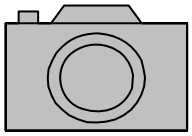
Faculty Block-4, Room 4206,
Nr. Indroda Circle,
Gandhinagar, 382007, GUJARAT

1st NEI Workshop On **DESIGNING OF CMOS ANALOG CIRCUITS** hosted by DA-IICT (June 11-22, 2012)

Registration Form

Paste your passport size photo here**



Name of Applicant (In block letters):**

_____

Sex (M/F): _____ Age: _____ Nationality: _____

Name and address of Institute/University/Organization/Employer:

_____

_____

_____

_____

Designation/Occupation: _____ Category No.: _____ (see Table-I)

Student ID No. (if student): _____ Current Degree program (if student): _____

Educational Qualifications (starting with highest degree)

Degree	College/University	Month/year of Degree	Percentage / Class / GPA / CPI

Address for Communication:

_____

_____

_____

City: _____ State: _____ Pin: _____

***Email: _____**

Fax: _____

Phone No: _____ Mob No: _____

Demand Draft Details:

Amount: ₹ _____

DD No: _____

Bank: _____

Branch: _____

Date of Issue: _____

_____

Signature of the Applicant **Date: _____**

***Note: You must provide email id. All future communications would be done through email.**
****Note: Staple/paste a recent passport size photo on the top right hand corner of this form.**

Postal Address (Send this form and DD to this address):

Prof. Mazad S. Zaveri,
Dhirubhai Ambani Institute of Information and Communication Technology,
Faculty Block-4, Room 4206, Nr. Indroda Circle, Gandhinagar, 382007, GUJARAT