PROJECT 1

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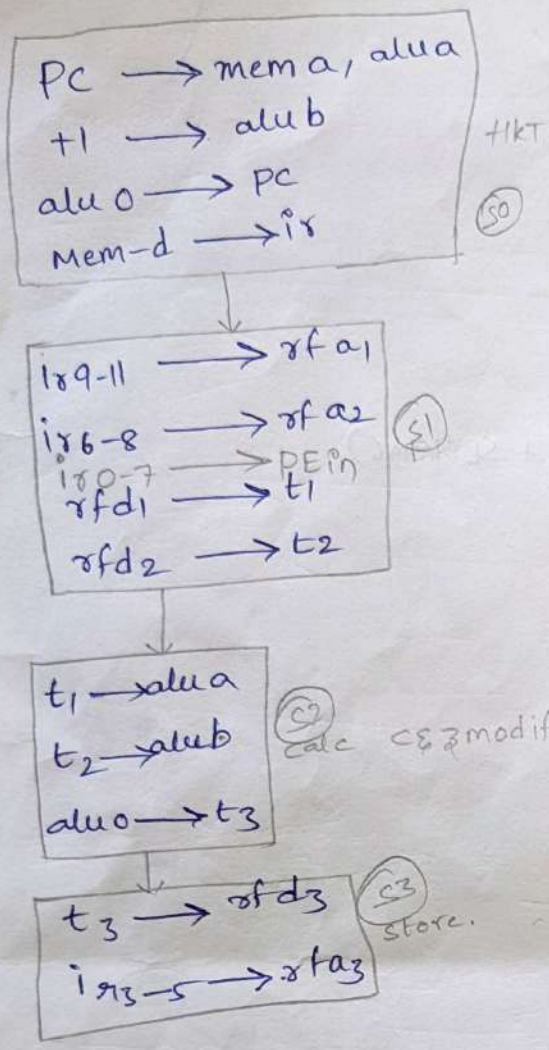
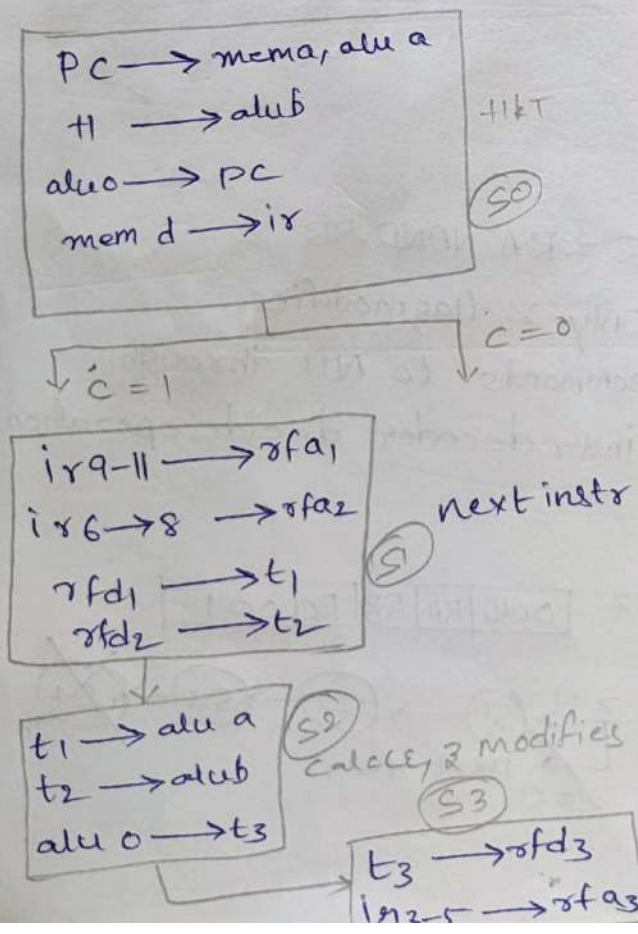
① ADD | 0001 | RA | RB | RC | 000 |
15 12 11 9 8 6 5 3 2 0

Rc = RA + RB & C & Z modifies.



② ADC | 0001 | RA | RB | RC | 010 |

if C = 1 Rc = RA + RB modifies C & Z



③ ADZ | 0001 | RA | RB | RC | 001 |

if Z = 1 RC = RA + RB Same as ②

But in place of 'C' in Br instr its 'Z'

④ ADL

0001	RA	RB	RC	011

one bit left shift of RB & then RC = RA + RB

S5:
- $ir_{9-11} \rightarrow rfa_1$
- $ir_{6-8} \rightarrow rfA_2$
- $rfd_1 \rightarrow t_1$
- $rfd_2 \rightarrow LS1 \rightarrow t_2$

⑤ ADI

0000	RA	RB	imm6

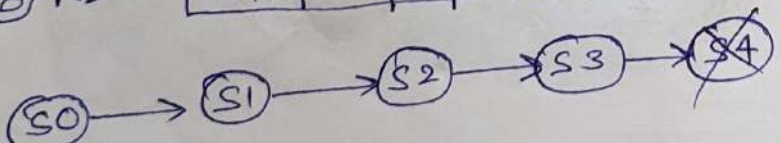
RB = RA + SE(imm6)

S6:
- $ir_{9-11} \rightarrow rfa_1$
- $ir_{0-5} \rightarrow SE6 \rightarrow t_2$
- $rfd_1 \rightarrow t_1$

S7:
- $t_3 \rightarrow rfd_3$
- $ir_{6-8} \rightarrow rfa_3$

⑥ NDU

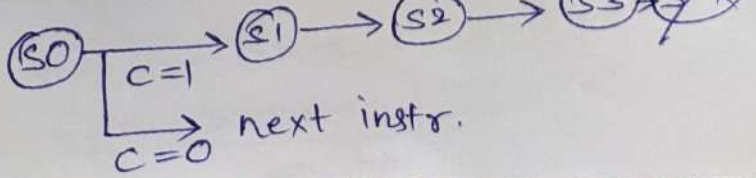
0010	RA	RB	RC	000



RC = RA . NAND . RB
Only z flag modifies
commands to ALU through
instr decoder decides operation.

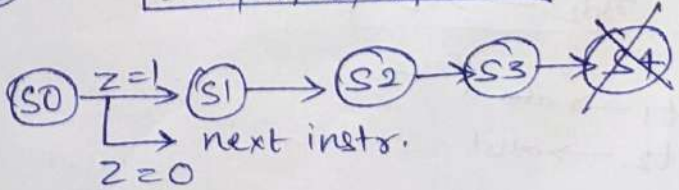
⑦ NDC

0010	RA	RB	RC	010

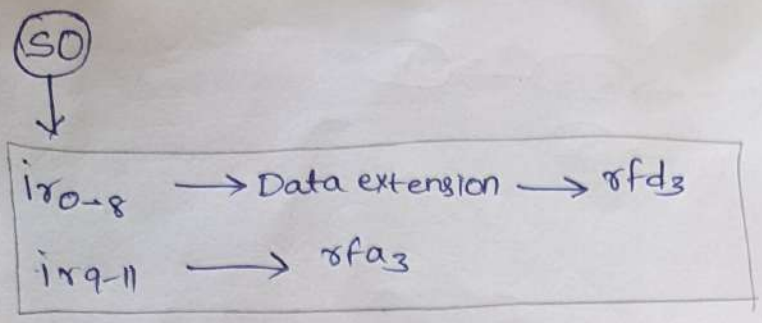


⑧ ND2

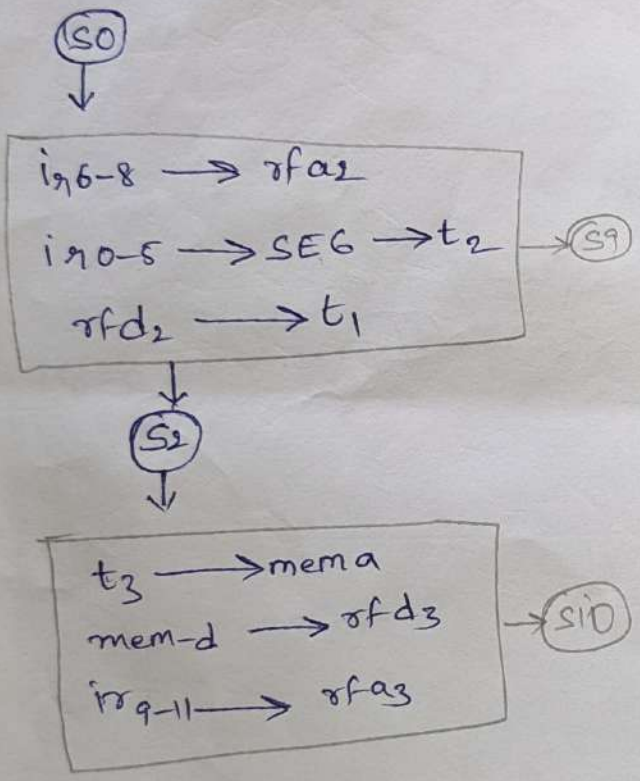
0010	RA	RB	RC	001



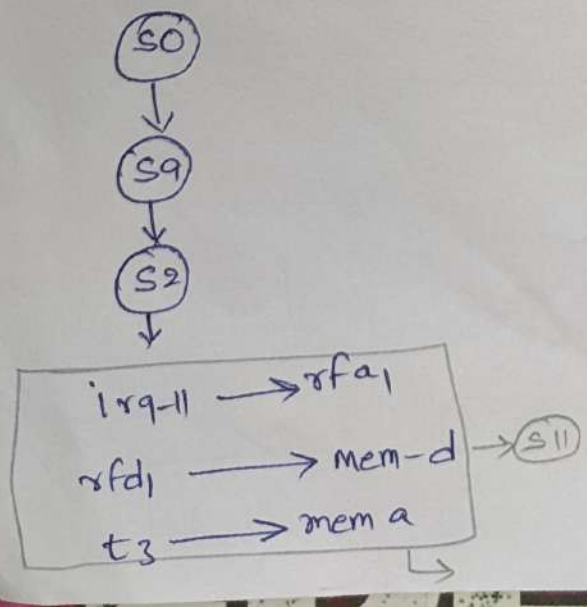
9) LHI | 0000 0011 | RA | 9bit imm



10) LW | 0111 | RA | RB | imm6 | RA = [[RB] + SE(imm6)]

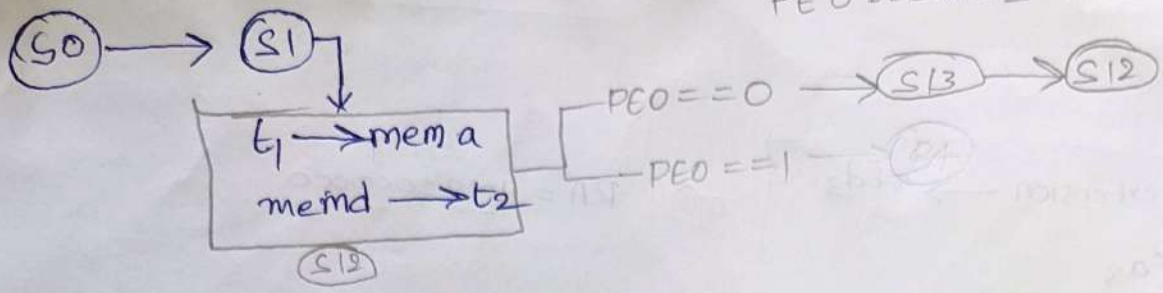


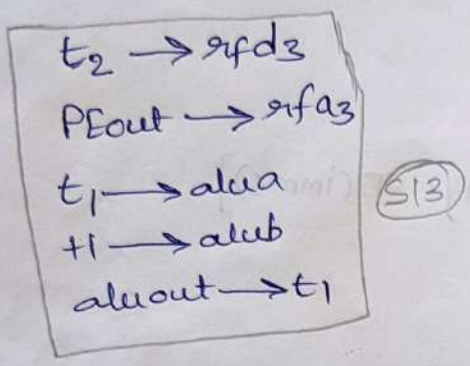
11) SW | 0101 | RA | RB | imm6 | [[RB] + SE(imm6)] = RA



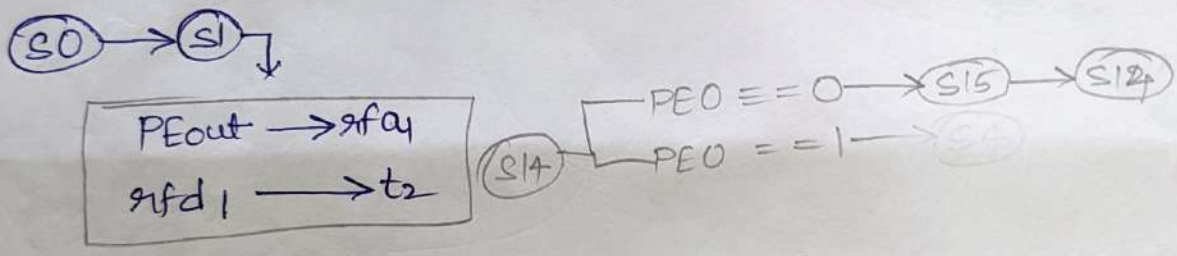
(12) LM | 1100 | RA | 0+8bits corresponding to Reg R_0 to R_7 (R to L) |

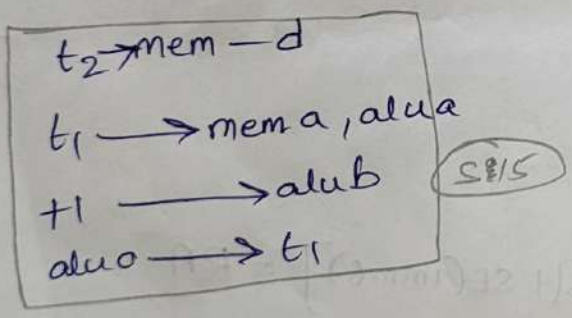
PE 0 becomes 1 when all are 0





(13) SM | 1101 | RA | 0+8bits corresponding to R_0 to R_7 (R to L) |

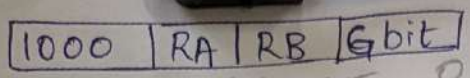


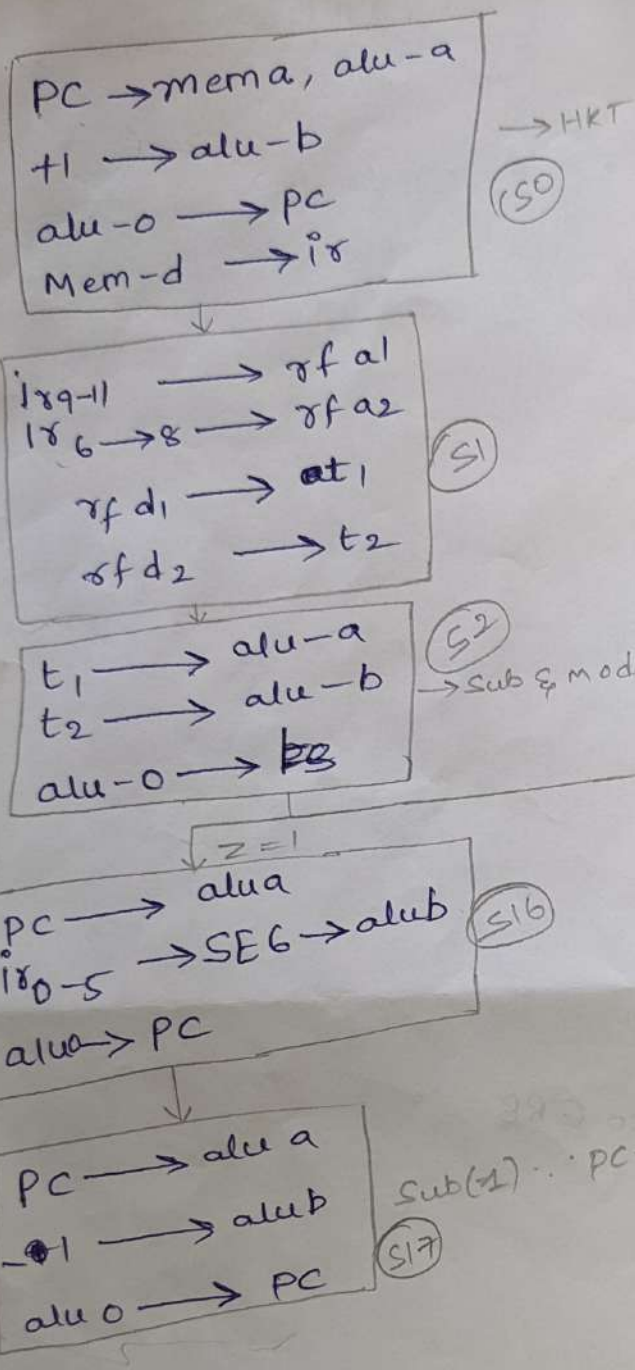


(S4) ~~if R7 changes then R7 $\rightarrow$ PC~~
~~O.W PC $\rightarrow$ R7~~

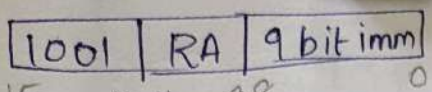
A

BEQ

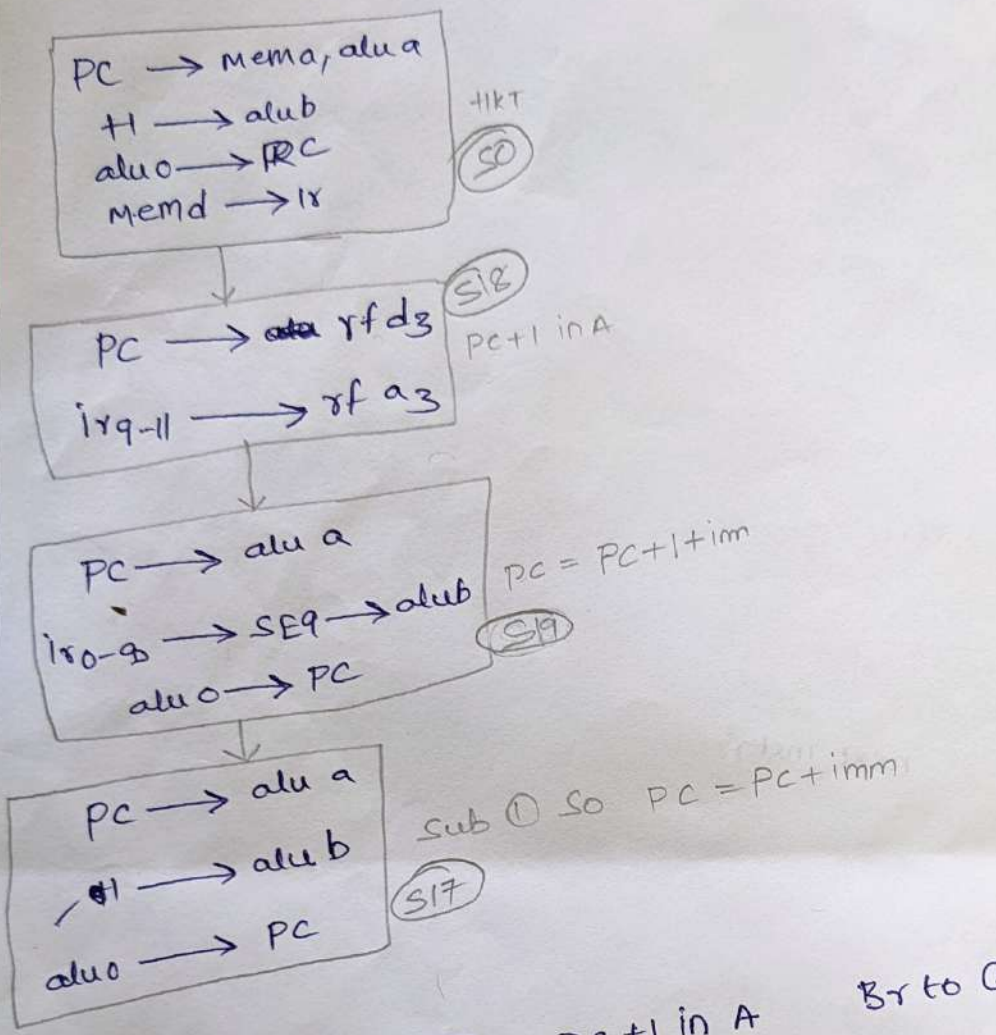

1000
RA
RB
6bit
15
12 11
9 8
6 5
0


PC → mem a, alu-a
+1 → alu-b
alu-o → PC
Mem-d → ir
→ HKT
S0
ir 9-11 → rf a1
ir 6→8 → rf a2
rf d1 → t1
rf d2 → t2
S1
t1 → alu-a
t2 → alu-b
alu-o → rb
S2
→ sub & modifies zero flag
z=1
z=0
next instr
PC → alu a
ir 0-5 → SE6 → alu b
alu → PC
S16
PC → alu a
-1 → alu b
alu o → PC
S17
sub(-1) ... PC + imm6

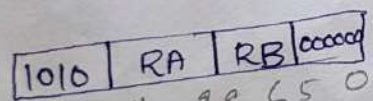
JAL 15



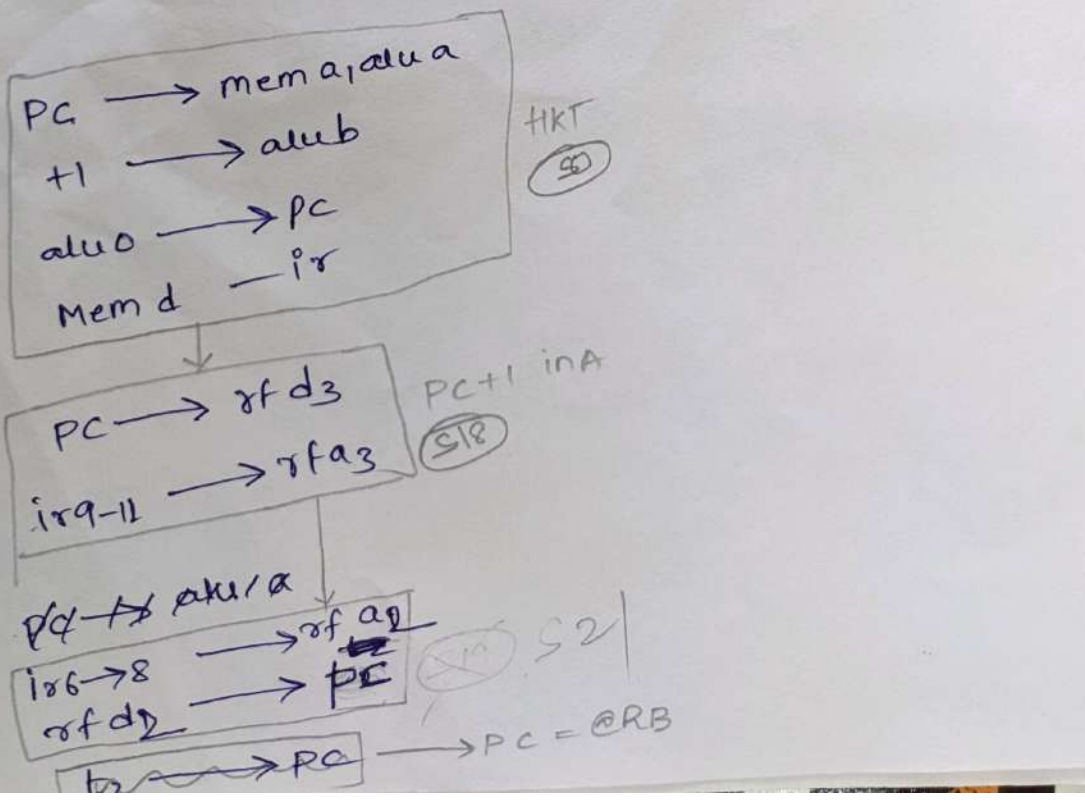
PC + imm → Branch
PC+1 in A



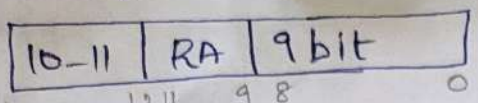
JLR 16

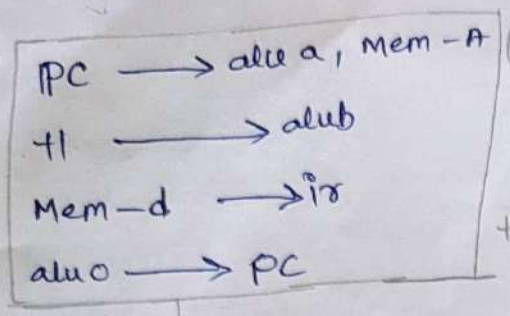


PC+1 in A
Br to @RB



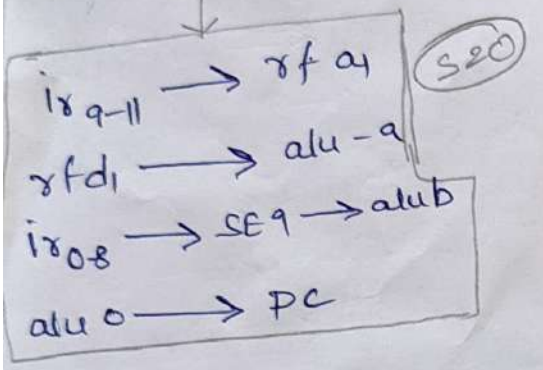
JRI -17





(1)

→ PC = PC+1 NOP No issues ∴ we are Modifying any way. (+0 dec states)



S20

add @RA + imm
Cnd move to PC.

* Things connected to rfa_1 & rfa_2 :-

$ir_{9-11} \longrightarrow rfa_1$

$PEout \longrightarrow rfa_1$

$ir_{6-8} \longrightarrow rfa_2$

* connected to rfa_3

$ir_{3-5} \longrightarrow rfa_3$

$ir_{6-8} \longrightarrow rfa_3$

$ir_{9-11} \longrightarrow rfa_3$

$PEout \longrightarrow rfa_3$

* connected to rfd_3

$t_3 \longrightarrow rfd_3$

$ir_{0-8}-DE \longrightarrow rfd_3$

$memd \longrightarrow rfd_3$

$PC \longrightarrow rfd_3$

$t_2 \longrightarrow rfd_3$

* connected to PC

$alu_0 \longrightarrow PC$

$rfd_2 \longrightarrow PC$

* connected to t_1

$rfd_1 \longrightarrow t_1$

$rfd_2 \longrightarrow t_1$

$alu_0 \longrightarrow t_1$

* connected to t_2

$rfd_2 \longrightarrow t_2$

$rfd_2 \longrightarrow LS1 \longrightarrow t_2$

$rfd_1 \longrightarrow t_2$

$memd \longrightarrow t_2$

$ir_{0-5} \longrightarrow SE6 \longrightarrow t_2$

* connected to t_3

$alu_0 \longrightarrow t_3$

alu a

$PC \longrightarrow alua$

$t_1 \longrightarrow alua$

$rfd_1 \longrightarrow alua$

alu b

$t_1 \longrightarrow alub$

$t_2 \longrightarrow alub$

$-1 \longrightarrow alub$

$ir_{0-5} \longrightarrow SE6 \longrightarrow alub$

$ir_{0-8} \longrightarrow SE9 \longrightarrow alub$

mem a

$PC \longrightarrow mema$

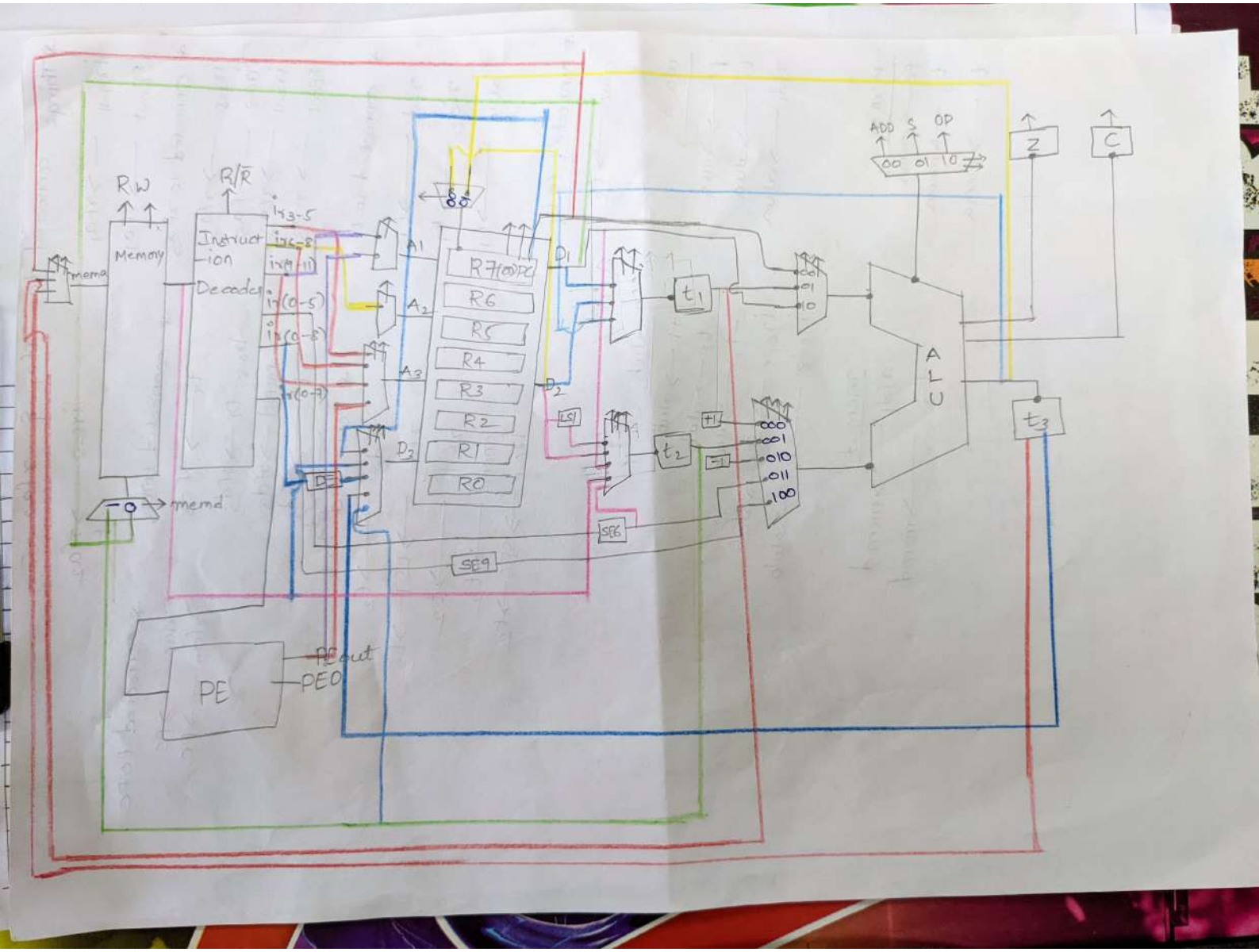
$t_3 \longrightarrow mema$

$t_1 \longrightarrow mema$

mem d

$rfd_1 \longrightarrow memd$

$t_2 \longrightarrow memd$


R/W
R/$\bar{R}$
Memory
Instruct
-ion
Decoder
mem_a
mem_d
i_{3-5}
i_{6-8}
i_{8-11}
$i_{(0-5)}$
$i_{(0-8)}$
$i_{(0-7)}$
A1
A2
A3
D1
D2
D3
80
R7(PC)
R6
R5
R4
R3
R2
R1
R0
LSI
SE6
SE9
t_1
t_2
t_3
+1
-1
000
001
010
011
100
001
01
10
ALU
ADD
S
OP
00 01 10
Z
C
PE
PEout
PEO

Controls

	R	W	Mem	mgn	A_1	A_2	A_3	IR	D_3	PC	RW (RF)	T_1	T_2	alu b	alua	alu	Z	C
S0	1	0	00	X	X	X	XX	1	XXX	01	00	XX	XXX	000	00	00	0	0
S1	0	0	XX	X	0	0	XX	0	XXX	11	10	00	001	111	11	11	0	0
S2	0	0	XX	X	X	X	XX	0	XXX	11	00	XX	XXX	001	01	10	1	1
S3	0	0	XX	X	X	X	00	0	011	11	01	XX	XXX	111	11	11	0	0
S5	0	0	XX	X	0	0	XX	0	XXX	11	10	00	000	111	11	11	0	0
S6	0	0	XX	X	0	X	XX	0	XXX	11	10	00	100	111	11	11	0	0
S7	0	0	XX	X	0	0	01	0	01	11	01	XX	XXX	111	11	11	0	0
S8	0	0	XX	X	X	X	10	0	010	11	01	XX	XXX	111	11	11	0	0
S9	0	0	XX	X	X	0	XX	0	XX	11	10	01	100	111	11	11	0	0
S10	1	0	10	X	X	X	10	0	001	11	01	XX	XXX	111	11	11	0	0
S11	0	1	10	0	0	X	XX	0	XXX	11	10	XX	XXX	111	11	11	0	0
S12	1	0	01	X	X	X	XX	0	XXX	11	00	XX	011	111	11	11	0	0
S13	0	0	XX	X	X	X	11	0	100	11	01	10	XXX	000	01	00	0	0
S14	0	0	XX	X	1	X	XX	0	XXX	11	10	XX	010	111	11	11	0	0
S15	0	1	01	1	X	X	XX	0	XXX	11	00	XX	XXX	000	01	00	0	0
S16	0	0	XX	X	X	X	XX	0	XXX	01	00	XX	XXX	011	00	00	0	0
S17	0	0	XX	X	X	X	XX	0	XXX	01	00	XX	XXX	010	00	00	0	0
S18	0	0	XX	X	X	X	10	0	000	11	00	XX	XXX	111	11	11	0	0
S19	0	0	XX	X	X	0	XX	0	XXX	00	00	XX	XXX	111	11	11	0	0
S20	0	0	XX	X	0	X	XX	0	XXX	01	00	XX	XXX	100	10	00	0	0
S21	0	0	XX	X	X	0	XX	0	XXX	01	00	XX	XXX	111	11	11	0	0

Total unique states = 21

Total control signals = 31