

Sr. No.	Test Case Name	Test Case Detail	Expected Result
1	stability_with_changing_clk	Change the clock frequency dynamically during operation and perform read/write operations.	RAM should function correctly at different clock frequencies without data loss or corruption.
2	rst_during_wr_rd	Write data to a specific address. Assert 'rst' signal during the write operation. Again, write data to the address and assert 'rst' signal.	Data should be handled according to the design specs. Typically data should be cleared or retained depending on the reset behavior defined in design.
3	single_wr_rd	Write to a single address and read from the same address but not simultaneously.	Data read from the address should match the data written to it.
4	multiple_wr_rd	Write to multiple addresses and read from the same addresses.	Data read from each address should match data written to it.
5	random_wr_rd	Write to and read from randomly selected addresses.	Data read from each address should match data written to it.
6	back_to_back_wr_rd	Perform back to back write or read operations on the different addresses	Each read operation should return the correct data written in the previous state operation.
7	error_handling	Perform write/read operations with addresses outside the valid range. Check data integrity and error signal.	Error signal should be asserted for invalid address operation. Data should not be corrupted.

Pass/Fail	Comments
	Verify if the 'rst' clears the data or retains it, as per design specification.
	Avoid 'X' and 'Z' in data