From: Nikul Mevada
Sent: 01 July 2024 19:39
To: Kaushal Baldevbhai Patel
Cc: Disha Kalpeshbhai Purohit
Subject: Verilog Project: Single Port RAM

Hi @Kaushal Baldevbhai Patel

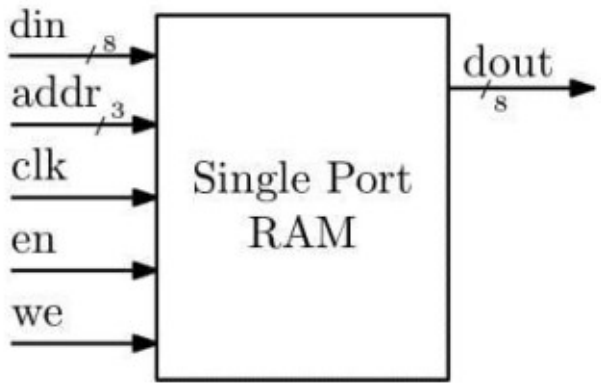
Please consider below requirements for single port RAM design and verification.

Topic : Design RTL and test-bench of Single port RAM with Handshaking mechanism using Verilog.

Description:

Random Access Memory (RAM) blocks are used to store data temporarily in digital system. In a single port RAM, writing and reading can be done through one port only. It has one en input and we input. When en and we are both high, data are written into RAM and if en is high but we is low, reading through RAM can be done.

Configuration : ADDR_WIDTH=5, DATA_WIDTH =32, MEM_DEPTH=32.



Add more signals, `valid`, `ready`, and `error`, in the above figure for a handshaking mechanism and error reporting.

Thank you,
Nikul