Daily Practice Problems:
Addressing Modes

Question 1

- Consider a PC-relative mode type branch instruction which takes branch on address 770 in memory. The instruction has offset value 150. What is the address of this instruction in memory, if each instruction is stored in memory on 4 locations?

Question 2

- The instruction POP uses which type of addressing mode?

Question 3

- An instruction is stored at Location X with its address field at location $X+1$. The address field has the value Y. A processor register contains the number Z. Evaluate the effective address, if addressing mode is:

  1. Direct

  2. Immediate

  3. Relative

  4. Register Indirect

Question 4

Consider a three word machine instruction

ADD A[R0], @ B

The first operand (destination) "A [R0]" uses indexed addressing mode with R0 as the index register. The second operand (source) "@ B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

Assume it takes 1 memory cycle to access 1 word form memory, further assume that each address and operand is of 1 word then, number of memory cycles needed to execute the above instruction is?

Question 5

- For the very first operand access among the table of content in _____ addressing mode, the operand accessed is same as register indirect mode?

a) Auto-increment mode

b) Auto-Decrement mode

c) Register mode

d) Indexed Register Mode

Question 6

- What happens in execution phase of branch instruction?

Question 7

- For branch type of instructions effective address only is calculated when the branch should be taken, otherwise not.

True/False?

Question 8

- How Relative addressing mode can work in 4-address instructions?

Question 9

- Consider a 2-word instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words and main memory takes 50ns for 1-word access.

Total memory access time required in:

1. Fetch cycle of instruction

2. Execution cycle of instruction

3. Instruction cycle of instruction

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