

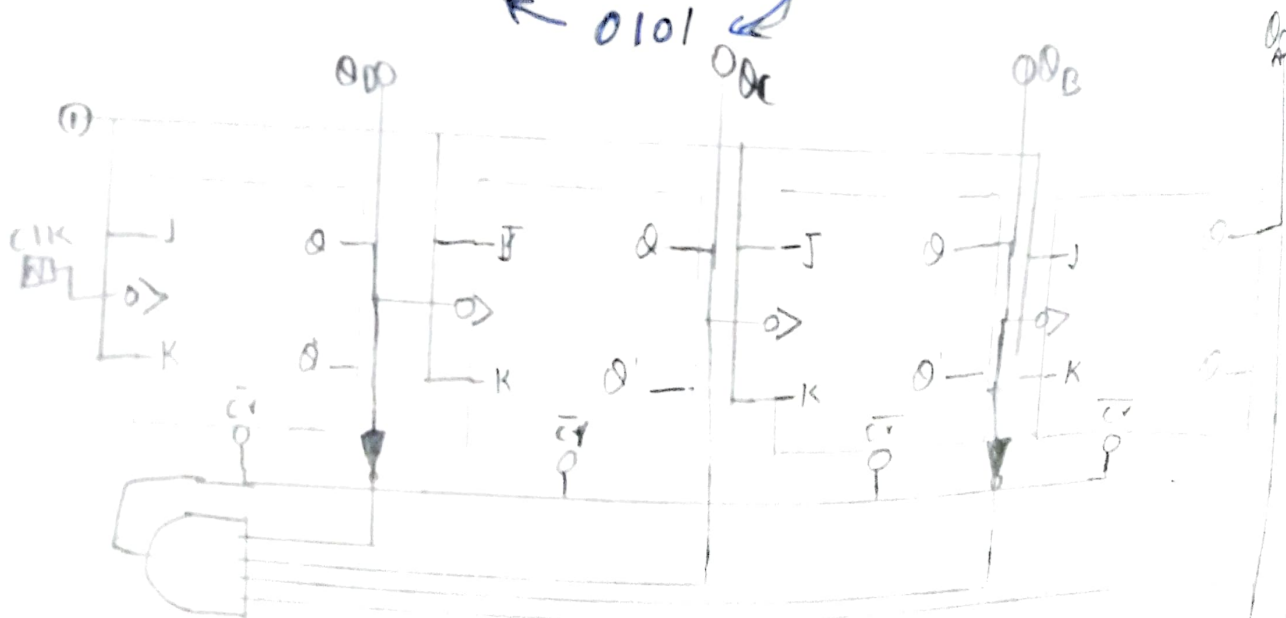
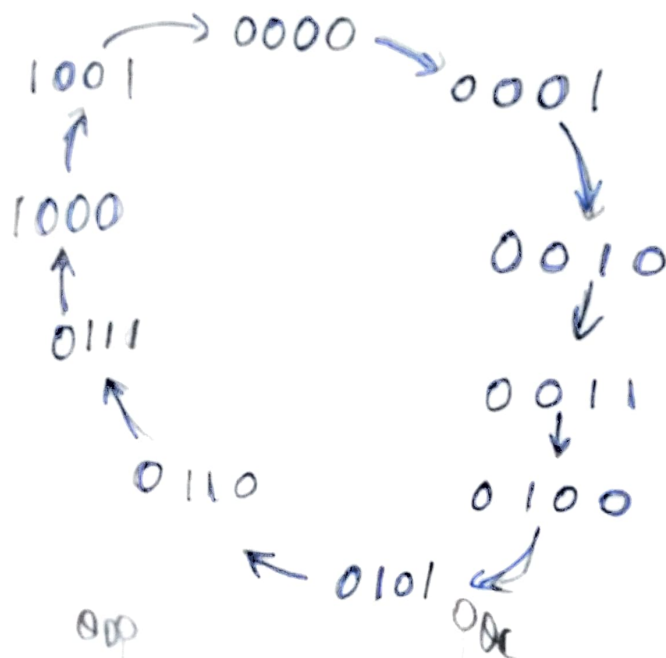
Date: 16/2/21

Aim: Design a decade asynchronous up counter

Apparatus:

1. J-K flip flop - 1C7473 - 1C7476
2. Not gate - 2.
3. AND gate - 1

State diagram:



Practical Procedure:

- 1) IC's are placed properly on bread board of the IC trainer kit.
- 2) Connections are made as per the designed circuit diagram.
- 3) Power supply to the board is turned ON.

Observation and conclusion:

Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purposes; they can count specific events happening in the circuit.

Asynchronous counter: we don't use a universal clock; only the first flip-flop is driven by the main clock and the clock input of the rest of the following flip-flops is driven by the output of the previous flip-flops.

MOD Counters are cascaded counter circuits which count to a set modulus value before resetting. The job of a counter is to count by advancing the contents of the counter by one count with each clock pulse.

Decade Counter means mod 10 counter so it counts from 0 to 9 and gets reset to 0.

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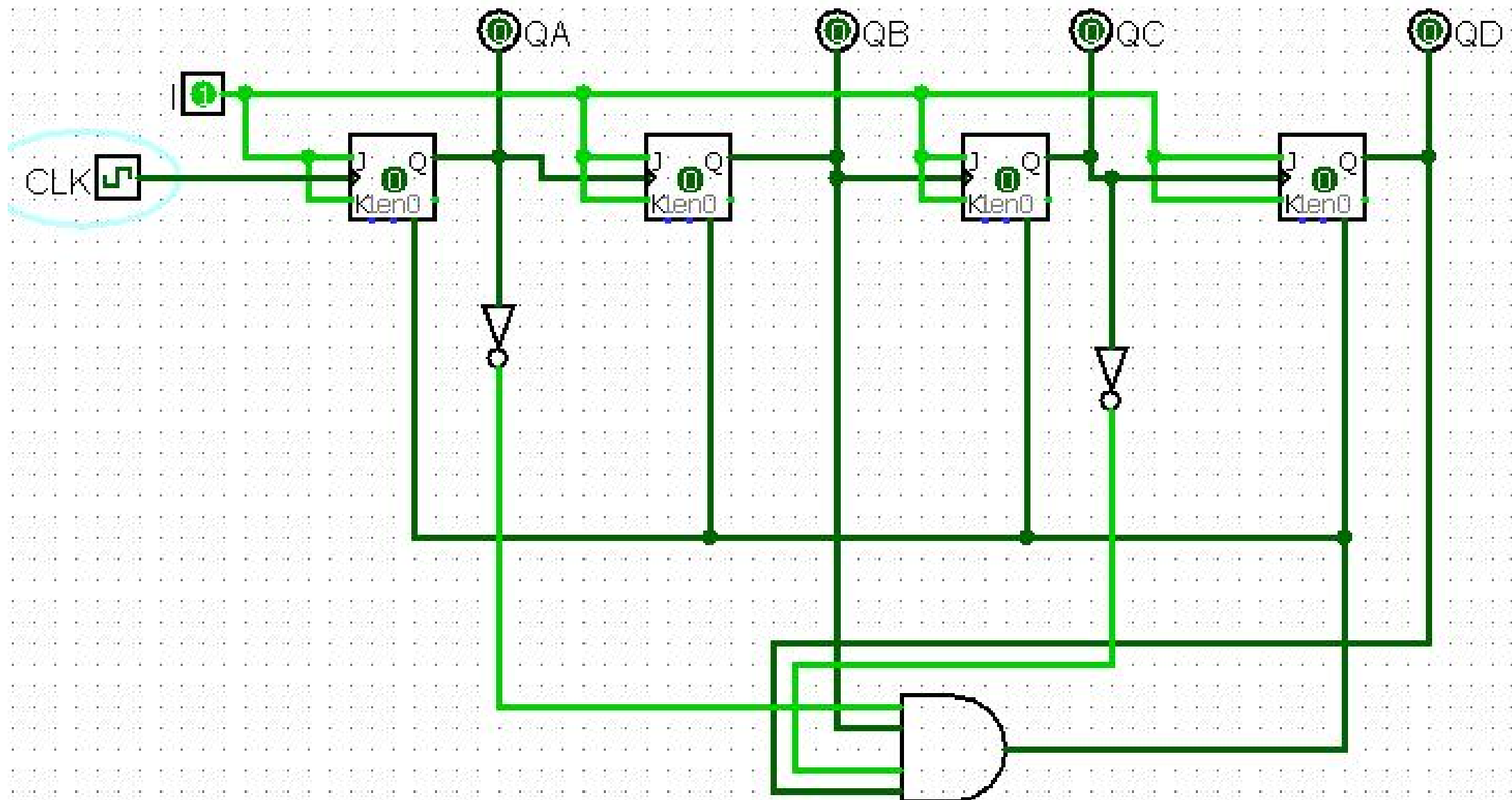
Date: 16/02/21

Sign:

Kaushik

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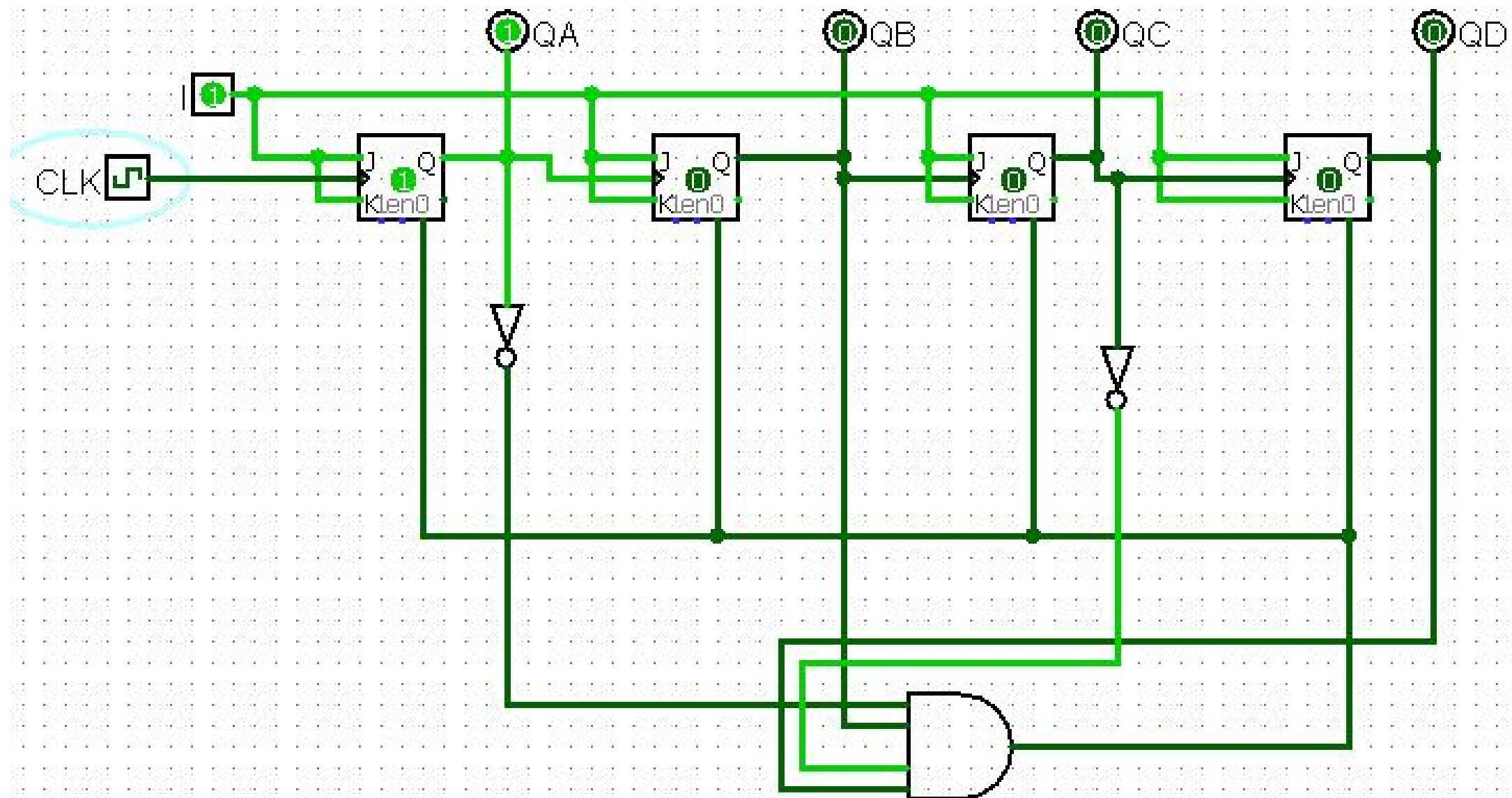
MOD 10 ASYNCHRONOUS COUNTER/ decade



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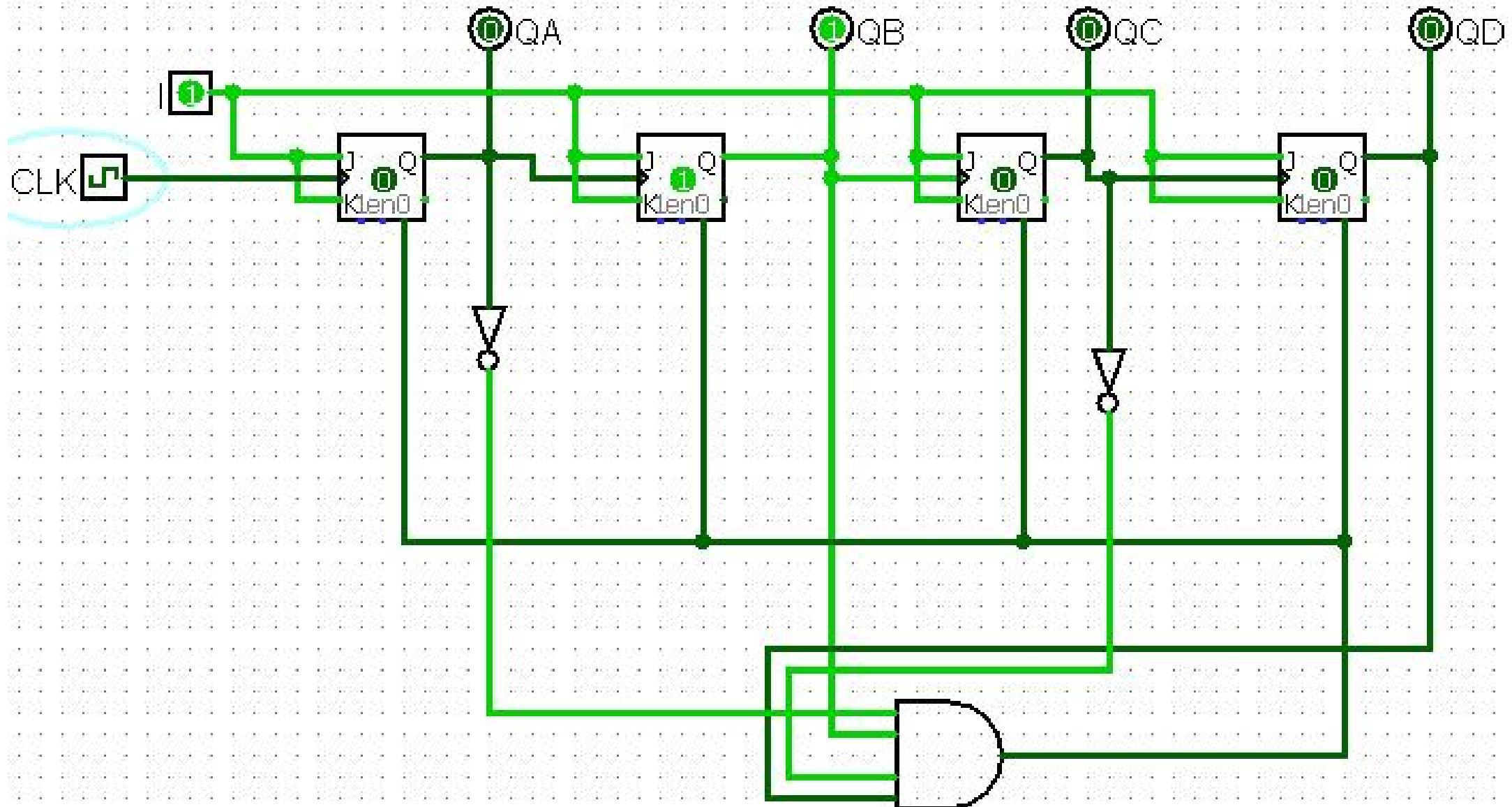
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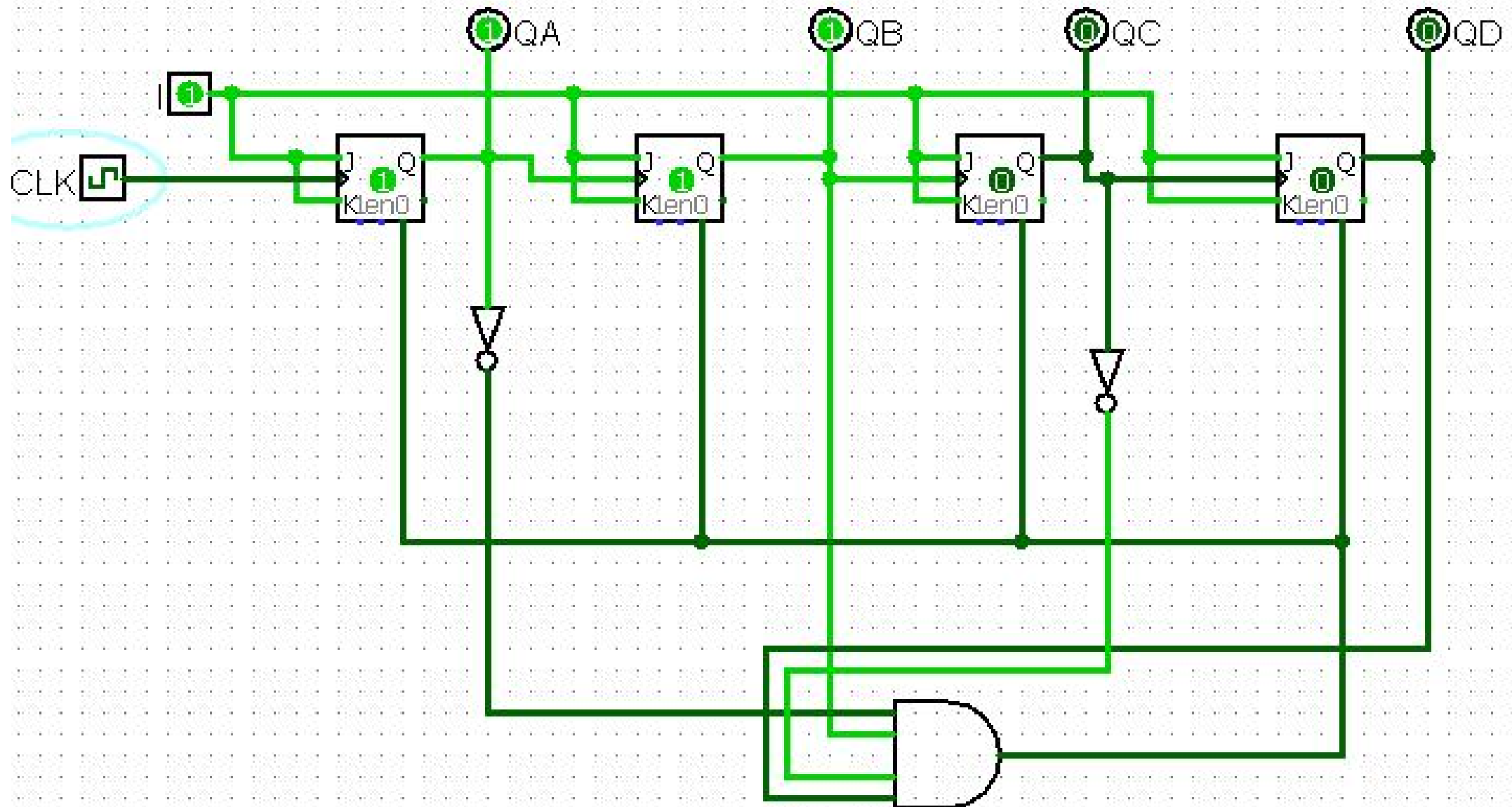
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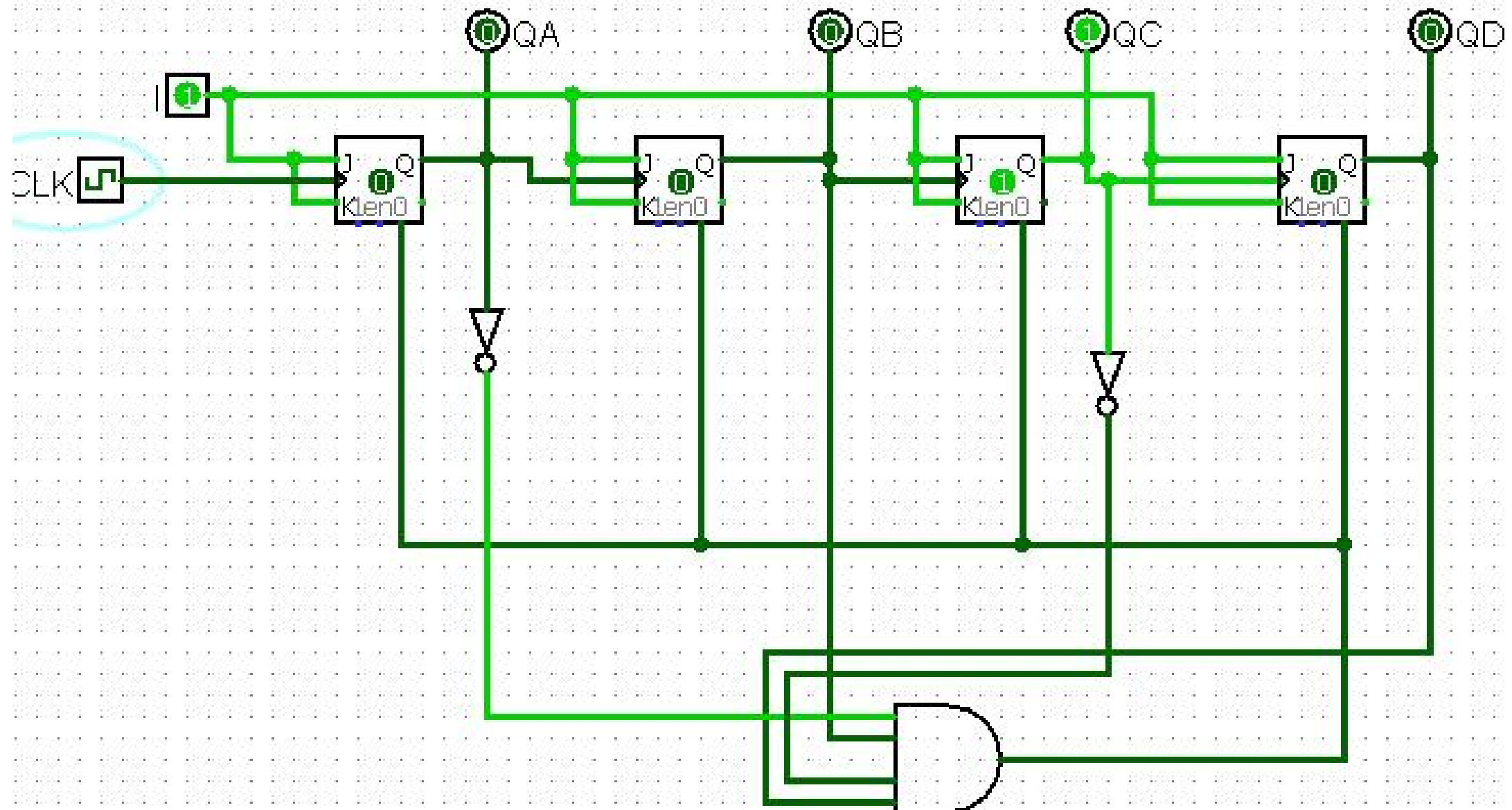
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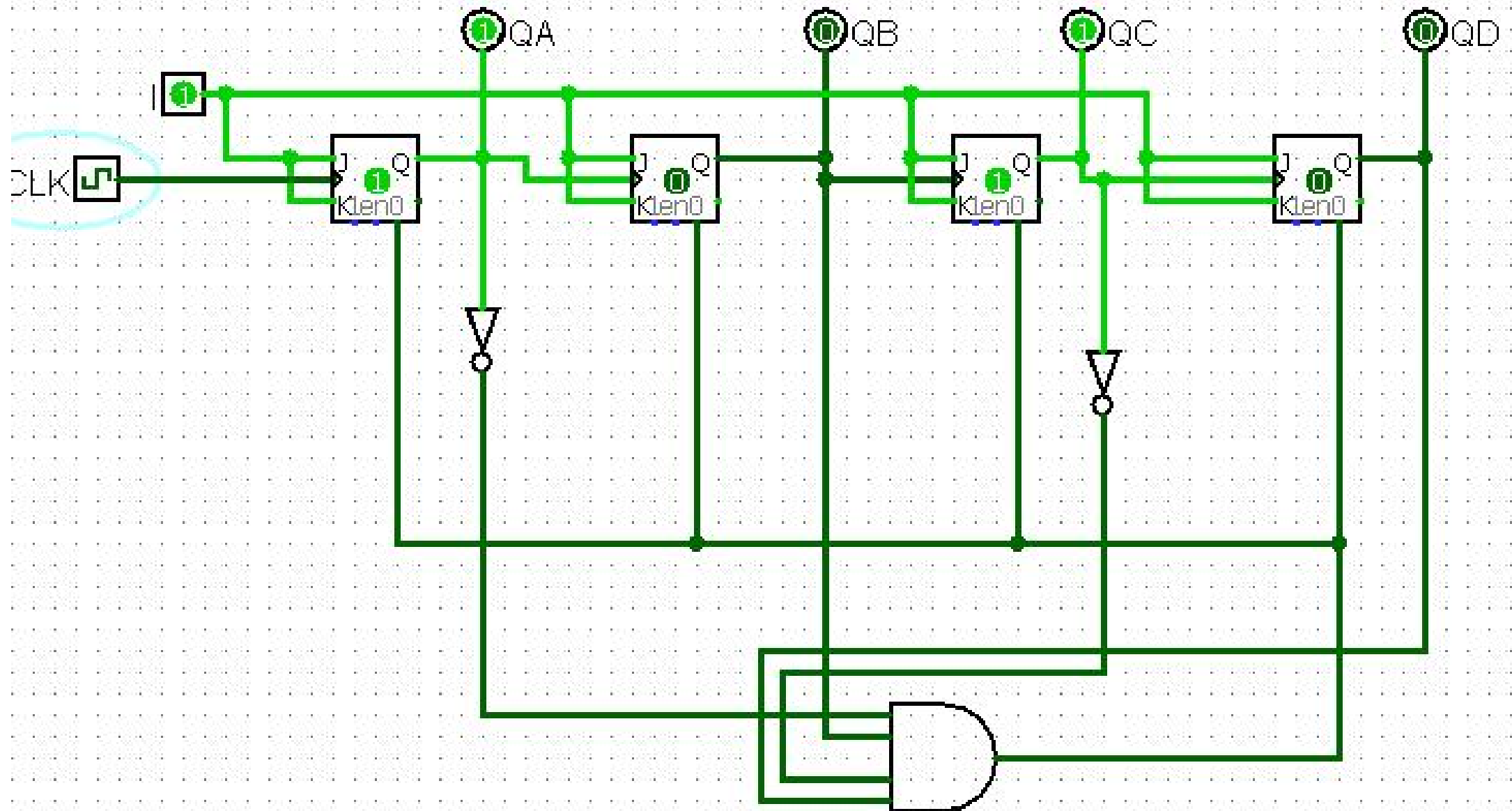
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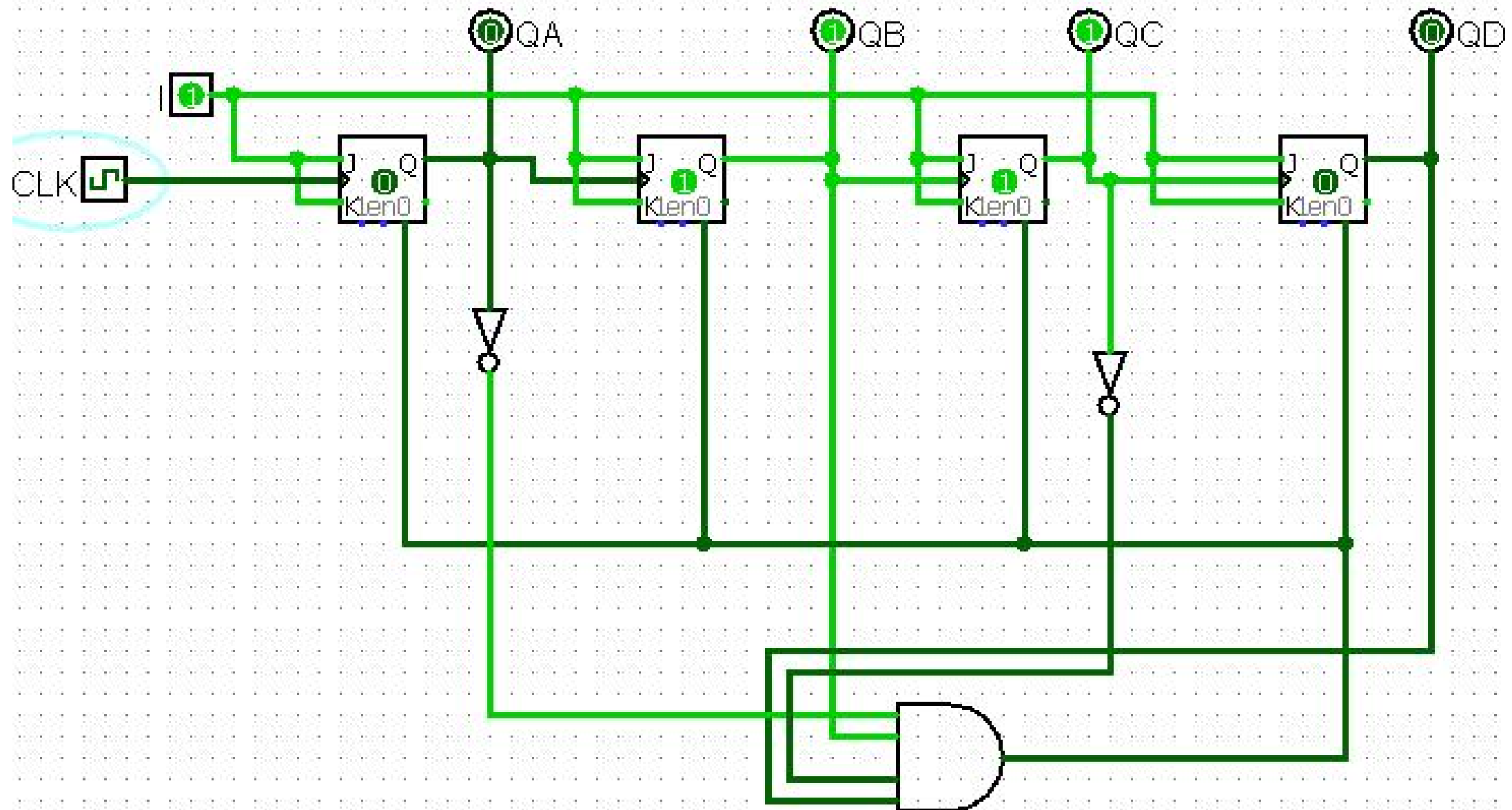
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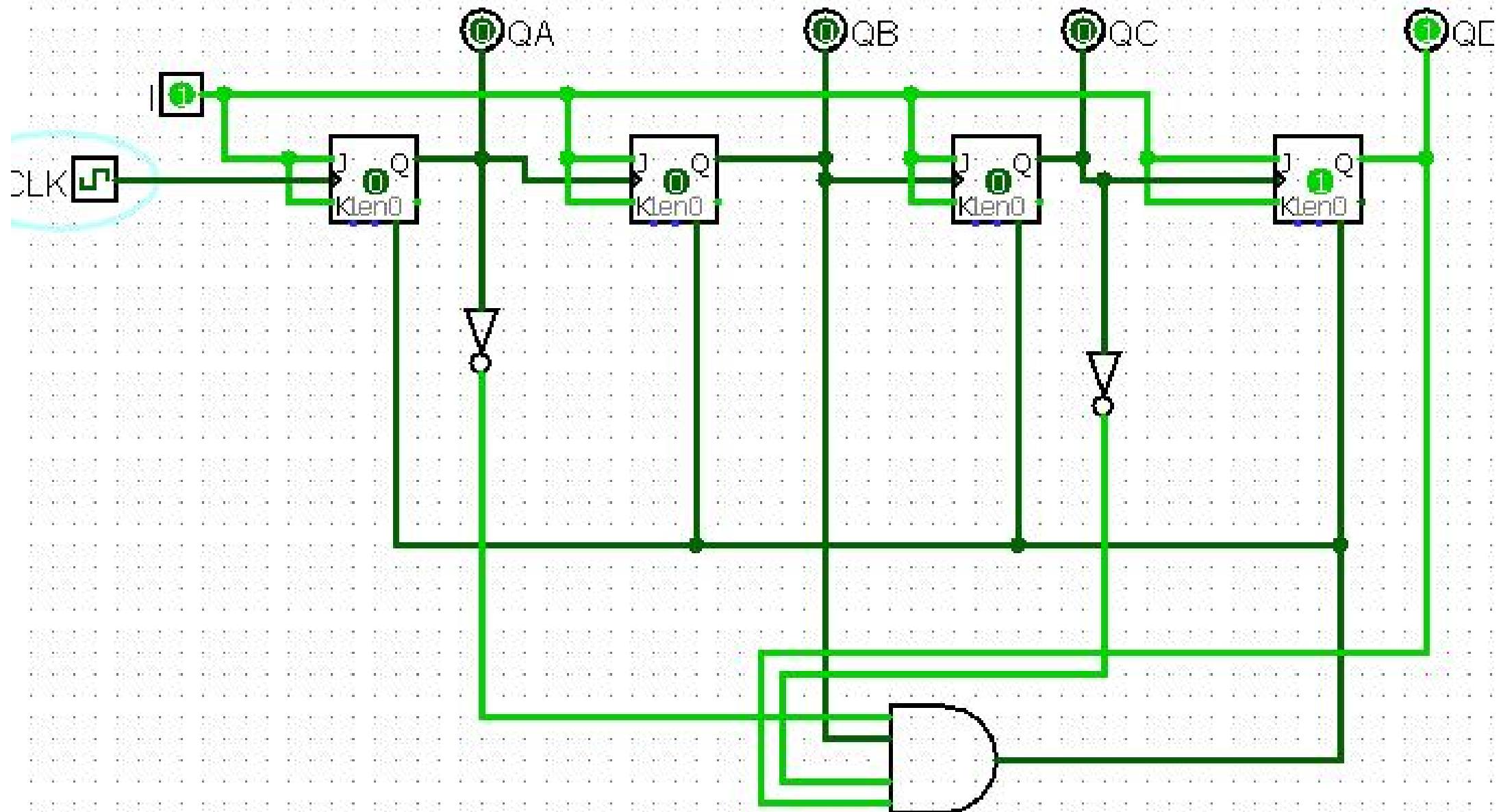
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The diagram shows a 4-bit shift register implemented with four J-K flip-flops. The clock signal (CLK) is connected to the clock input of all flip-flops. The output of the first flip-flop (QA) is connected to the input of the second flip-flop (QB). The output of the second flip-flop (QB) is connected to the input of the third flip-flop (QC). The output of the third flip-flop (QC) is connected to the input of the fourth flip-flop (QD). The output of the fourth flip-flop (QD) is connected to the input of the first flip-flop (QA) through a 4-input AND gate. The output of the AND gate is connected to the input of the first flip-flop (QA). The output of the first flip-flop (QA) is also connected to the input of the AND gate. The output of the second flip-flop (QB) is connected to the input of the AND gate. The output of the third flip-flop (QC) is connected to the input of the AND gate. The output of the fourth flip-flop (QD) is connected to the input of the AND gate. The output of the AND gate is connected to the input of the first flip-flop (QA).

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