Experiment no: 7

Experiment name: Construction & Varification of flip-flop:

Aim: Construct: (i) S R flipflop
(ii) D flip flop
(iii) J K flipflop
(iv) T flip flop

Apparatus Required:

		Quantity:		
1. Nor gate	– IC 7402	– 1	6. Nand gate	– 1
2. Not gate	– IC7404	– 1		
3. And gate	– IC7408	– 1		

4 Connecting wire
5. Clock.

Theory:

Flipflop is a basic storage element used to store 1 bit of data. Flipflop & latches are fundamental building block of any Sequential circuit.

Flipflop are used in counters, registers & Sequence generators.

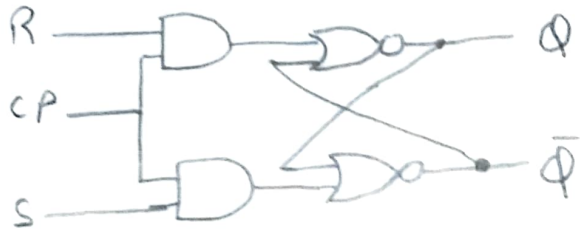
Their are four types of flip flops.

i S-R flip flop
ii D - flip Flop
iii J K - flip flop
iv T - flip flop.

They are edge-sensitive or -ve edge trigg ered.
For rest Part of clock pulse, the flipflop remains insensitive

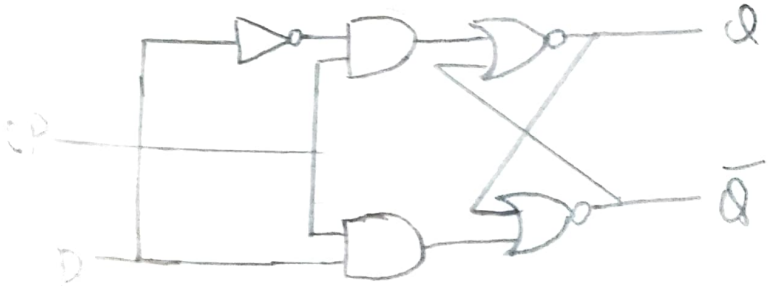
(i) SR flip flop:

Input			Output
Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate



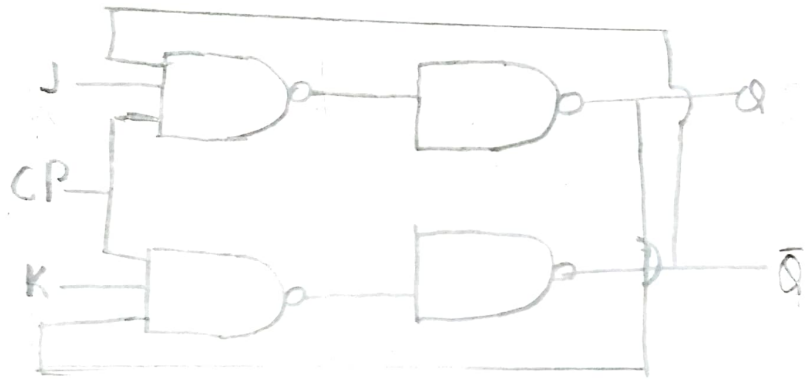
(ii) D flip flop:

Input		Output
Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1



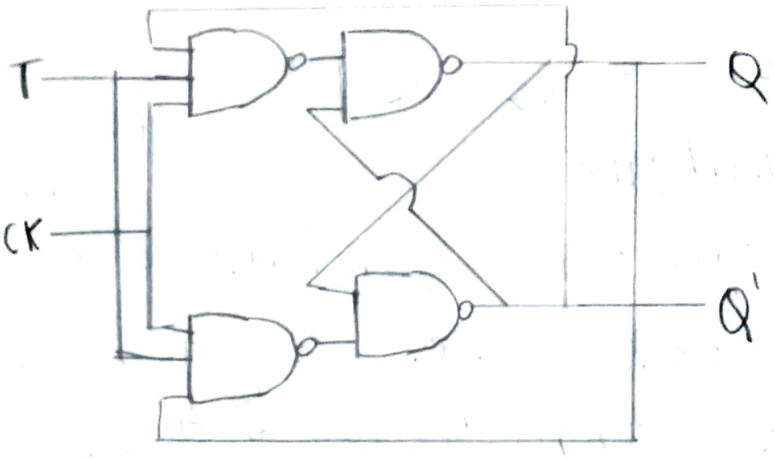
(iii) JK flip flop:

Input			Output
Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



(iv) T flip flop:

Input		Output
Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0



Practical Procedure:

1. IC's are placed properly on the bread board of IC kit
2. Connections are made as per the designed circuit diagram.
3. Power supply to the bread board is turned on.
4. Circuit is varified as per the characteristic table of circuit.

Observations & conclutions:

S-R-flip flop:

1) It consists of 2 and gate & 2 nor gate.
2) S - Set & R - Reset These are active only if clock is active
3) in case of S=R=1 The output is of $Q = \bar{Q} = 0$ since This is wrong & Q is not compliment of $\bar{Q}$ that case is called indeterminate state.

D-flip flop:

1) It consists of or gate, & 2 and gates & 2 nor gate,
2) It is a modified version of S-R flip flop &
3) its called data flipflop, its one of the most commonly used flip flop to store data.
4) it has has only one input (D) & its negation is used to given an input.

5) In this we are avoiding the state $S=R=1$,

J-K flip flop:

1) It consists of 4 nand gates.
2) it overcomes situation of $J=K=1$, but toggling occures
3) its only active if clock is active.
4) except for $J=K=1$ The rest behaviour of This flipflop is same as S-R flip flop.

T flipflop:

1) it consists of 4 nandgates,
2) But it has only 1 ϕ input, T, This flipflop is called toggle flip flop.
3) its used if we only want toggling effect in our output
4) Its a modification of JK flipflop, its active only if clock is active.

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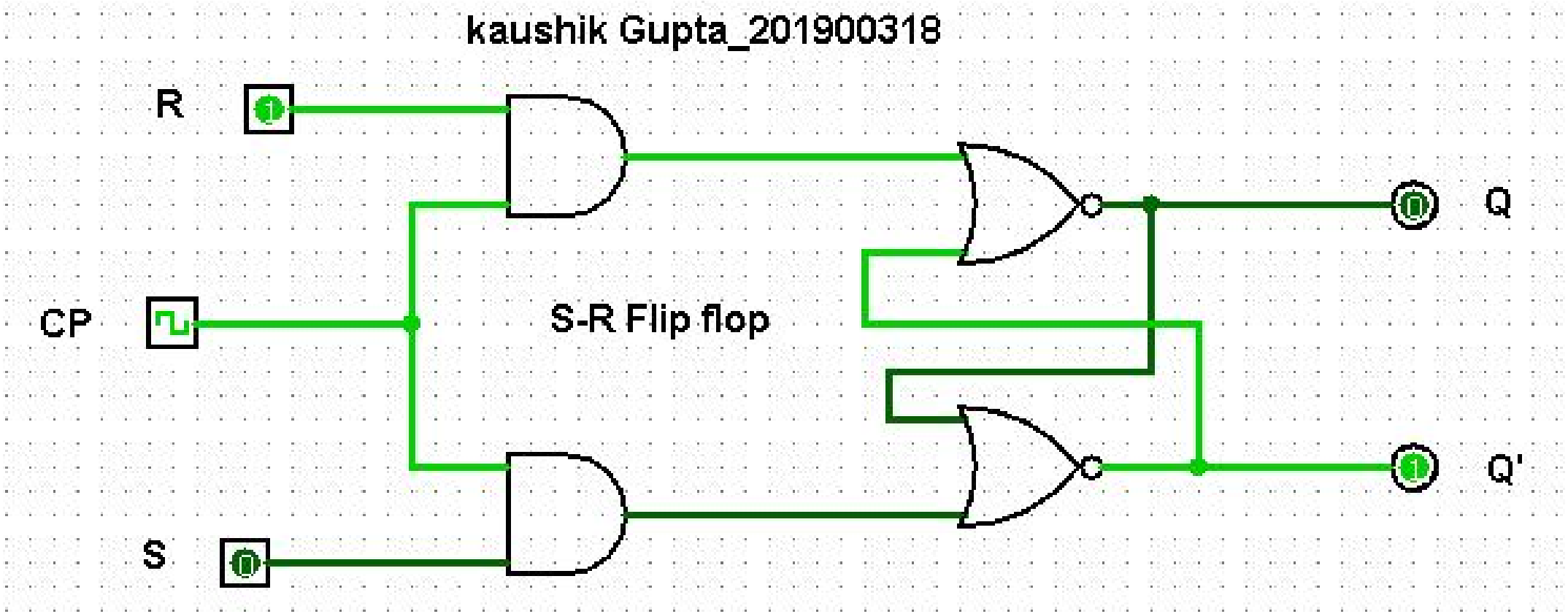

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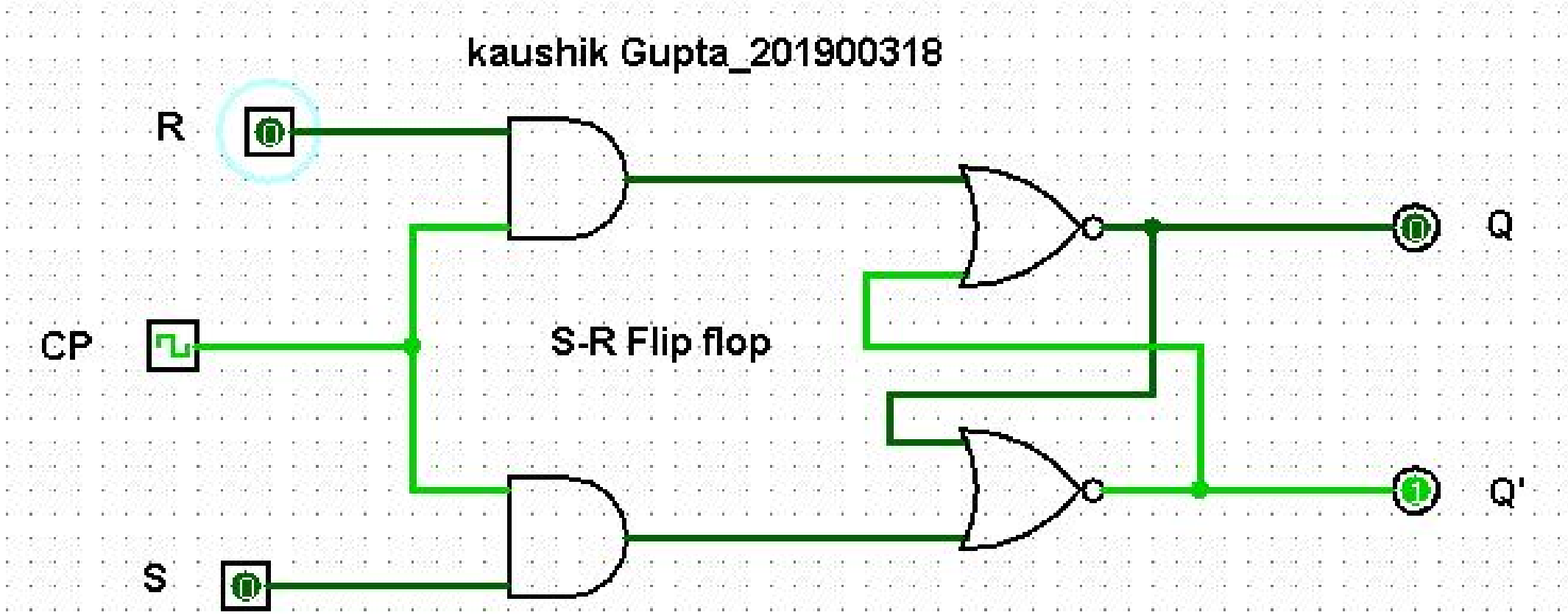

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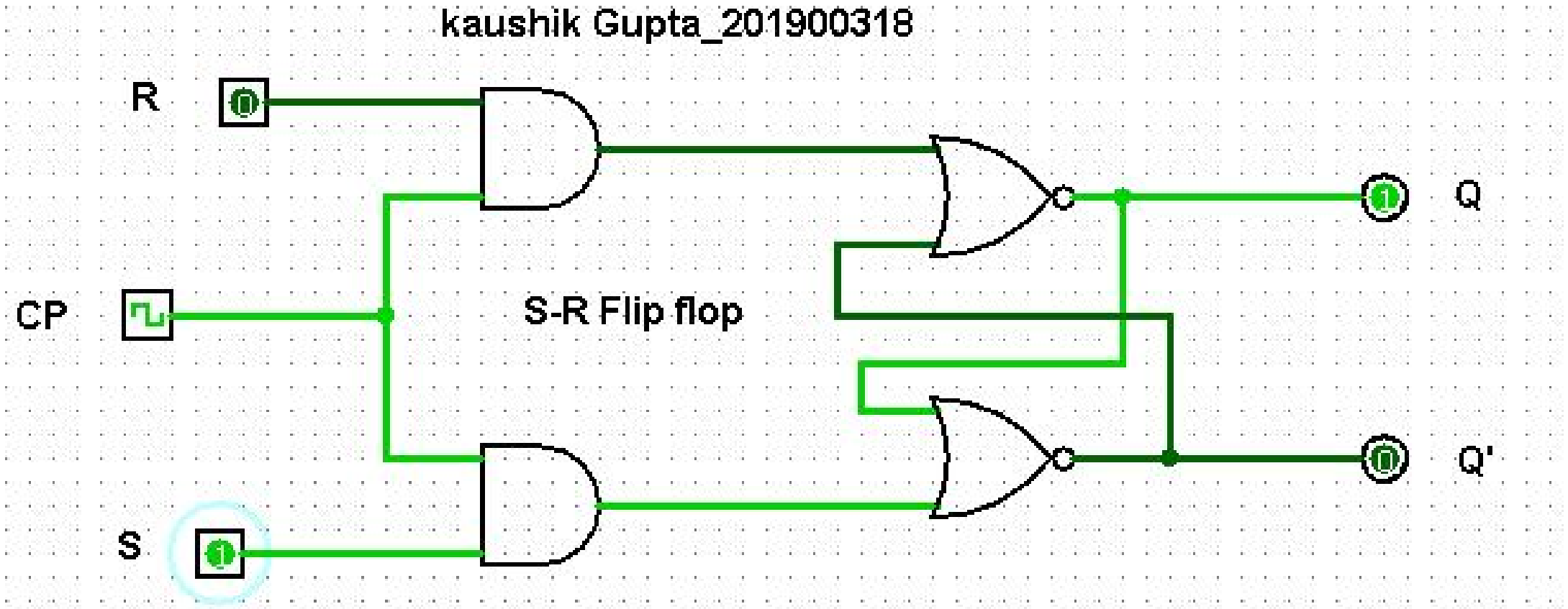

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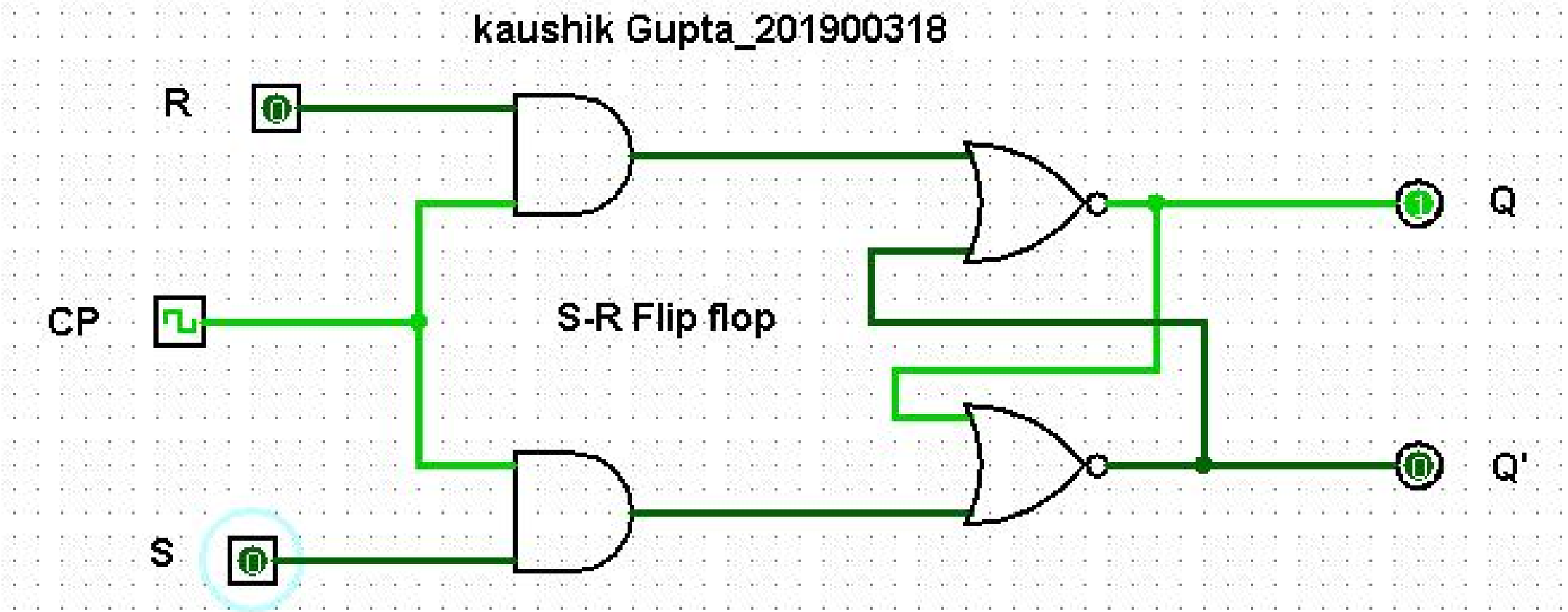

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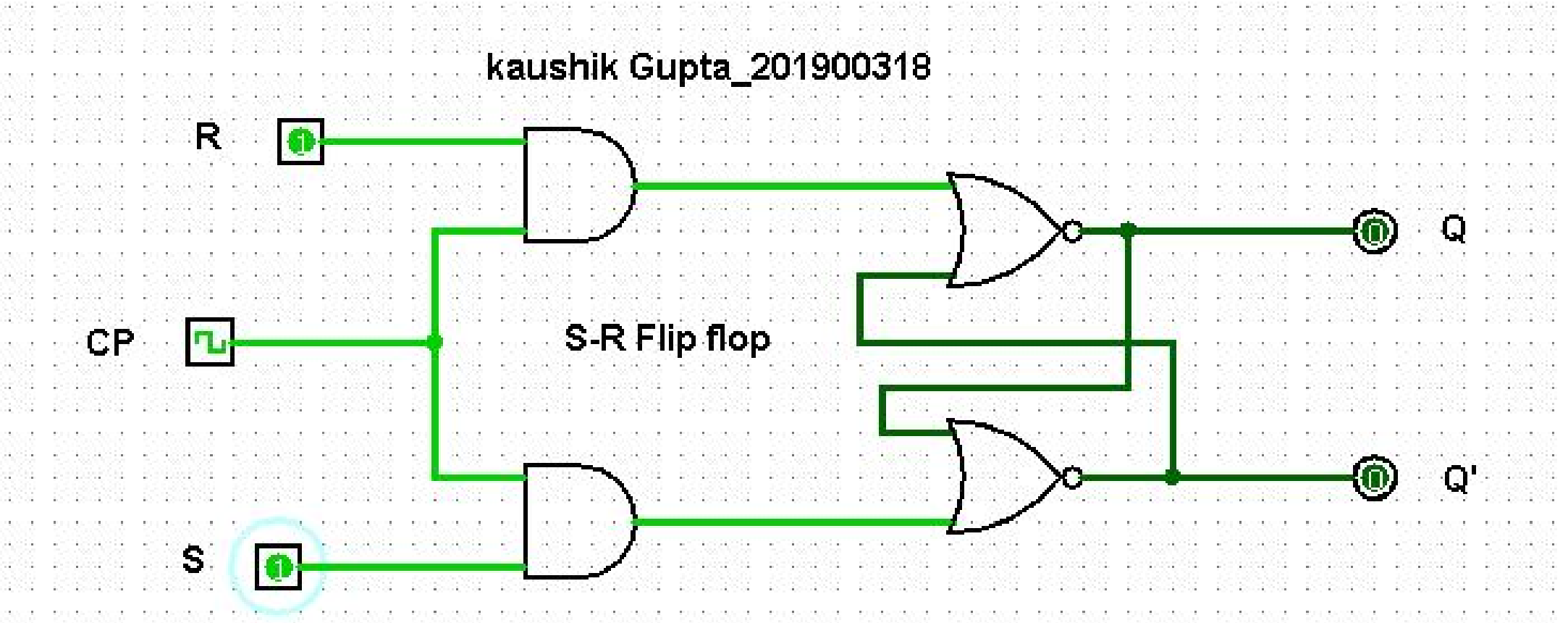

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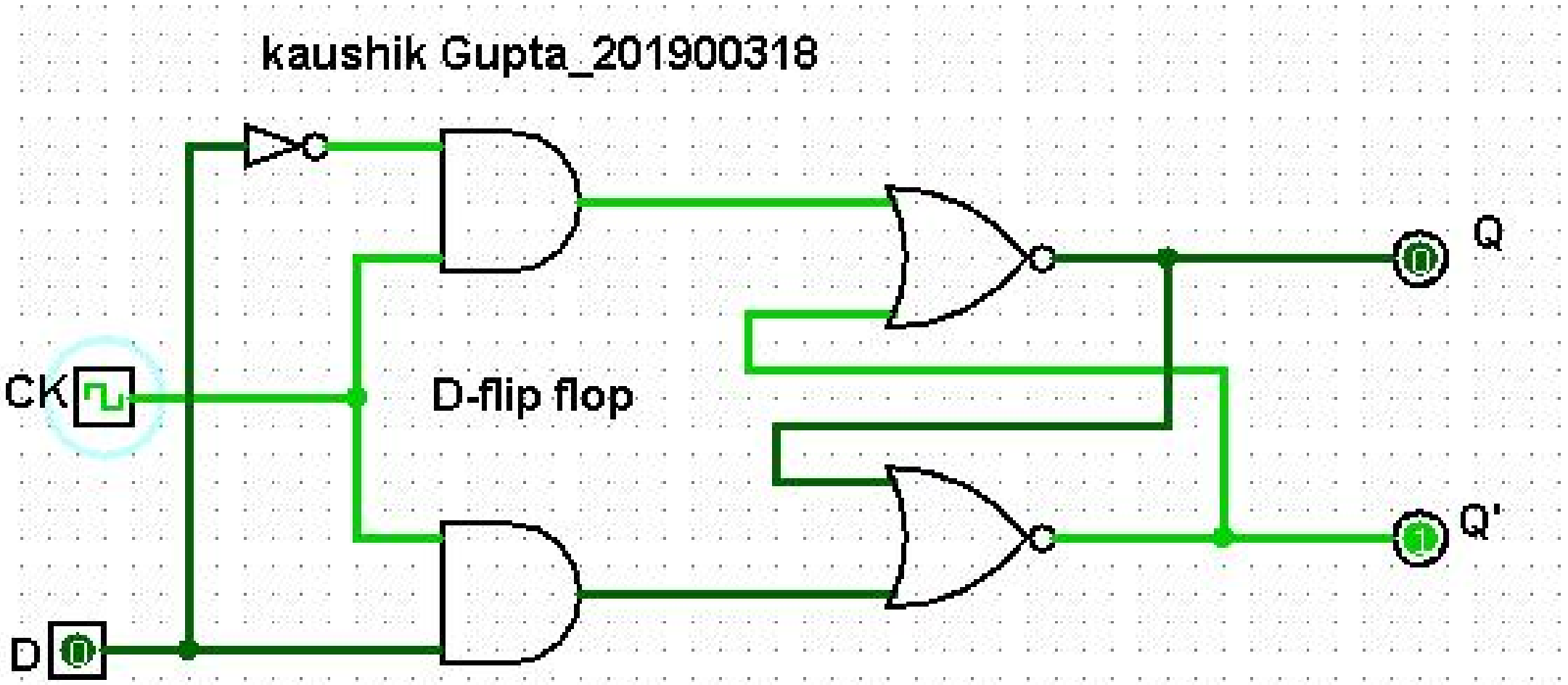

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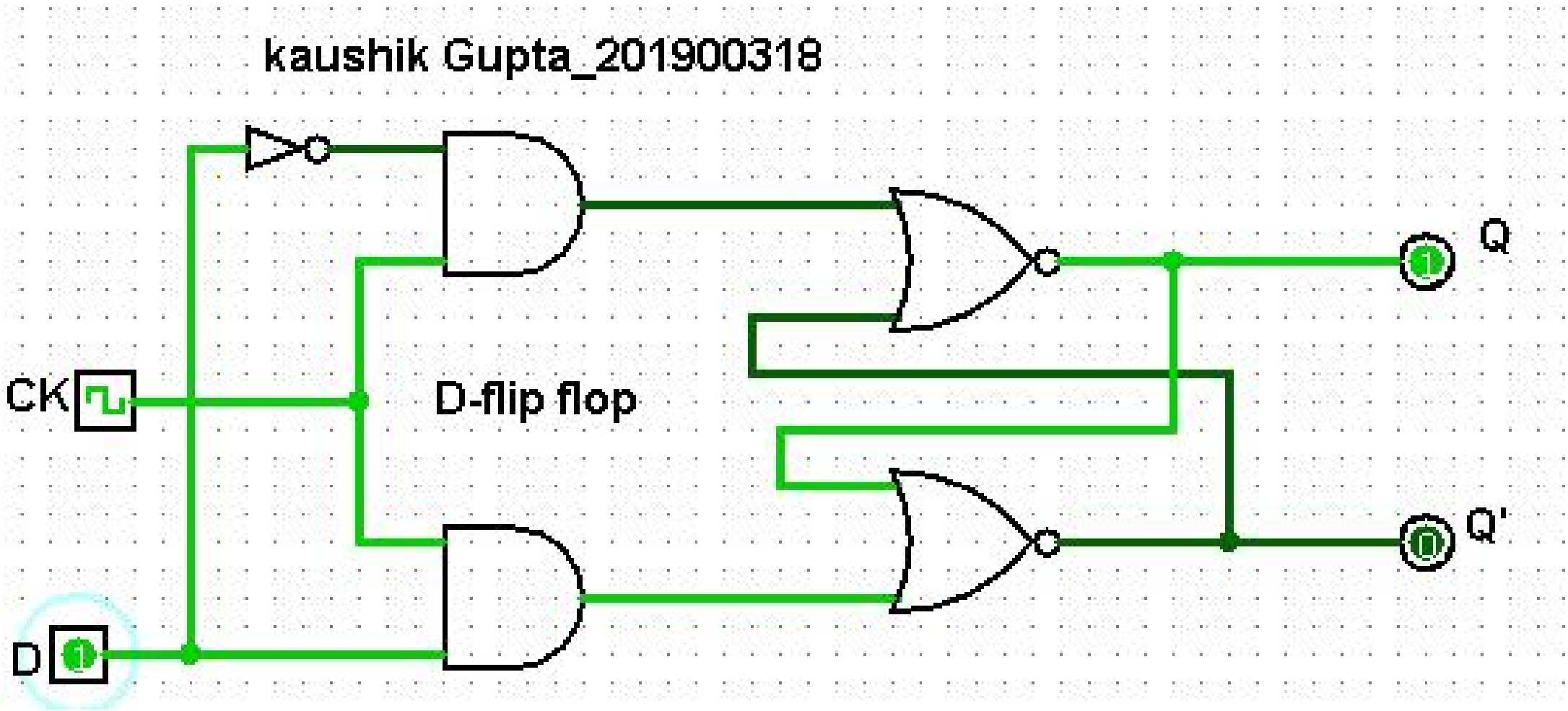

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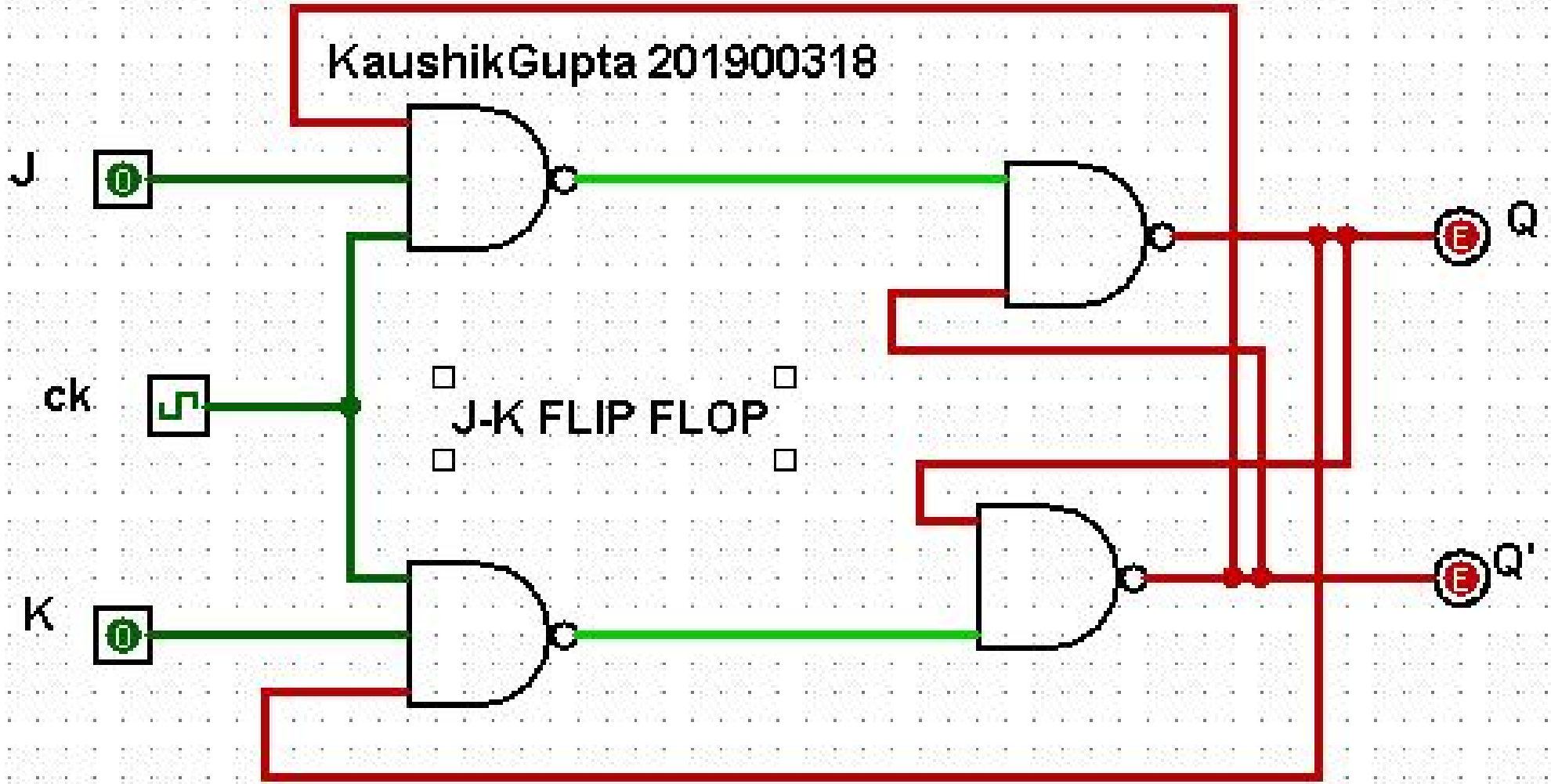

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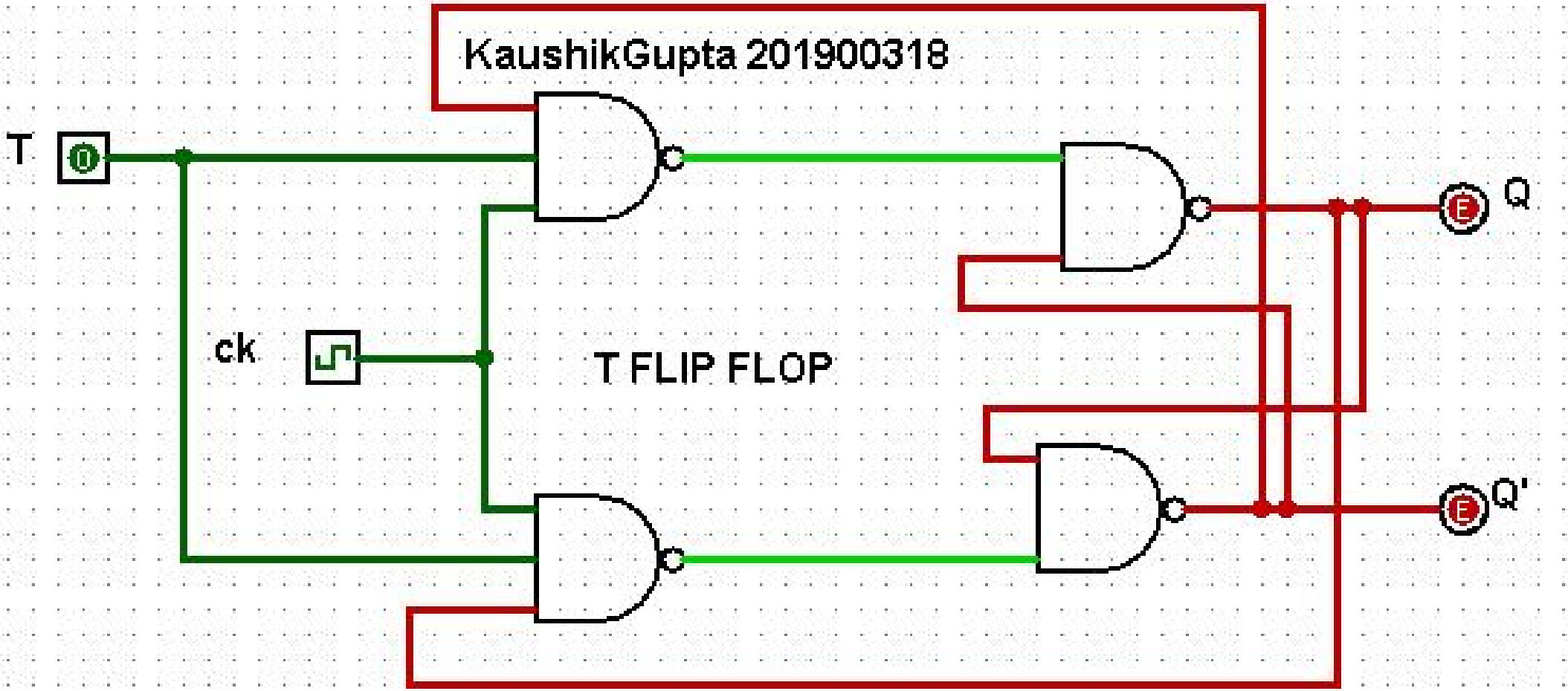

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