Date:

Experiment Number: 6

Experiment name: Design of a mod 16 - Synchronous up counter using J-K ~~ff~~ flip flops.

Aparatus used:

1. AND gate - IC 7408
2. JK-ff - IC7473/7476
3. connecting wires
4. Power supply.

Theory:

Synchronous up counter (4bit) counts from 0000 to 1111 after that it resets. Its operating range is much higher than asychronous counter, this type counter has common clock to operate all the flip flops.

Present State				Next state				Excitation table of JK flip-flop							
Q_A	Q_B	Q_C	Q_D	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x
0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1
0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x
0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1
0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	x
0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1
0	1	1	0	0	1	1	1	0	x	x	0	x	0	x	x
0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1
1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x
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1	1	0	1	1	1	1	0	x	0	x	0	1	x	x	1
1	1	1	0	1	1	1	1	x	0	x	0	x	0	x	x
1	1	1	1	0	0	0	0	x	1	x	1	x	1	x	1

K-map for J_A:

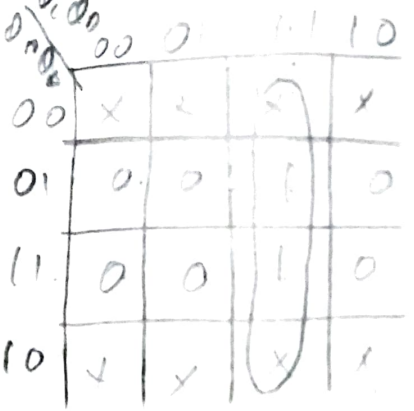
$J_A = Q_C Q_D Q_B$

$J_B = Q_C Q_D Q_B$

K-map For J_B:

$J_B = Q_C Q_D$

K-map For K_B:



$K_B = Q_C Q_D$

K-map for J_C:

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	1	x	x
01	0	1	x	x
11	0	1	x	x
10	0	1	x	x

$J_C = D$

K-map for K_C:

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	1	1	x
01	0	x	x	x
11	0	1	1	x
10	0	1	x	x

$K_C = D$

Kmap for J_D:

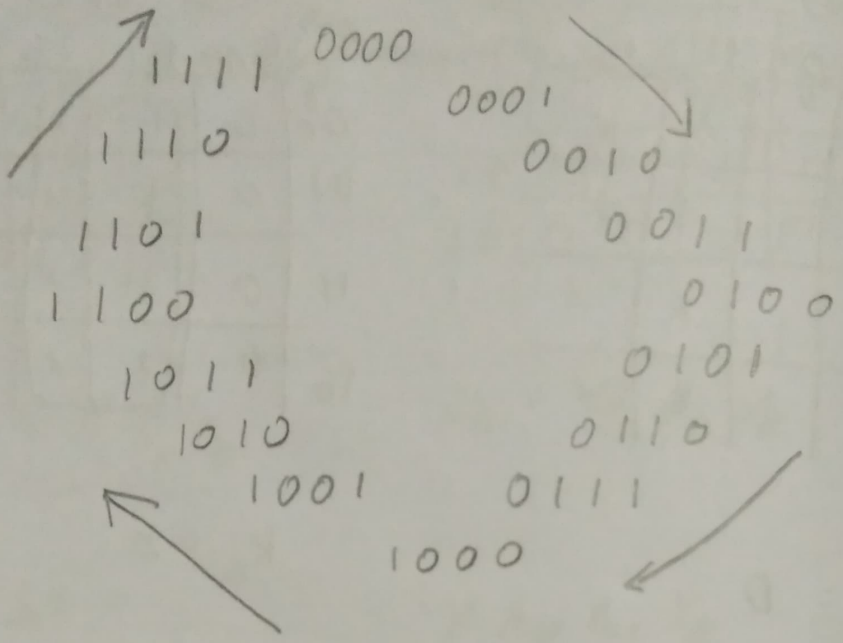
$Q_C Q_D$ \ $Q_A Q_B$	00	01	11	10
00	1	x	x	1
01	1	x	x	1
11	1	x	x	1
10	1	x	x	1

$J_D = K_D = 1$

K-map for K_D:

$Q_C Q_D$ \ $Q_A Q_B$	00	01	11	10
00	x	1	1	x
01	x	1	1	x
11	x	1	1	x
10	x	1	1	x

State diagram:



Design & Practical procedure:

1. Truth table of 4bit binary to gray code converter is prepared.
2. K-map for all the output var (A, B, C, D) are drawn.
3. Circuit diagram is drawn as per simplified expression of output variable obtained.
4. ICs are placed on the bread board of IC trainer kit.
5. Connections are made properly & Power is turned on.

Observations:-

• Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counter are used in digital electronics for counting purpose, they can count specific event happening in the circuit.

• The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

• Synchronous Counters are so called because the clock input of all the individual flip-flops within the counter are all clocked together at the same time by the same clock signal.

• MOD Counters are cascaded counter circuits which count to a set modulus value before resetting. The job of a counter is to count by advancing the contents of the counter by one count with each clock pulse.

• In this experiment we have use four JK flip flop for the mod counter.

Name: kaushik gupta
Regno:201900318
sign:kaushik
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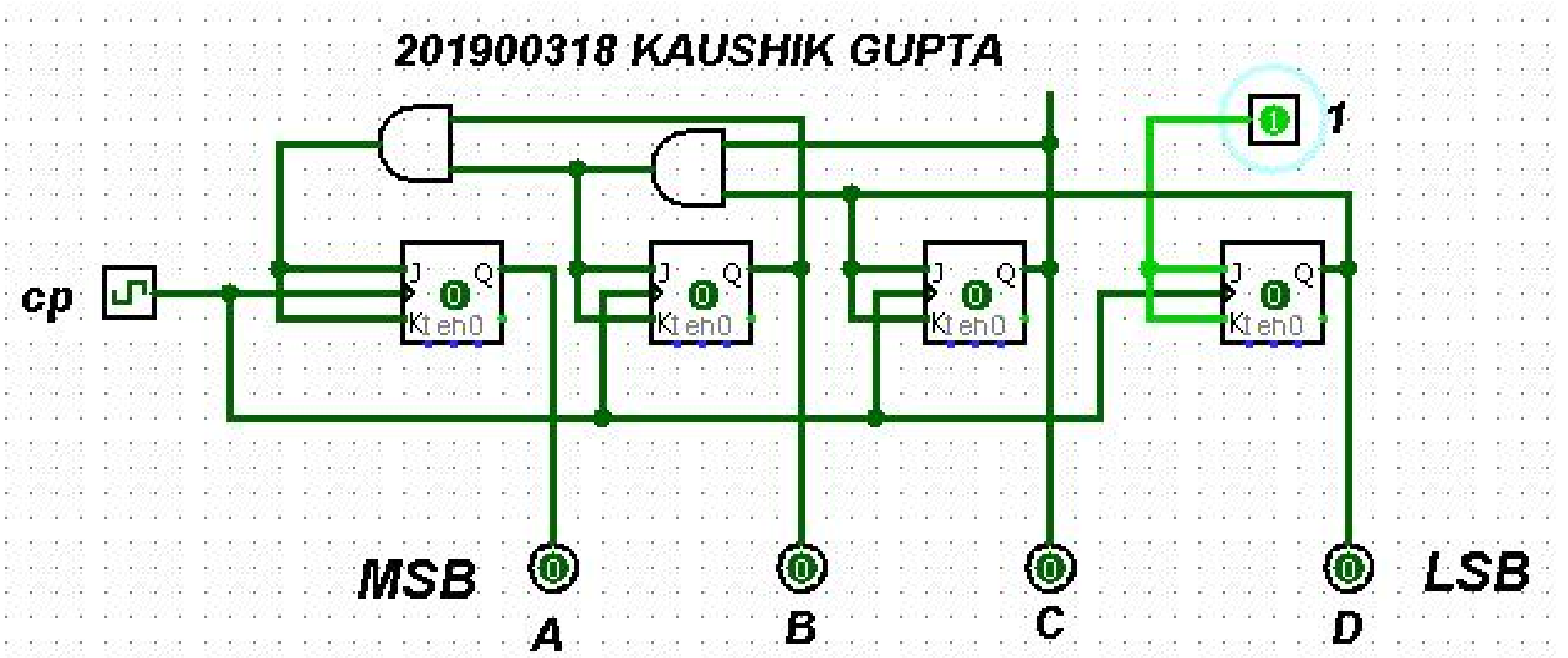
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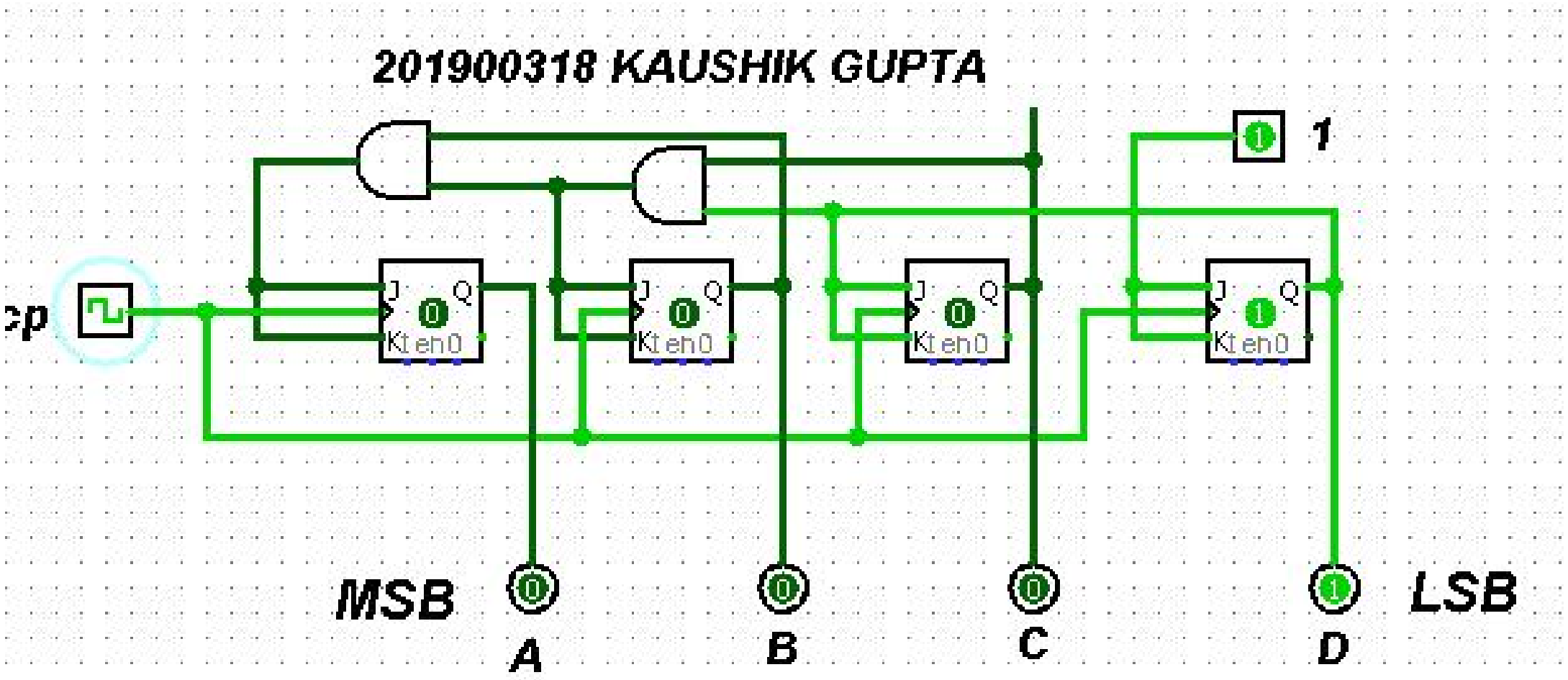
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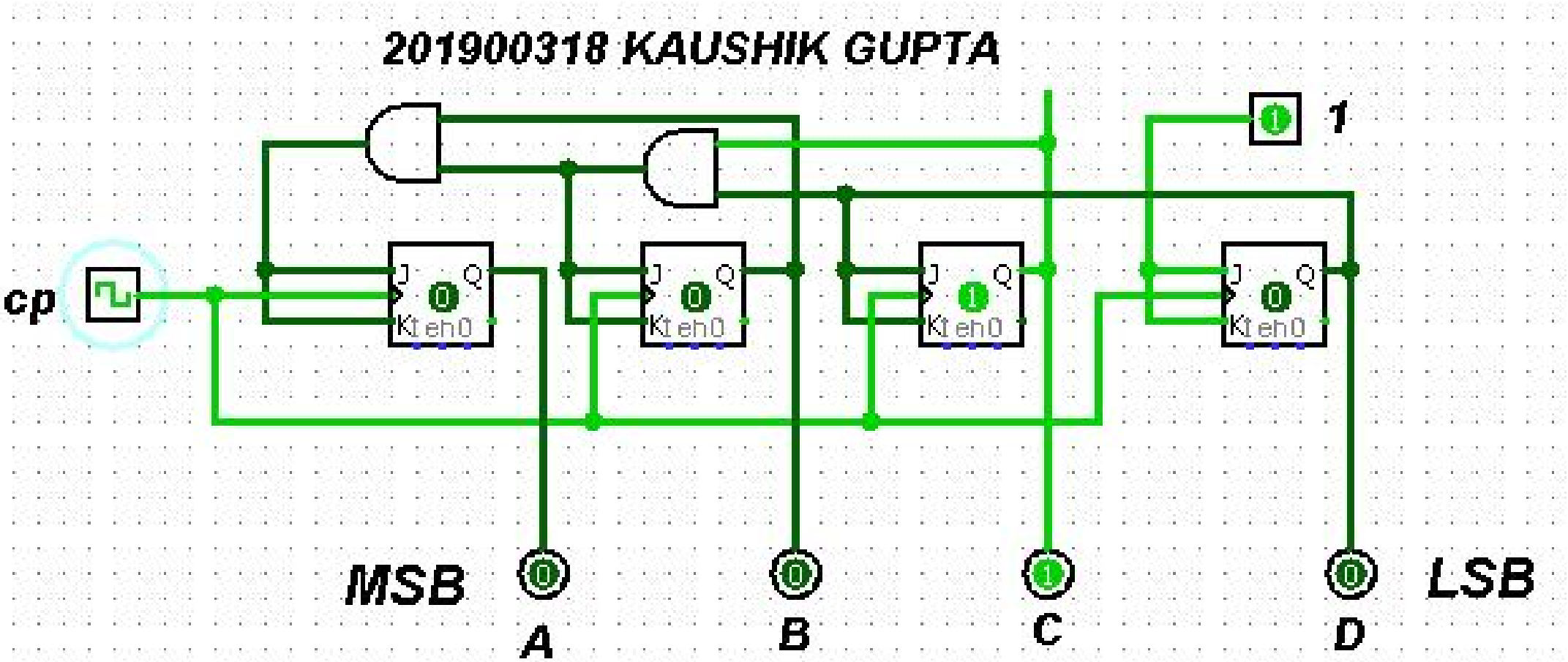
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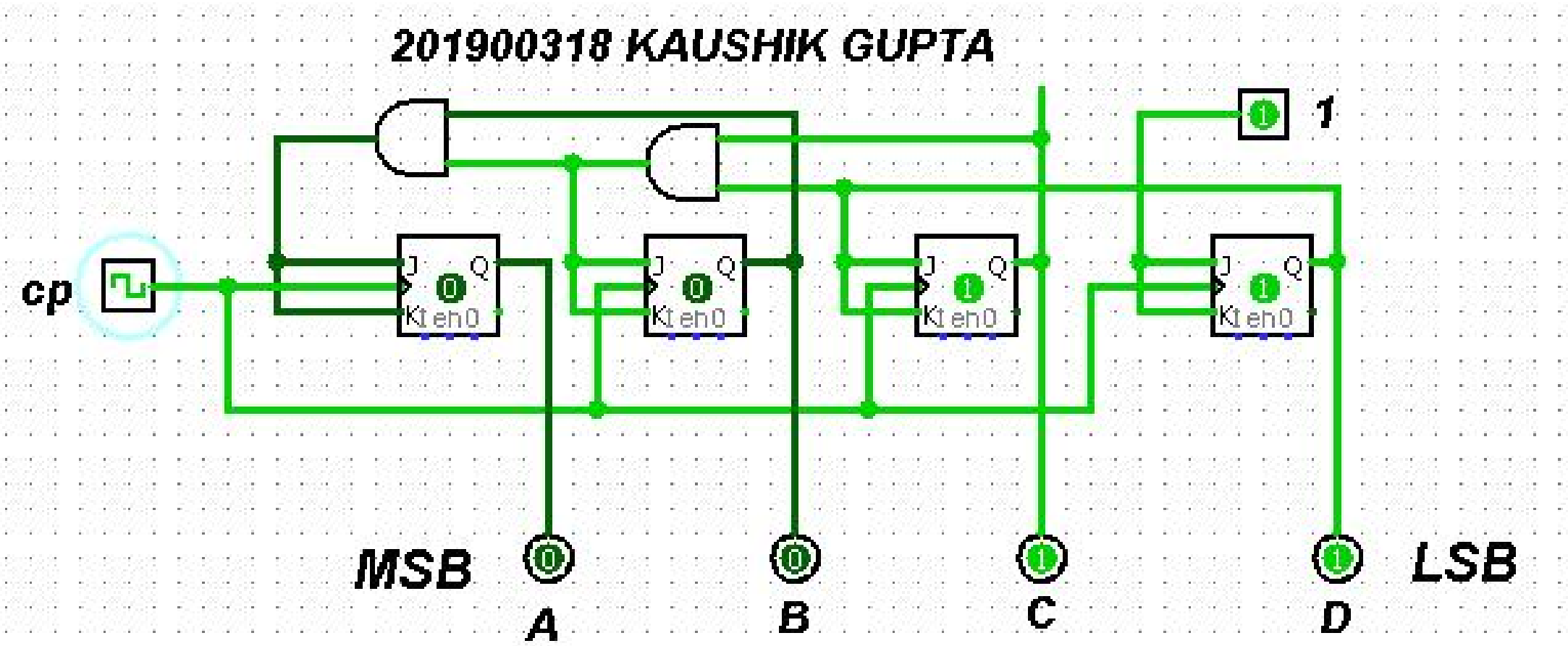
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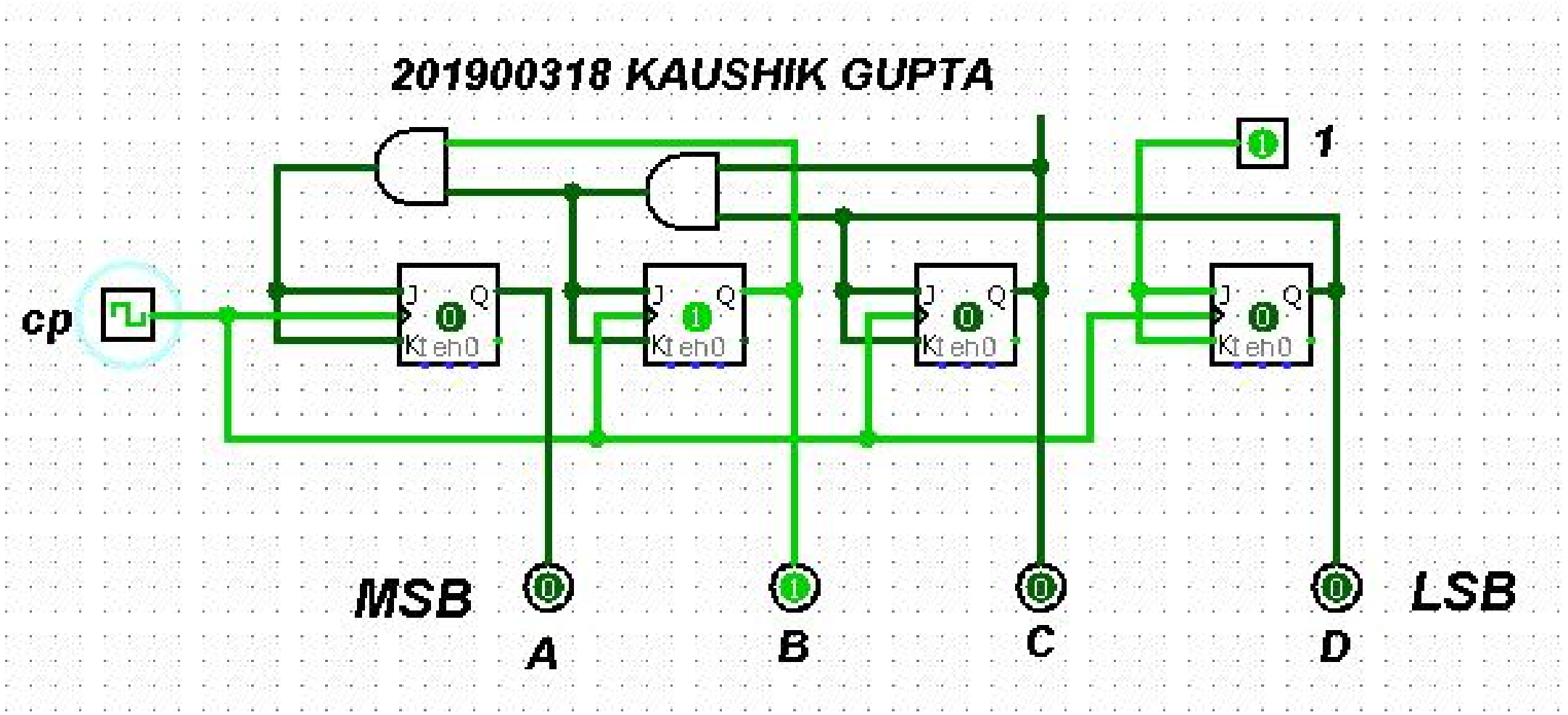
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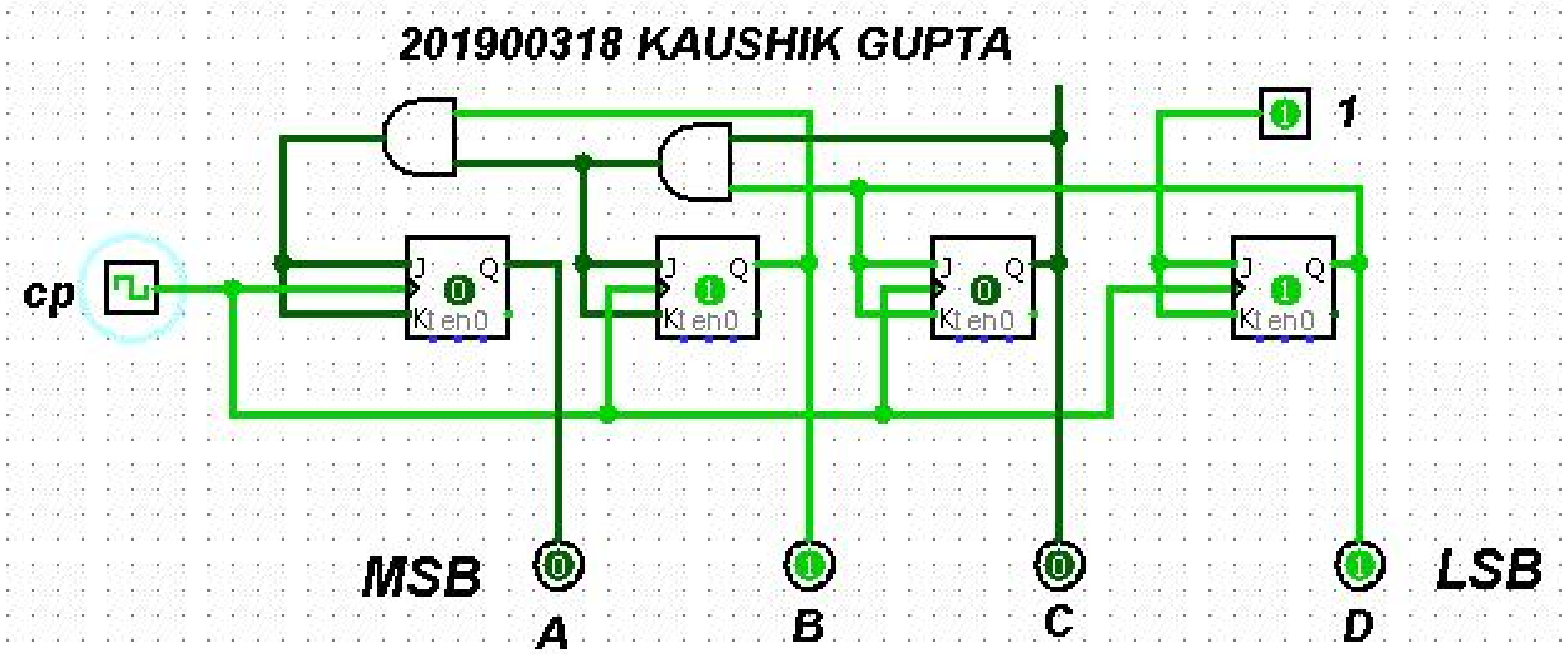
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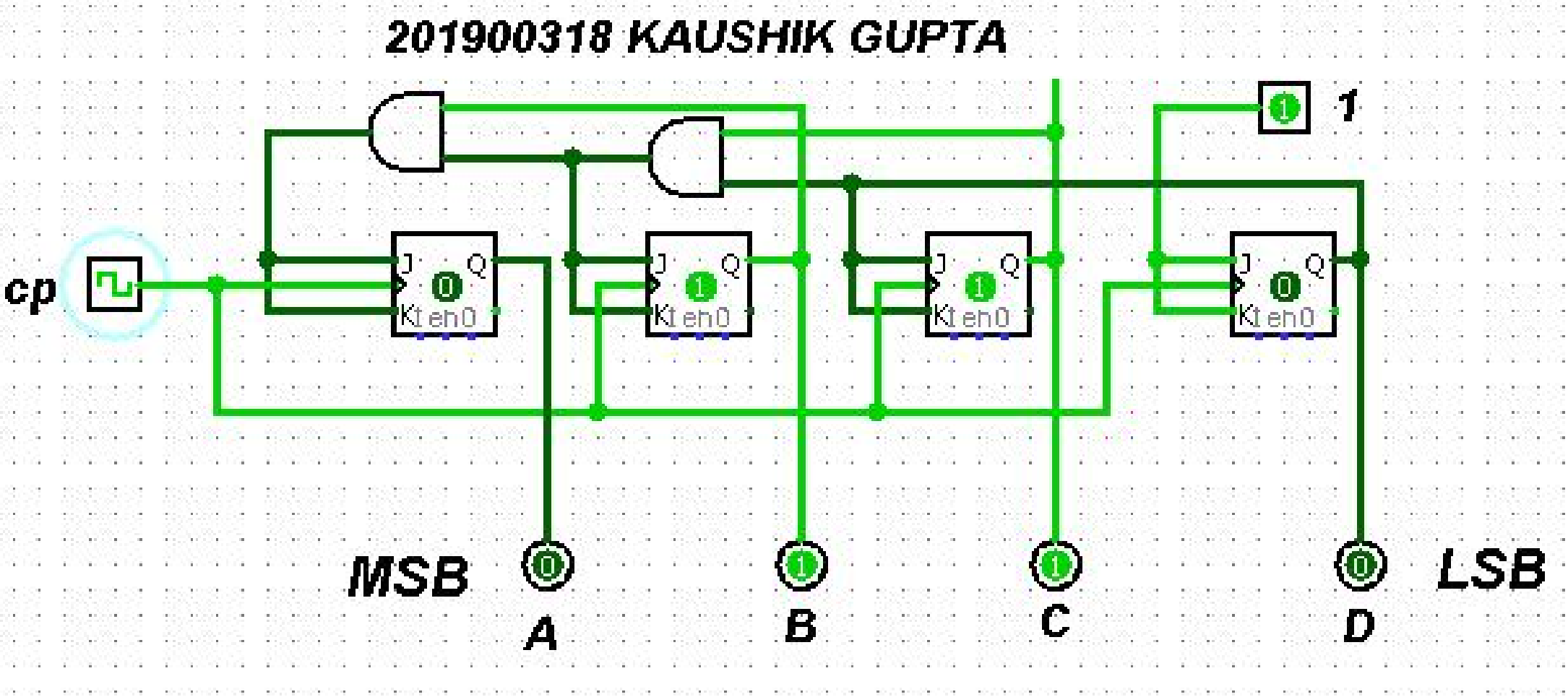
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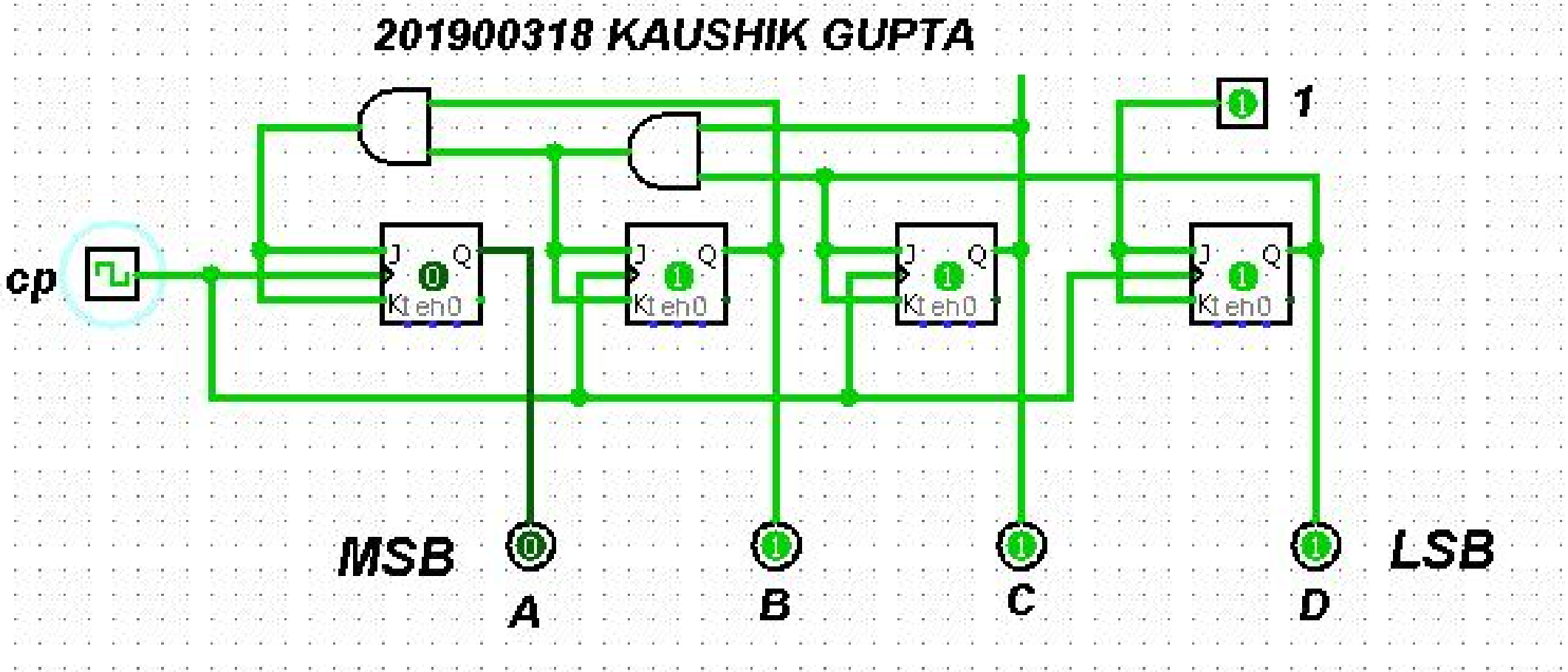
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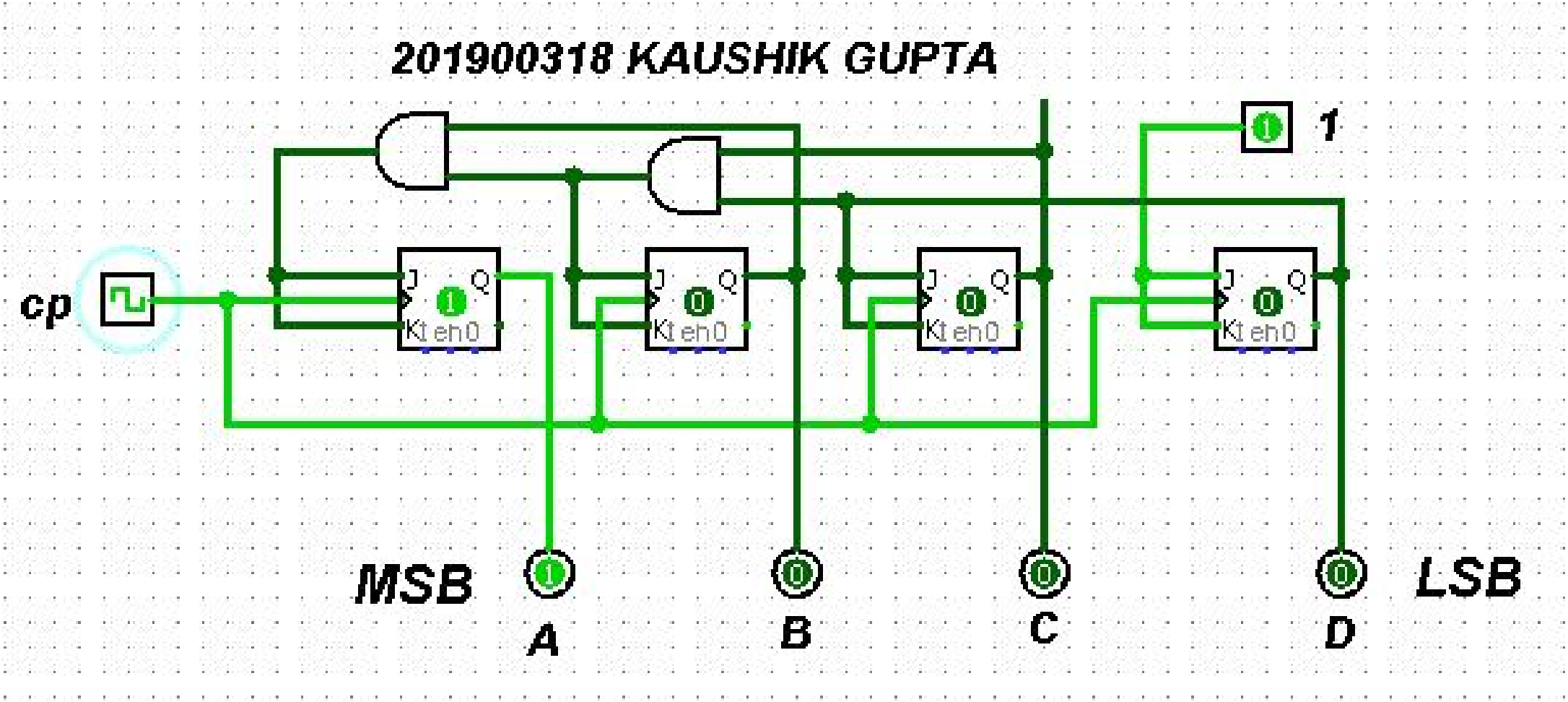
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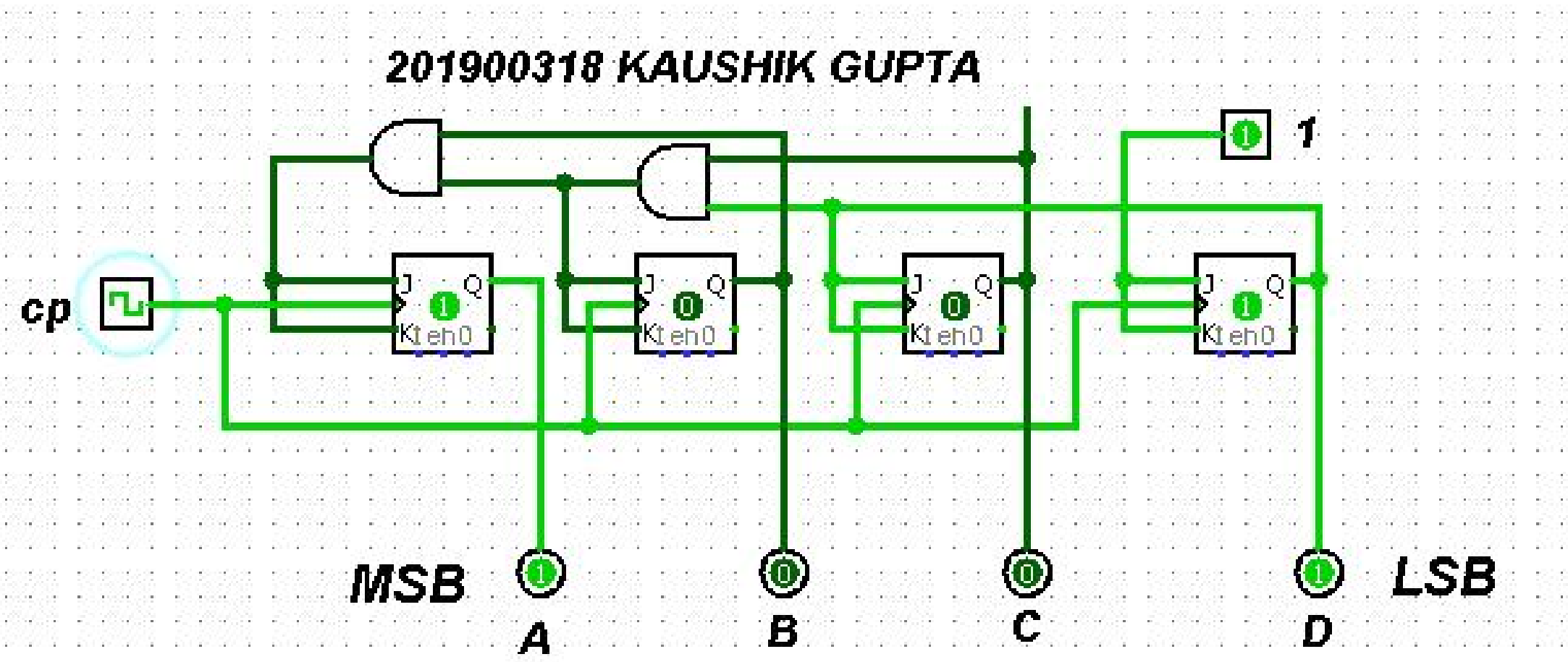
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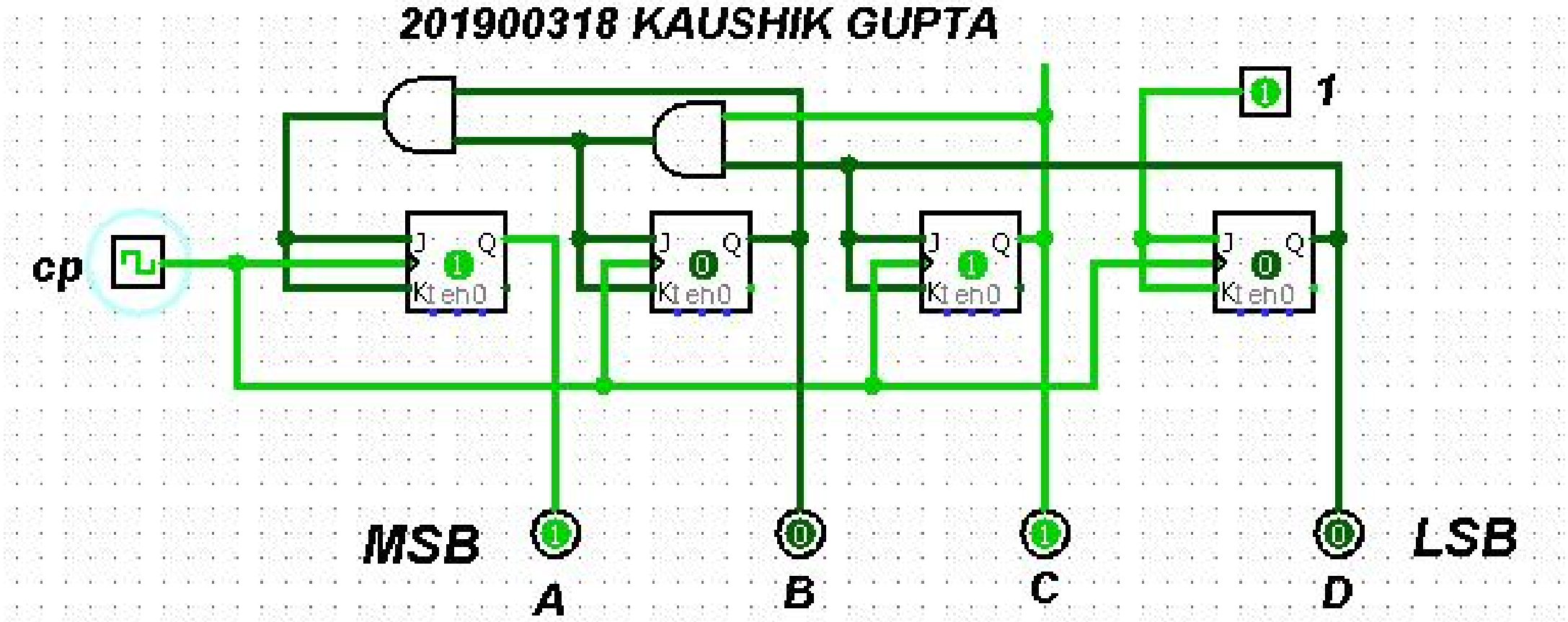
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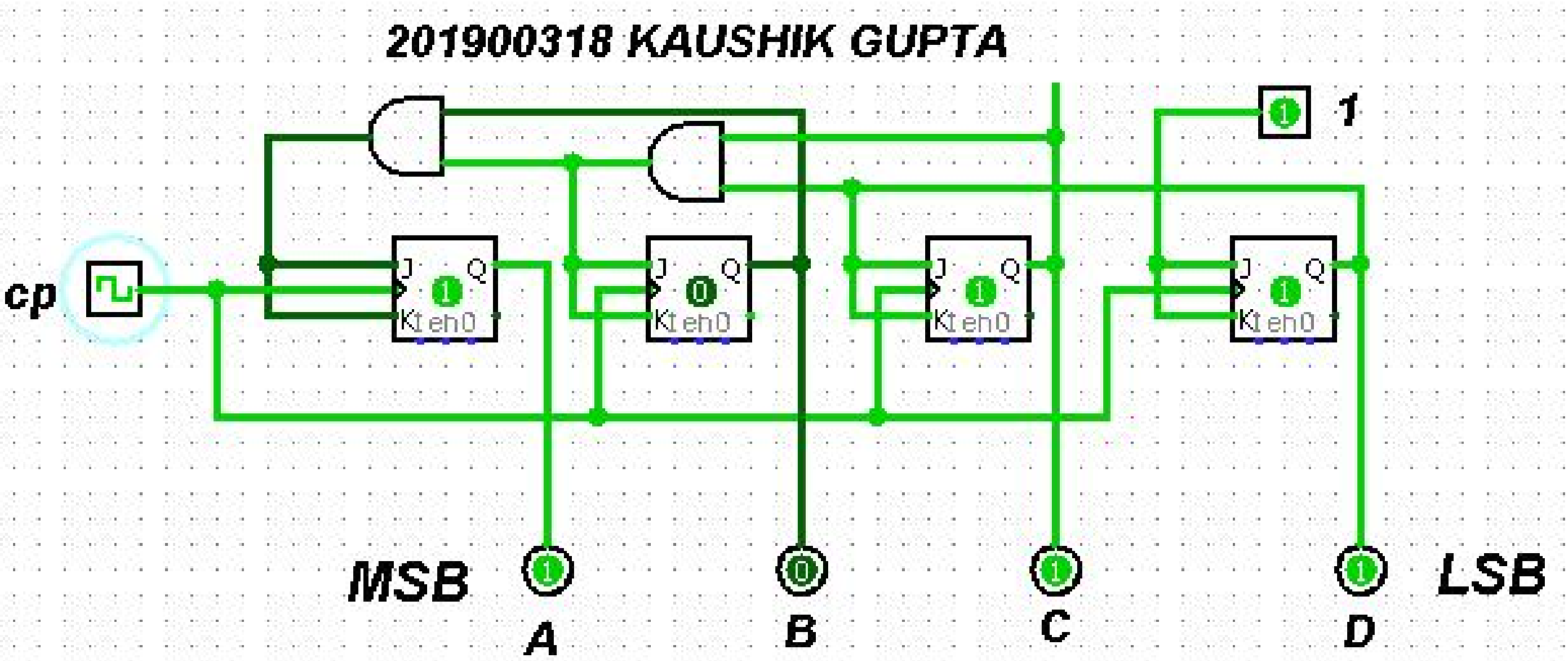
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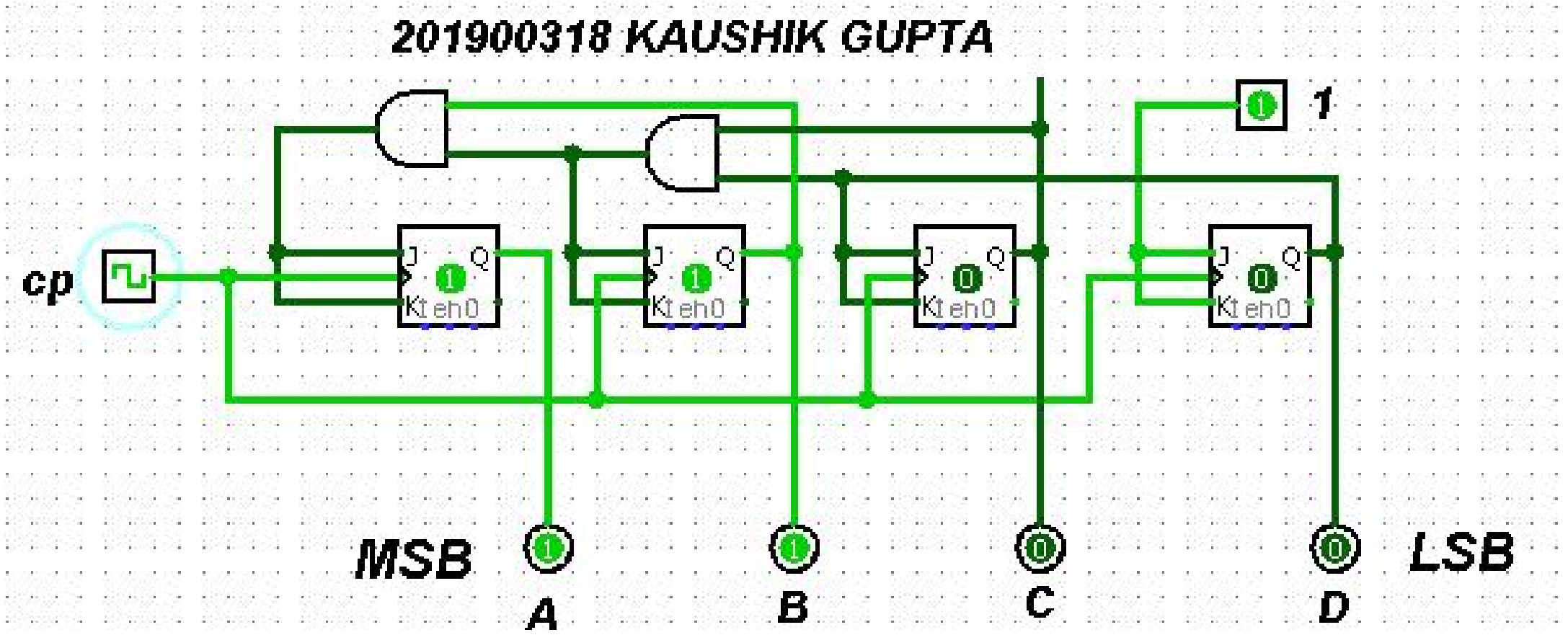
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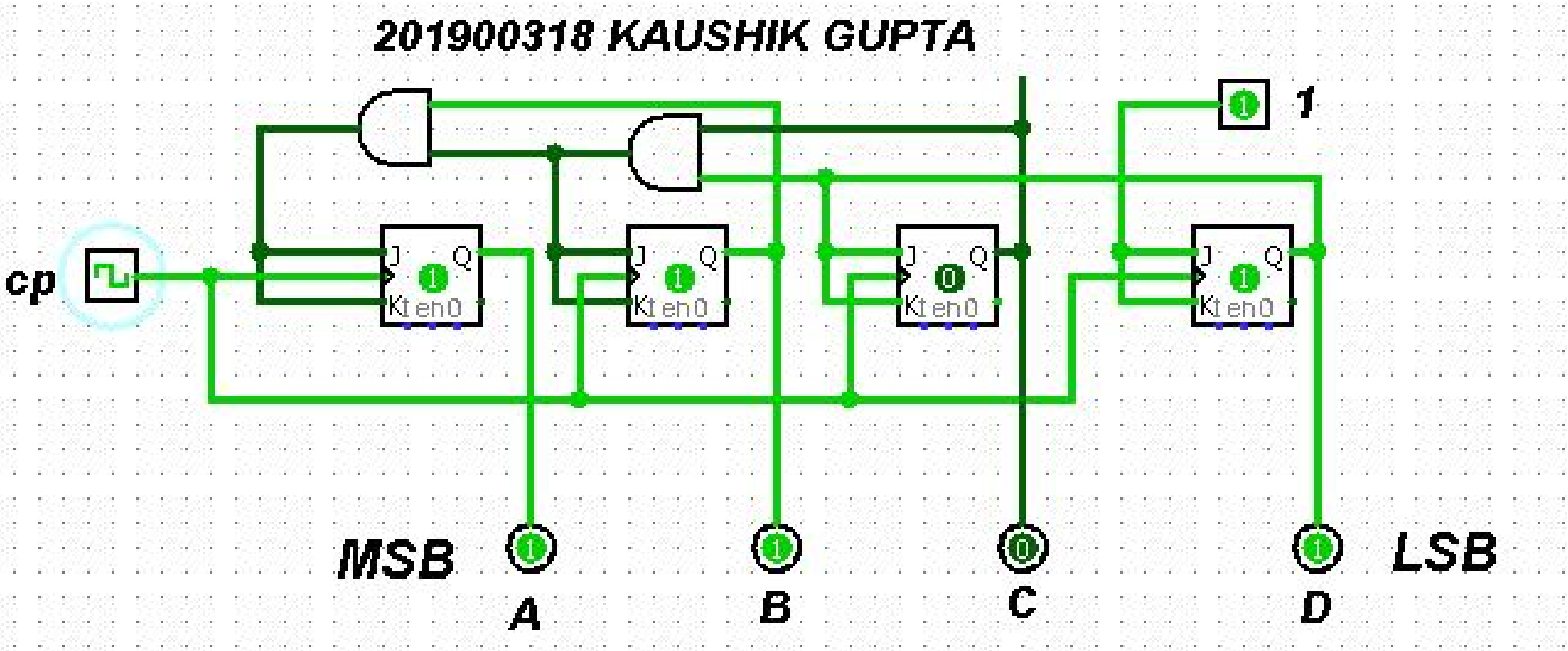
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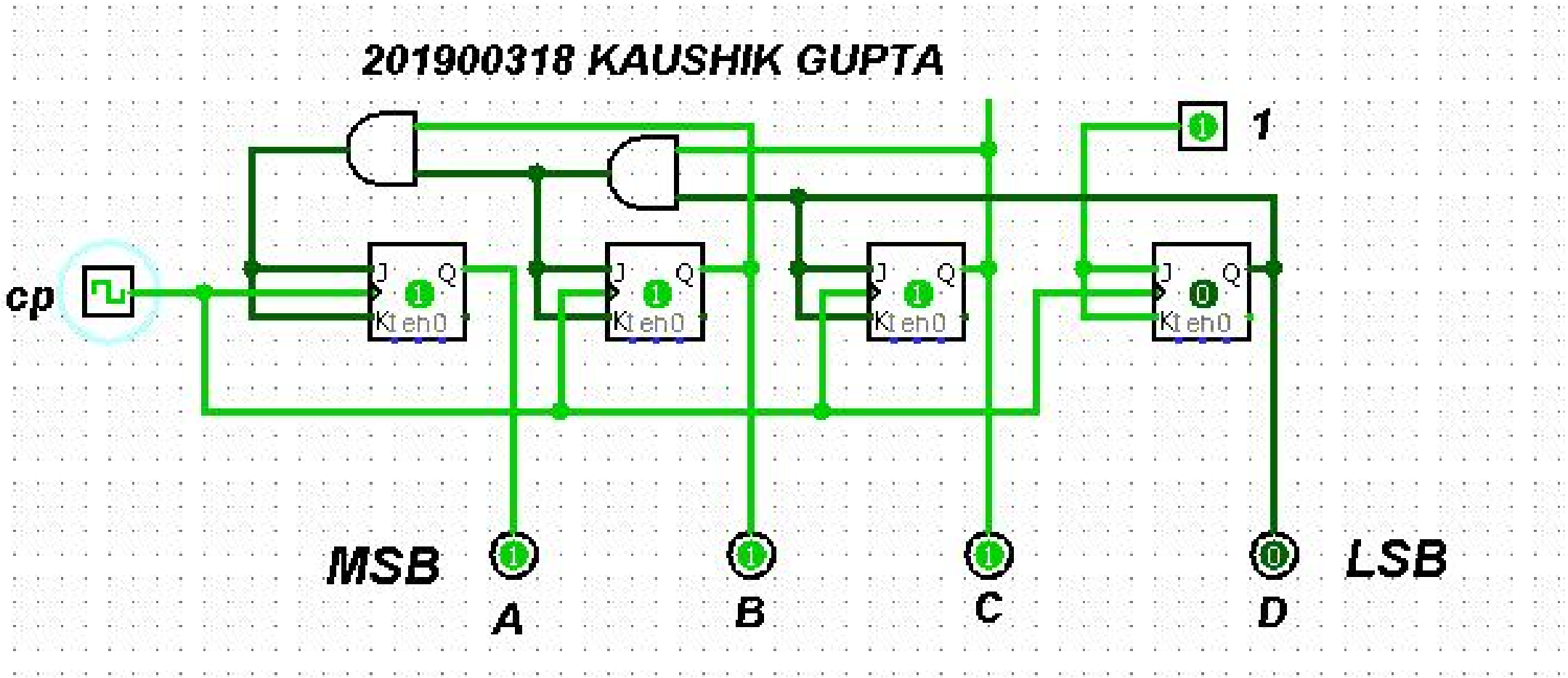
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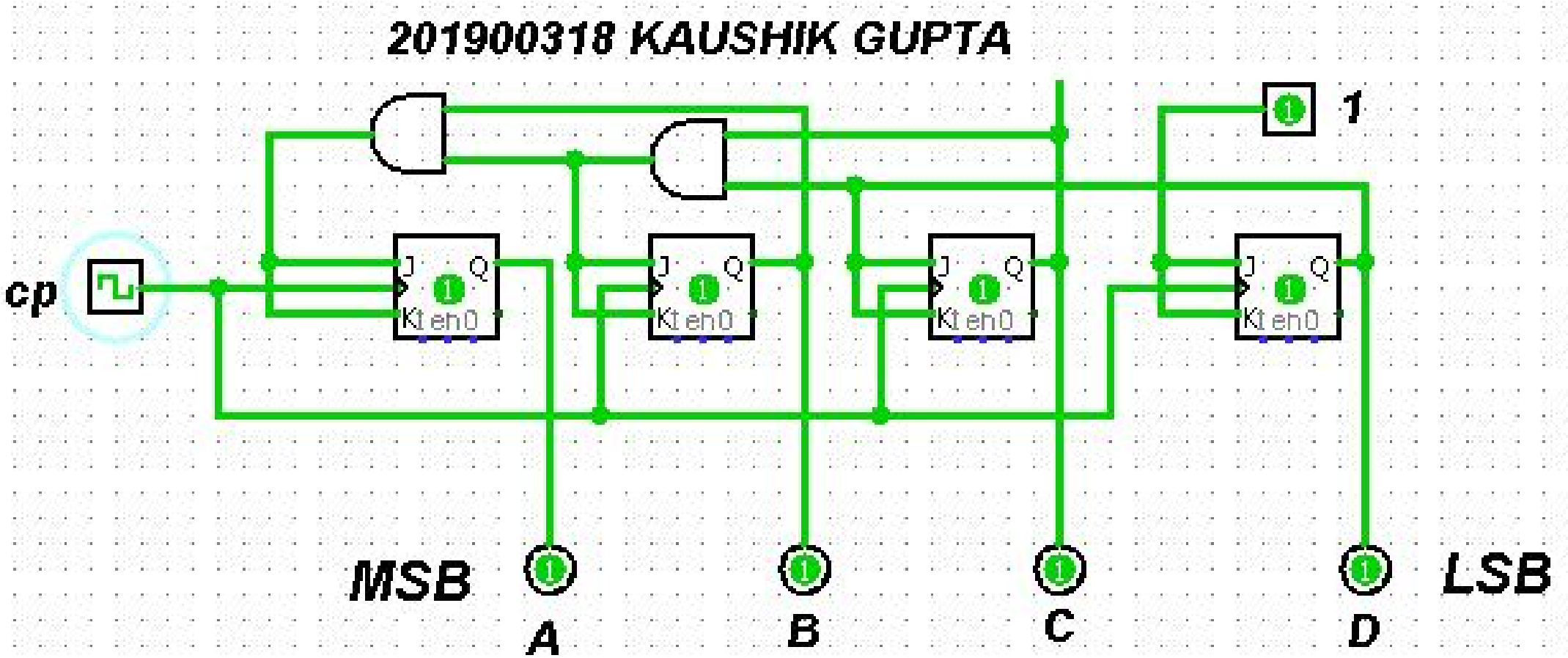
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