

exp No: 15.

exp Name: Verification of registers.

Aim: To realize and study of shift register in.

- (i) SISO
- (ii) SIPO
- (iii) PIPo
- (iv) PISO.

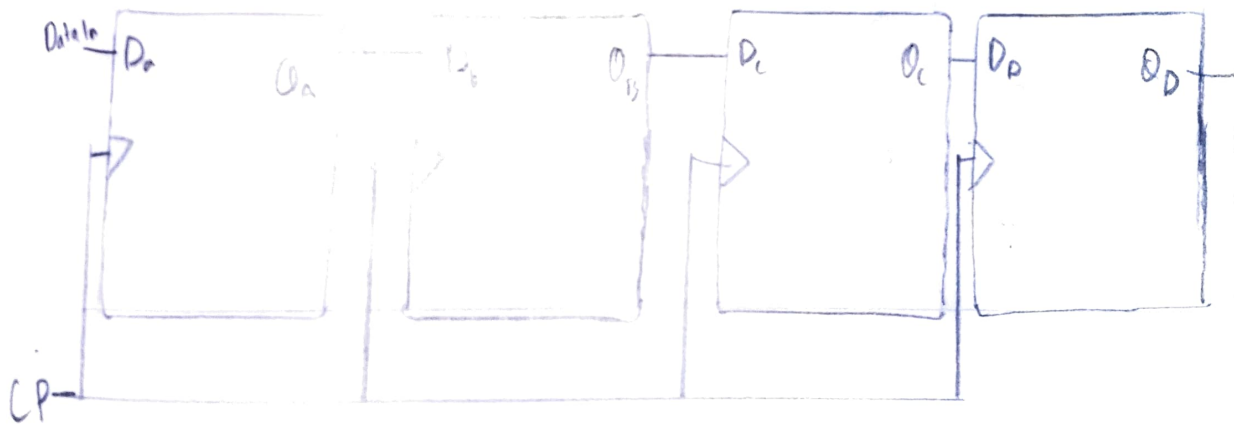
Apparatus needed:

D flip flop - 1C7474 2

2:1 mux - 3

Connecting wires

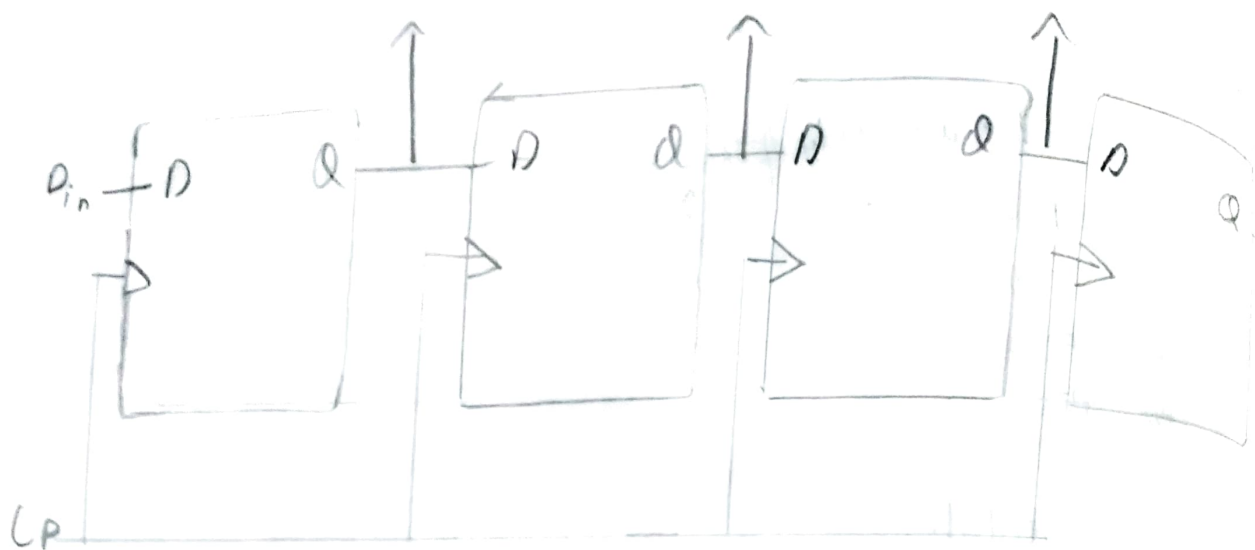
Theory: (SISO)



CP	Data inP	Op
0	1	x
1	0	x
2	1	x
3	0	x
4	1	*
5	0	0

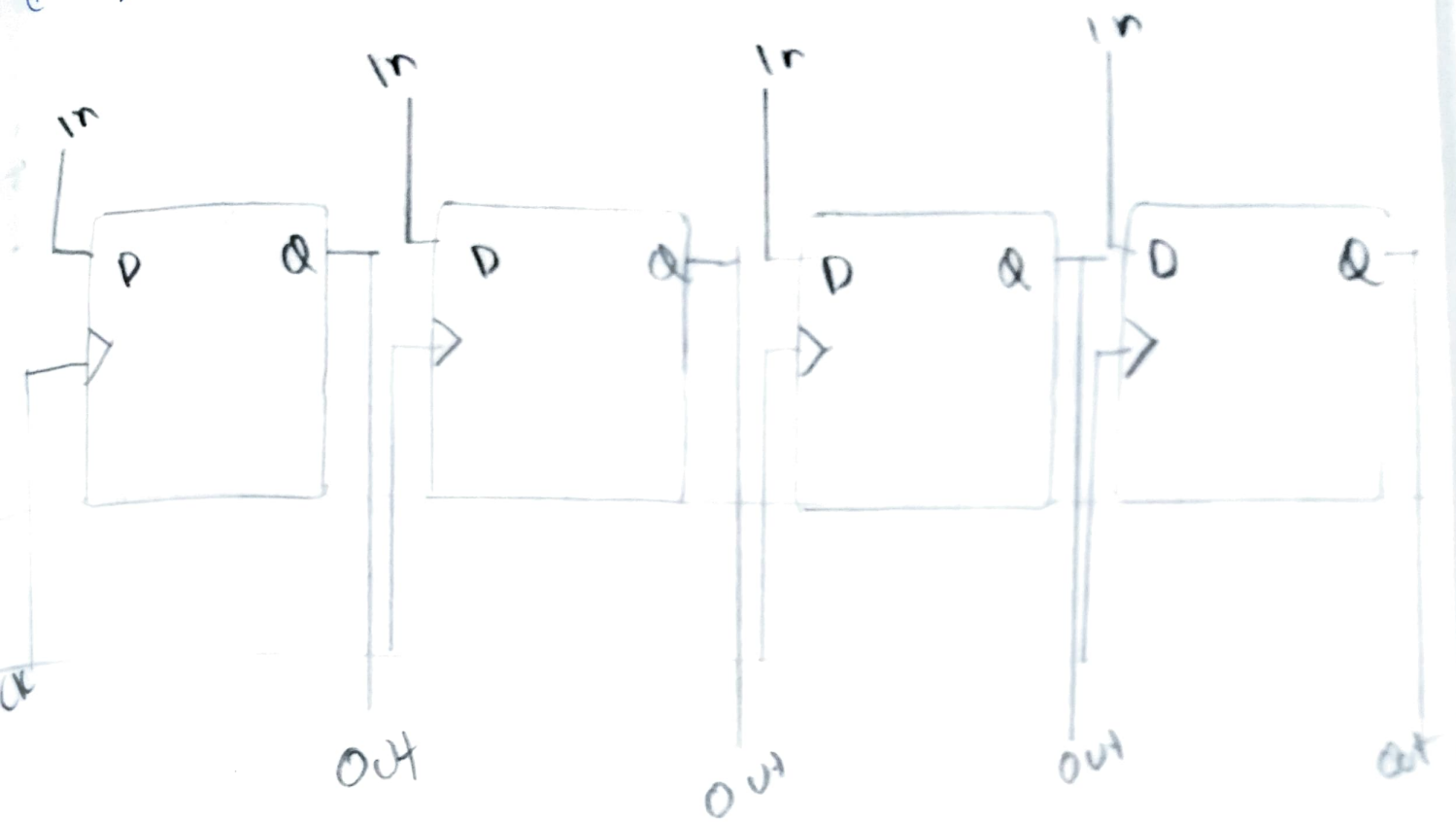
(ii) (51 Po)

(Dout) (↑)



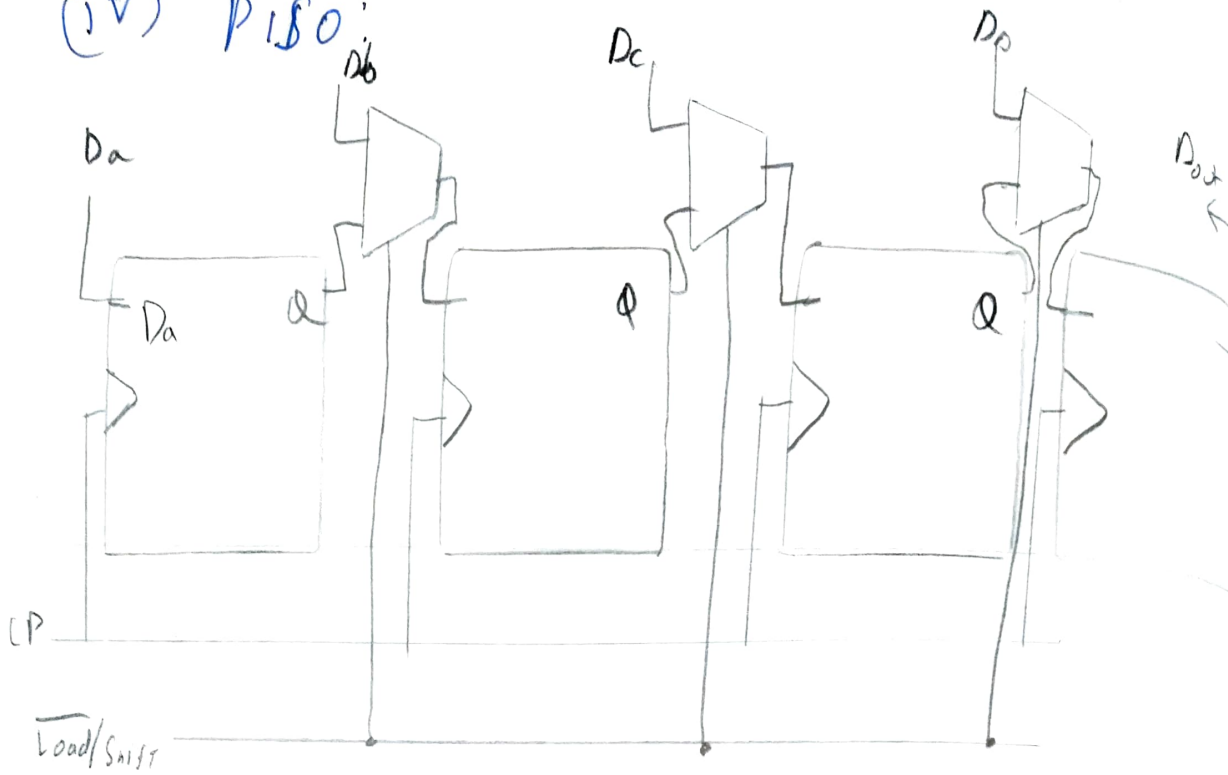
CP	Data <sub>in</sub>	Q <sub>n</sub>	Q <sub>s</sub>	Q <sub>c</sub>	Q <sub>o</sub>
0	1	X	X	X	X
1	0	1	X	X	X
2	1	0	1	X	X
3	0	1	0	0	X
4	1	0	1	1	1

(4) PIPO



CP	Data in				$Q_A$	$Q_B$	$Q_C$	$Q_D$
	$D_A$	$D_B$	$D_C$	$D_D$				
0	1	0	1	0	x	x	x	x
1	x	x	x	x	1	0	1	0

(1V) PISO



#### PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

#### Student's Observations:

- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

Name: kaushik Gupta

Regno: 201900318

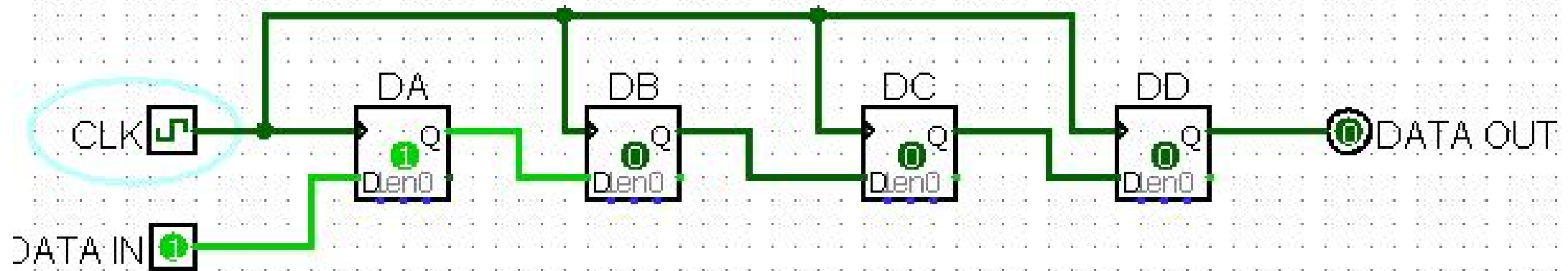
Date: 20/4/21

Sign: kaushik

*kaushik gupta*

201900318

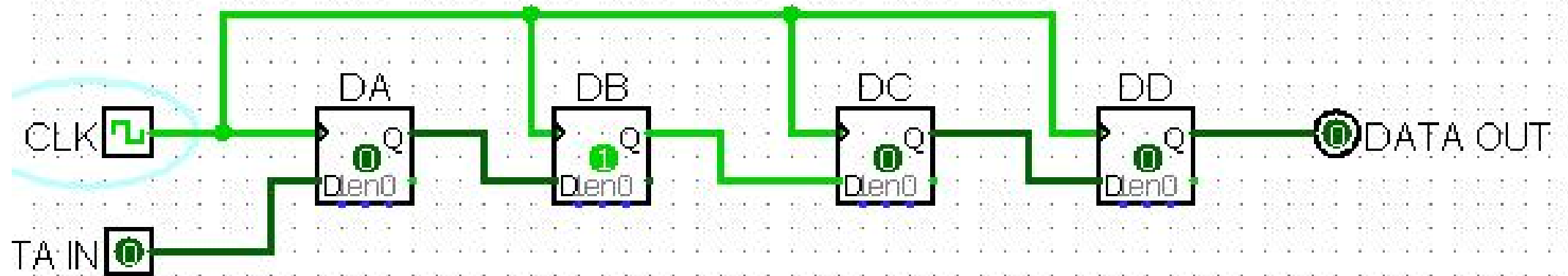
## SERIAL IN SERIAL OUT (SISO)



*kaushik gupta*

201900318

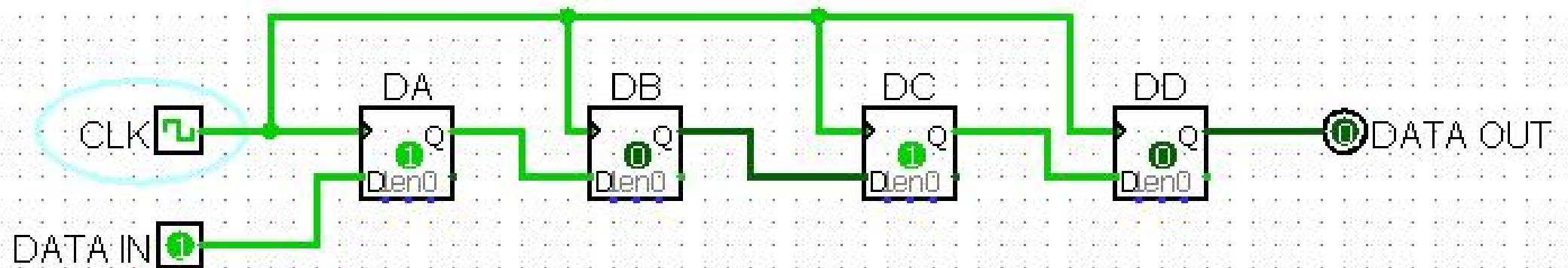
## SERIAL IN SERIAL OUT (SISO)



***kaushik gupta***

**201900318**

## **SERIAL IN SERIAL OUT (SISO)**

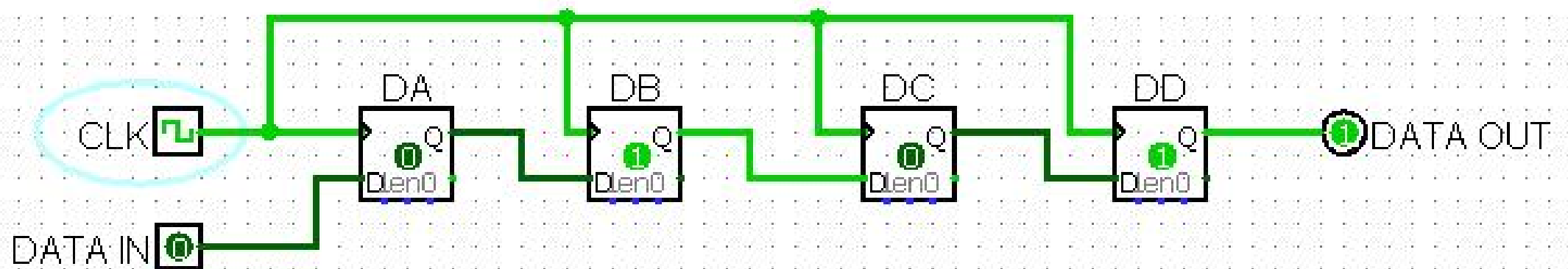




**kaushik gupta**

**201900318**

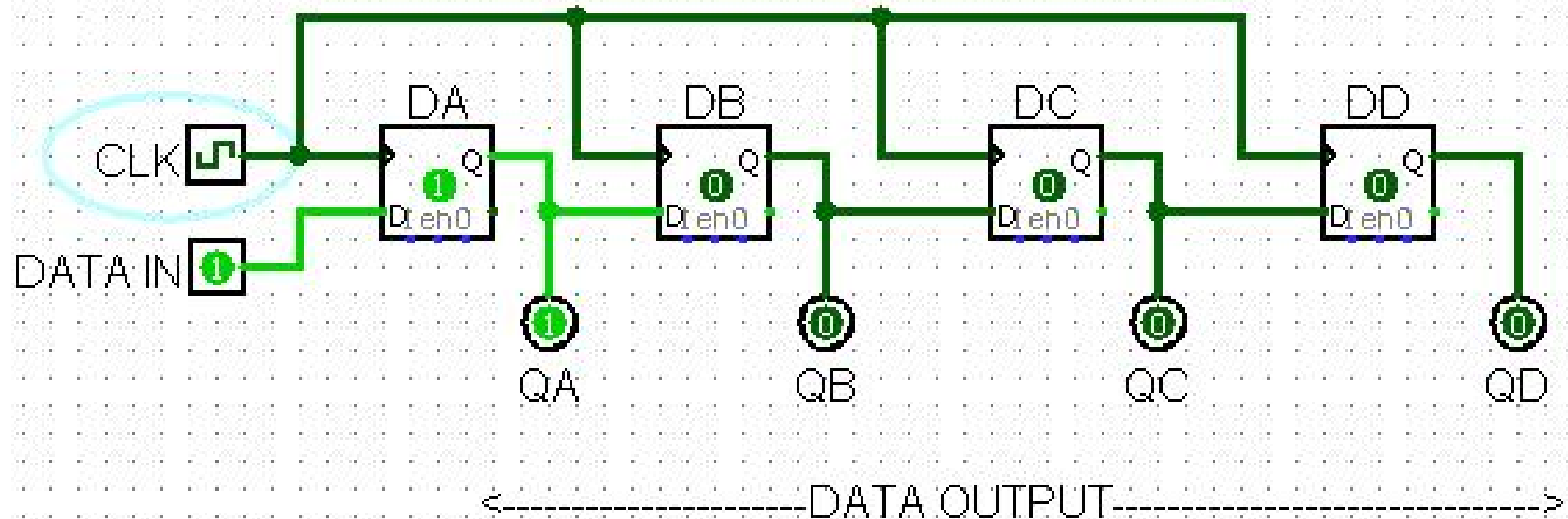
## **SERIAL IN SERIAL OUT (SISO)**



kaushik gupta

201900318

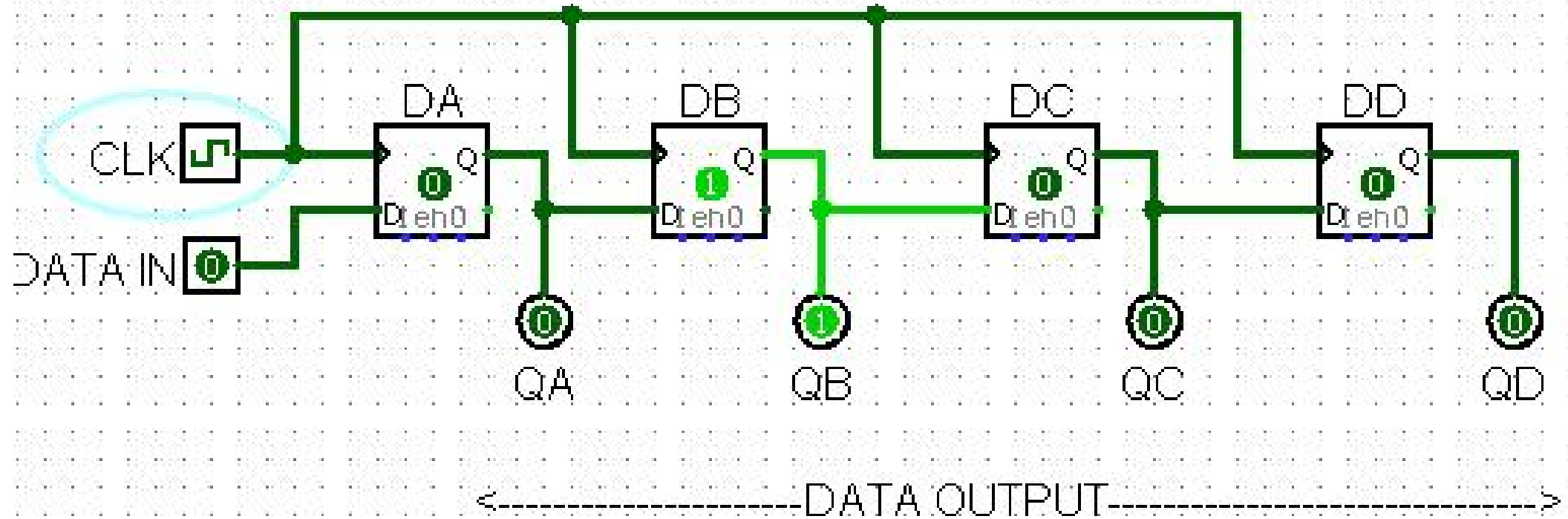
## SERIAL IN PARALLEL OUT (SIPO)



kaushik gupta

201900318

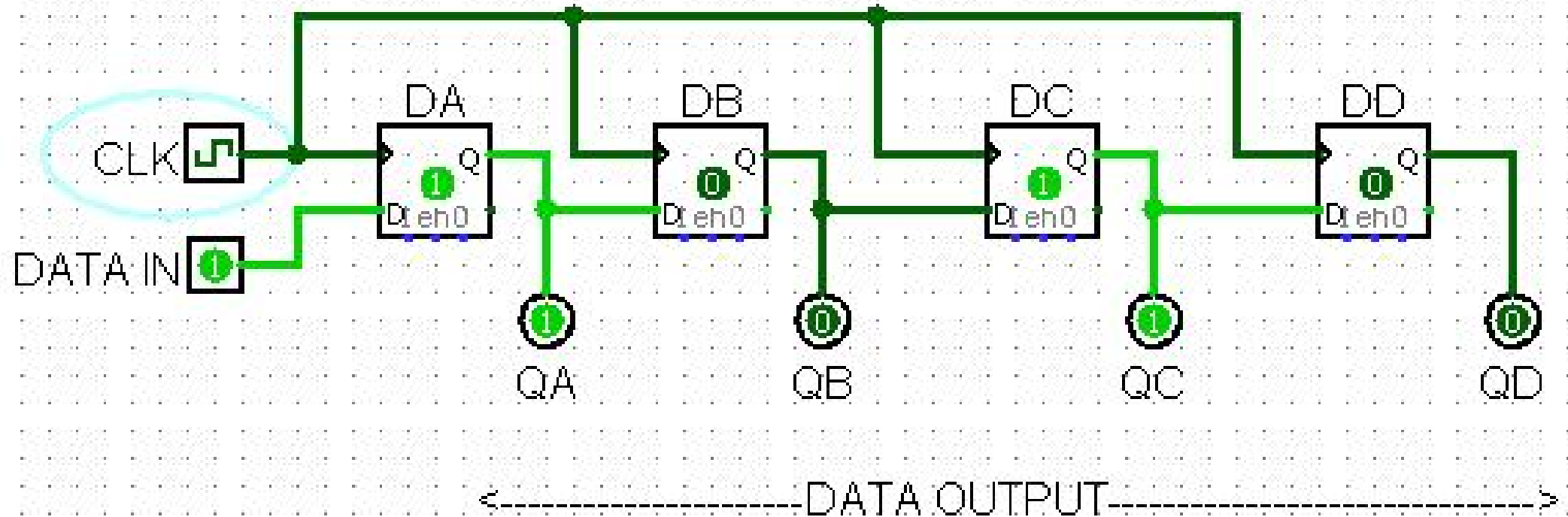
## SERIAL IN PARALLEL OUT (SIPO)



kaushik gupta

201900318

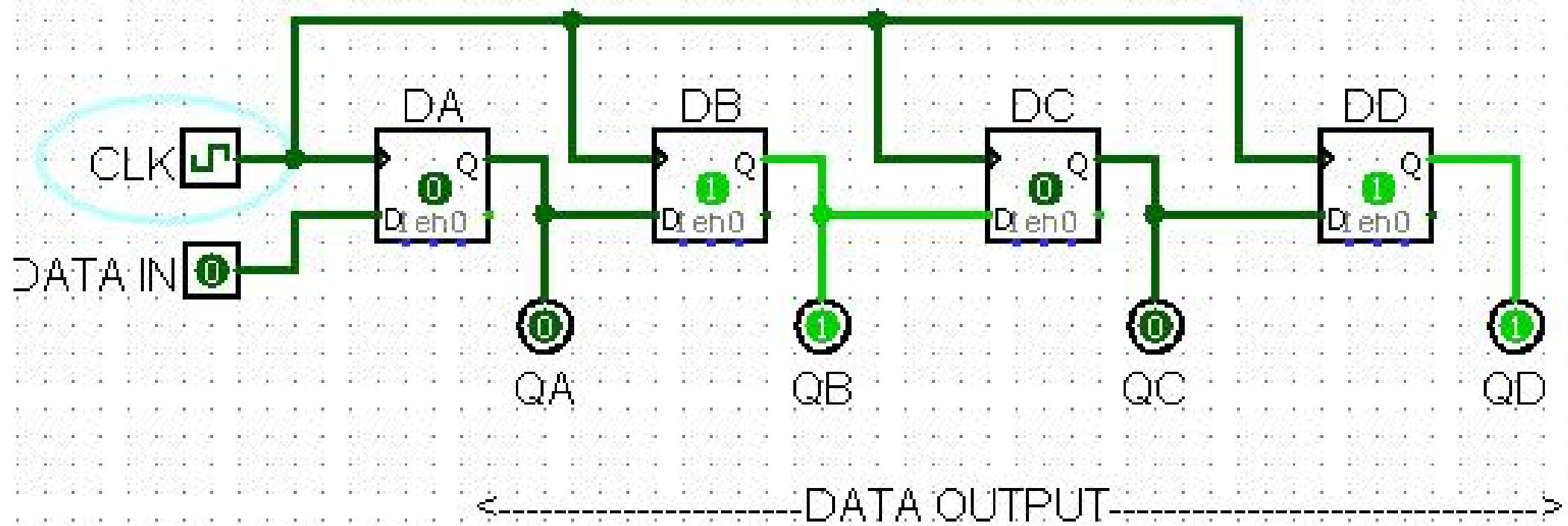
## SERIAL IN PARALLEL OUT (SIPO)



kaushik gupta

201900318

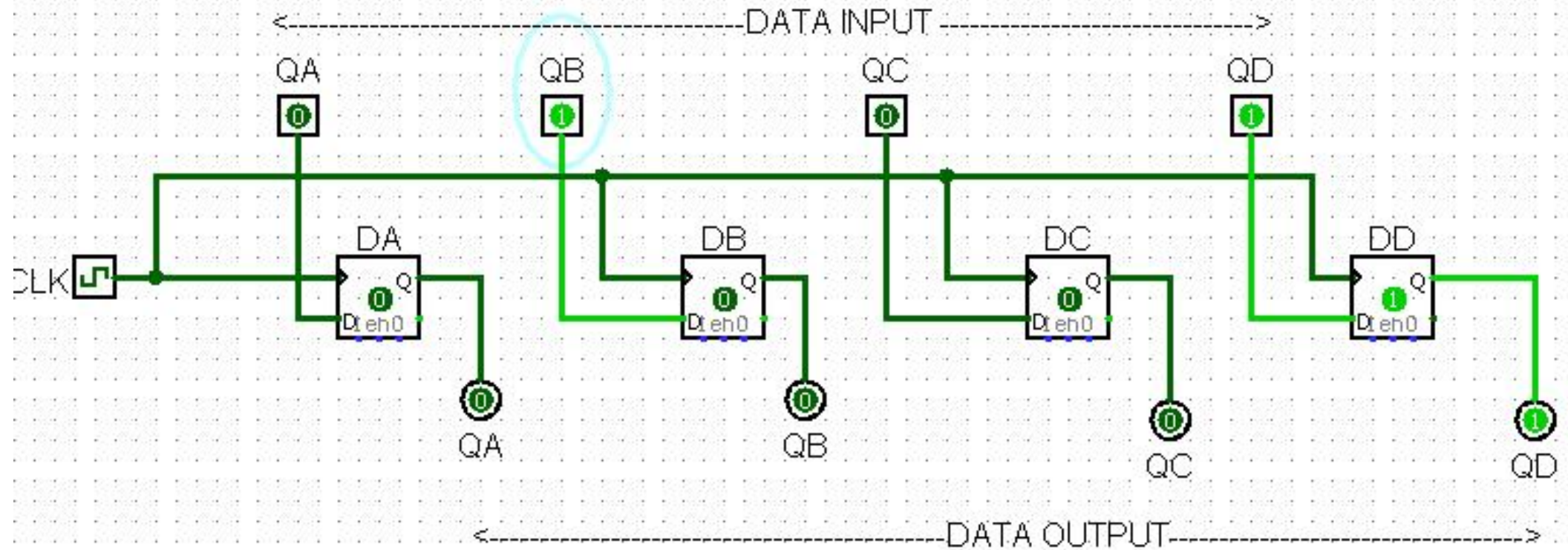
## SERIAL IN PARALLEL OUT (SIPO)



kaushik gupta

201900318

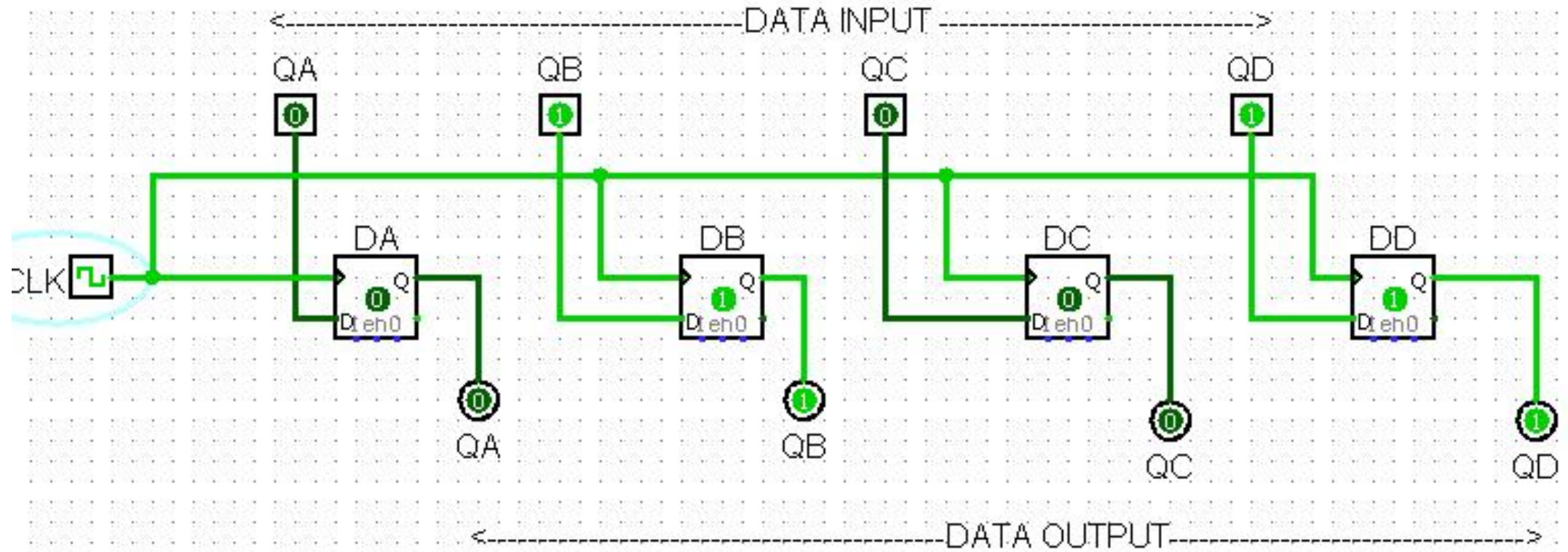
### PARALLEL IN PARALLEL OUT (PIPO)



kaushik gupta

201900318

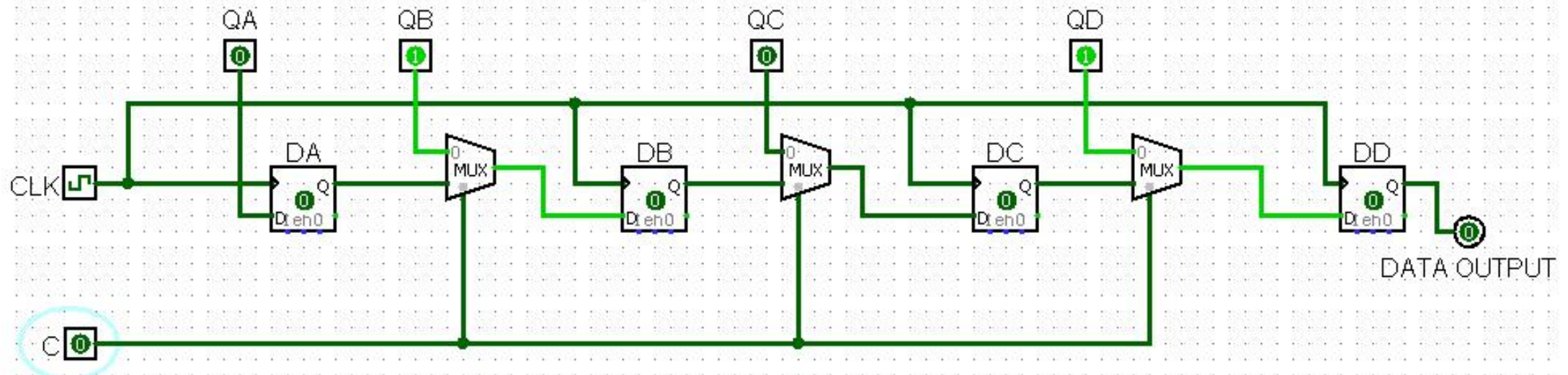
## PARALLEL IN PARALLEL OUT (PIPO)





201900318

DATA INPUT

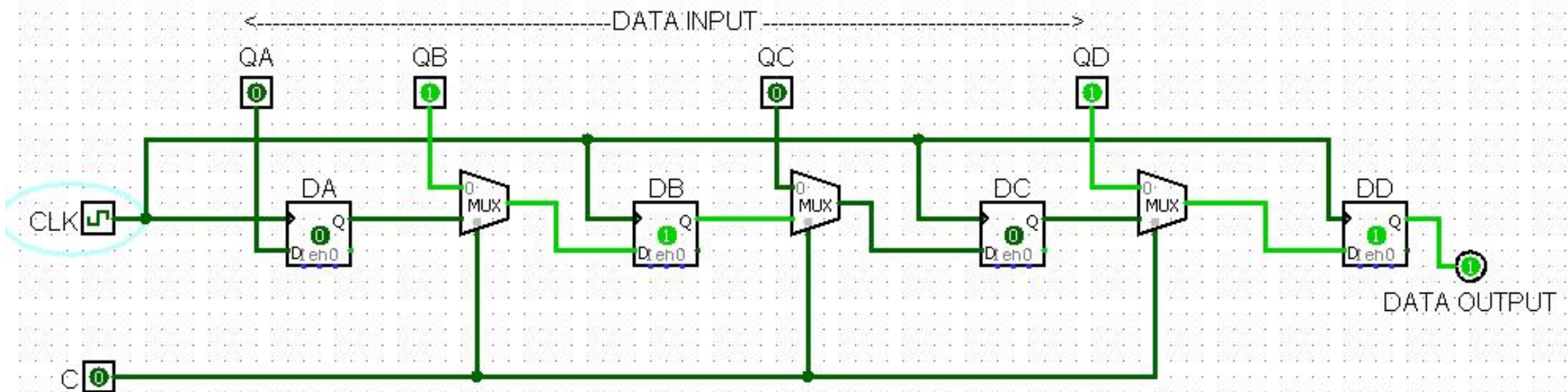




kaushik gupta

201900318

### PARALLEL IN SERIAL OUT (PISO)



kaushik gupta

201900318

### PARALLEL IN SERIAL OUT (PISO)

