Date:

EXPNO: 7

Name: Design a mod 4 Synchronous up/down coonter with a control line using D flip flops.

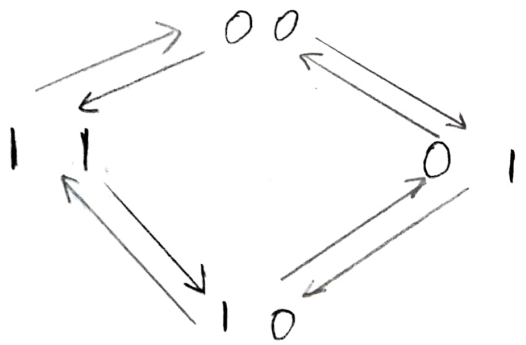
Aparatus used:

1- D flip flops - 2
2. Xor gate - 1
3. clock

Theory:

Up/down coonter is a combination of both up counter and down counter. It has a control line to select weather the counter is upcounter of do wn coonter.
& Since its synchronous counter it has common clock for both flip flops.

State diagram:



State table:

Cntrl I/P	Present State		Next State		Excitation table for DFF	
C	Q_A	Q_B	Q_{AN}	Q_{BN}	D_A	D_B
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

K-maps:

1) D_A

C \ $Q_A Q_B$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$D_A = C \oplus Q_A \oplus Q_B$

2) D_B

C \ $Q_A Q_B$	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$D_B = Q_B'$

Practical Procedure:

1.) Ic's are placed on bread board

2) Connection are made as per designed circuit

3) make sure of Power Supply is Proper adiquit

Obsrvations:

1. A synchronous 2-bit **up/down counter** built from D flipflops. Depending on the logic value on the *Up/down* input, the counter will increment or decrement its value on the falling edge of the clock signal. The additional *enable* input down (1) or up(0) counting.

2.in this type of counter the clock supplied id common to all flip flops and can perform both increment and decrement operation based on the control input.

3.Counter are used not only for counting but also for measuring frequency and time ; increment memory addresses . Counter are specially designed synchronous sequential circuits, in which , the state of the counter is equal to the count held in the circuit by the flip flops

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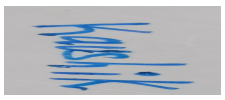
Sign:



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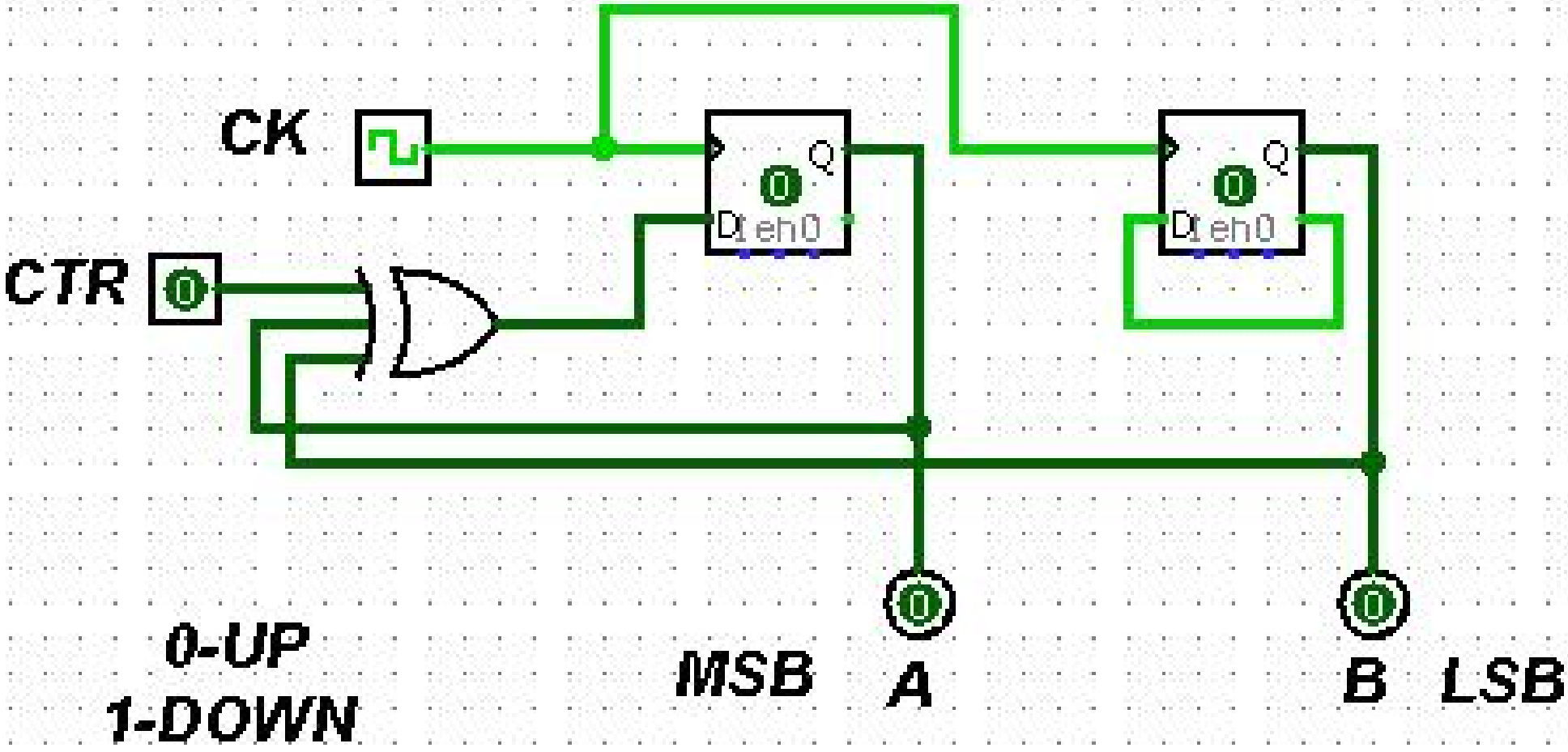

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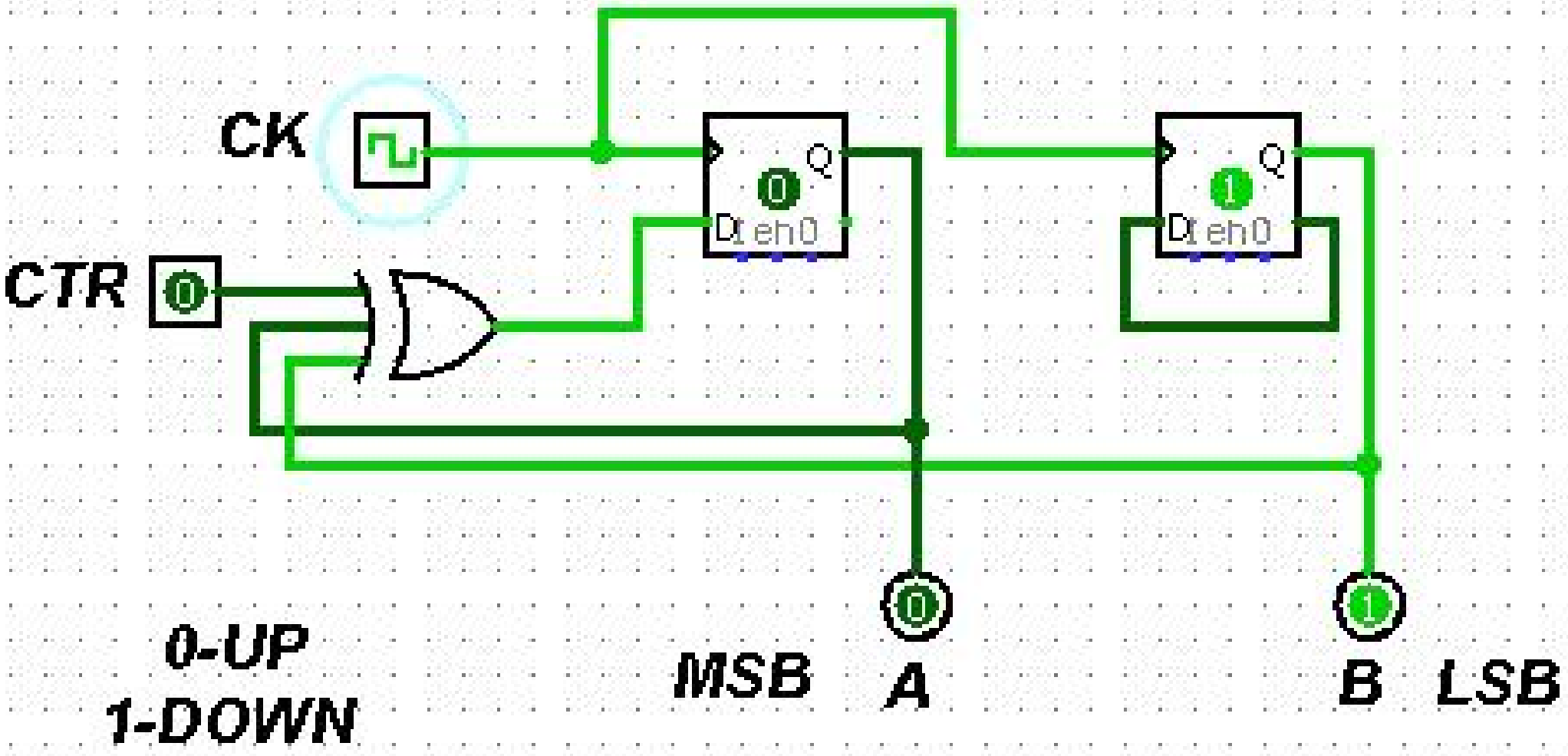

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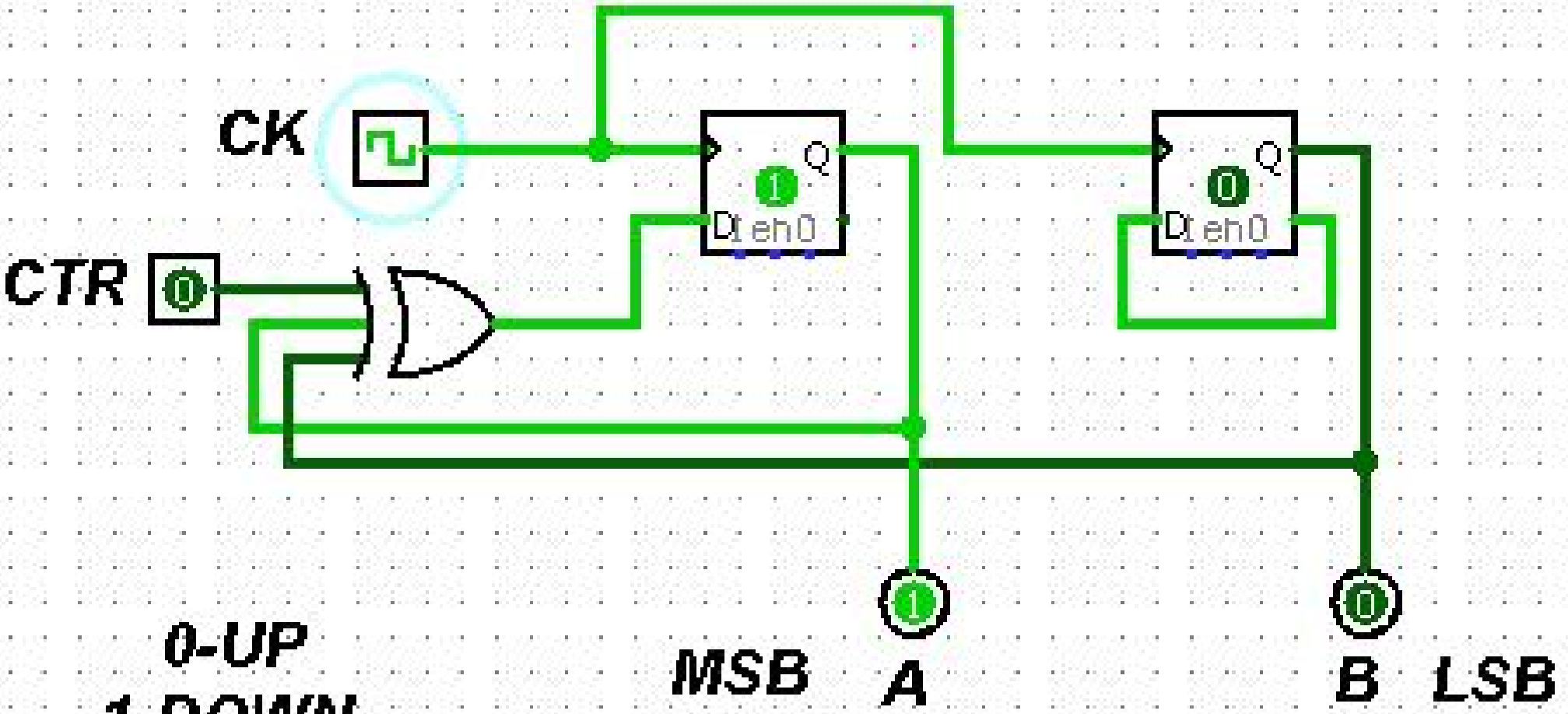

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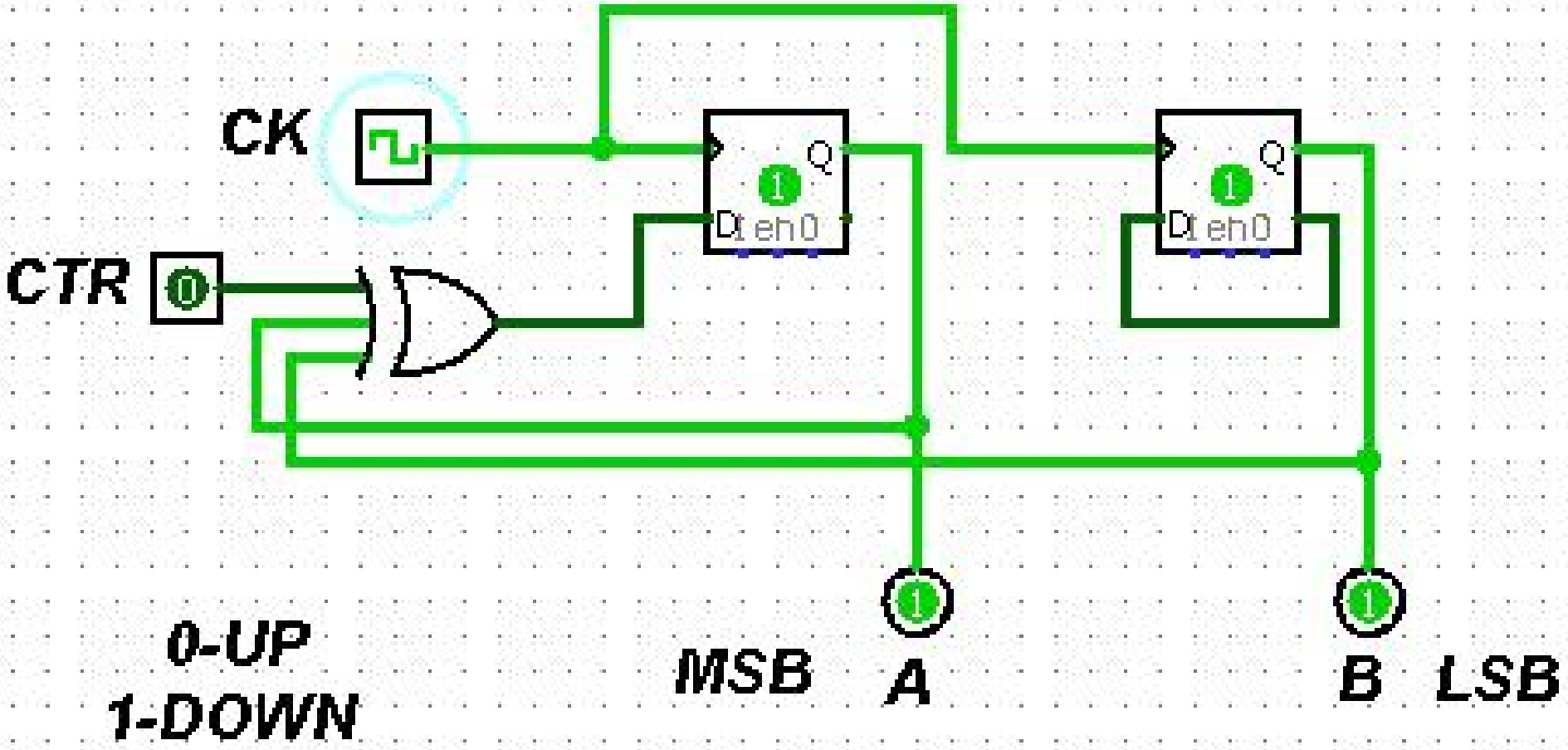

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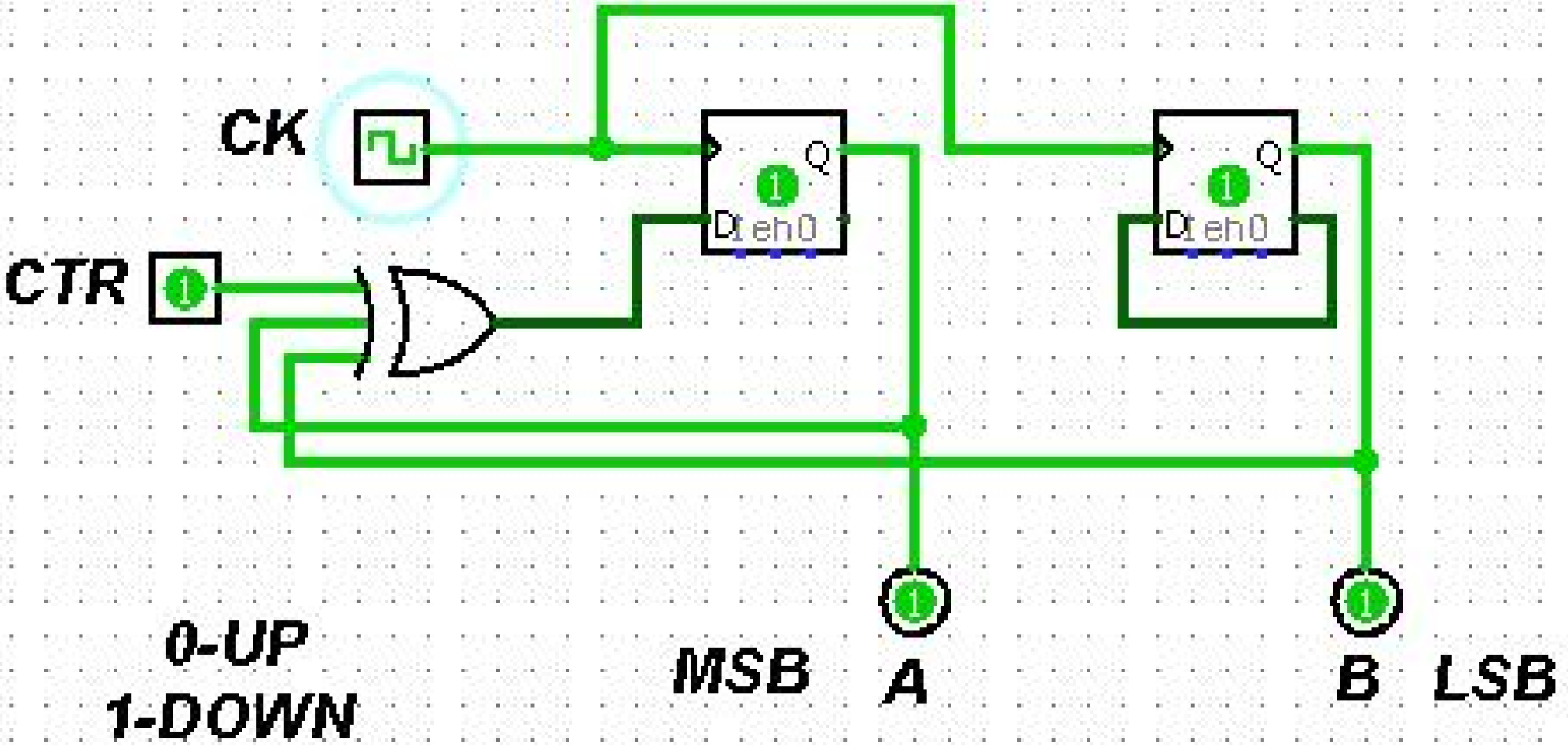

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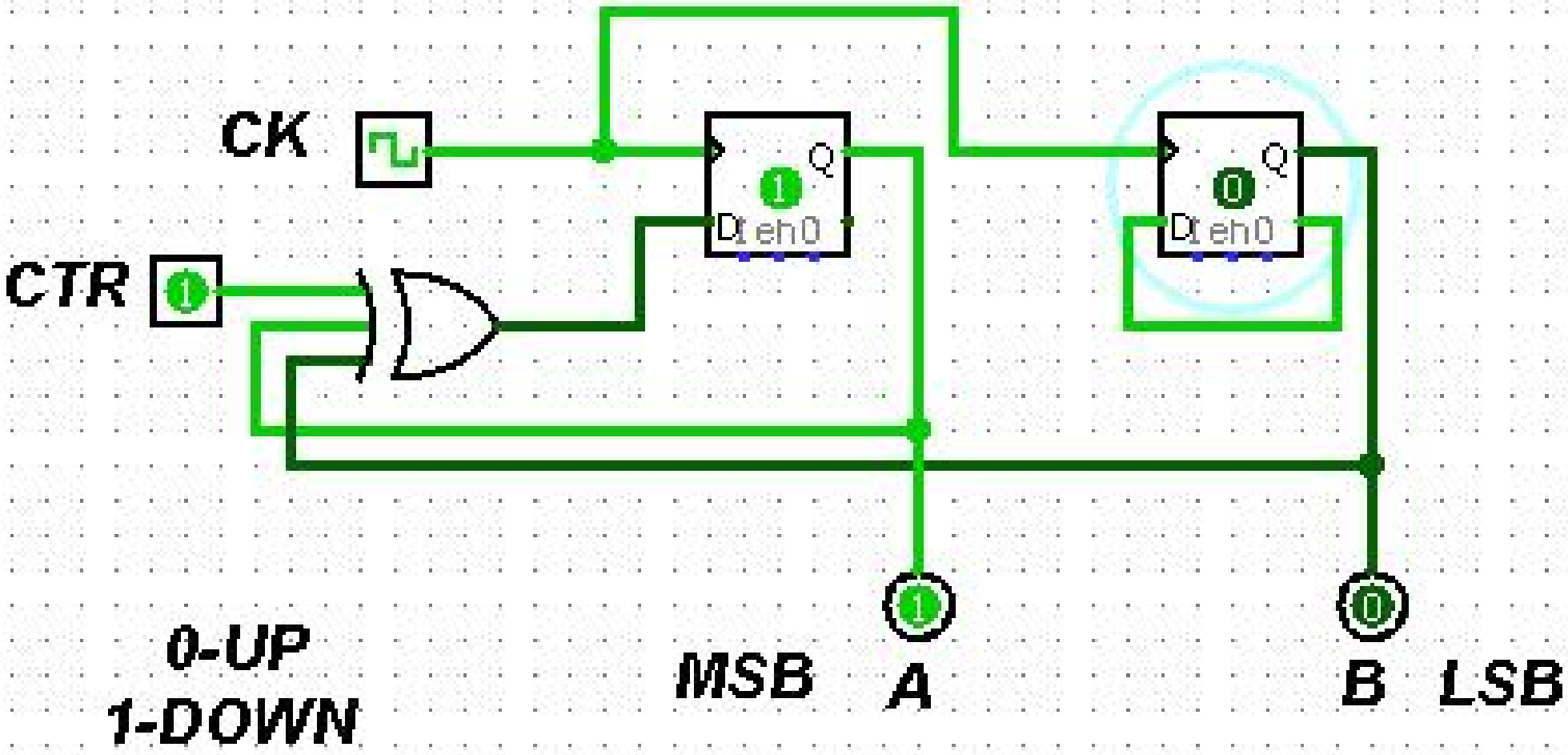

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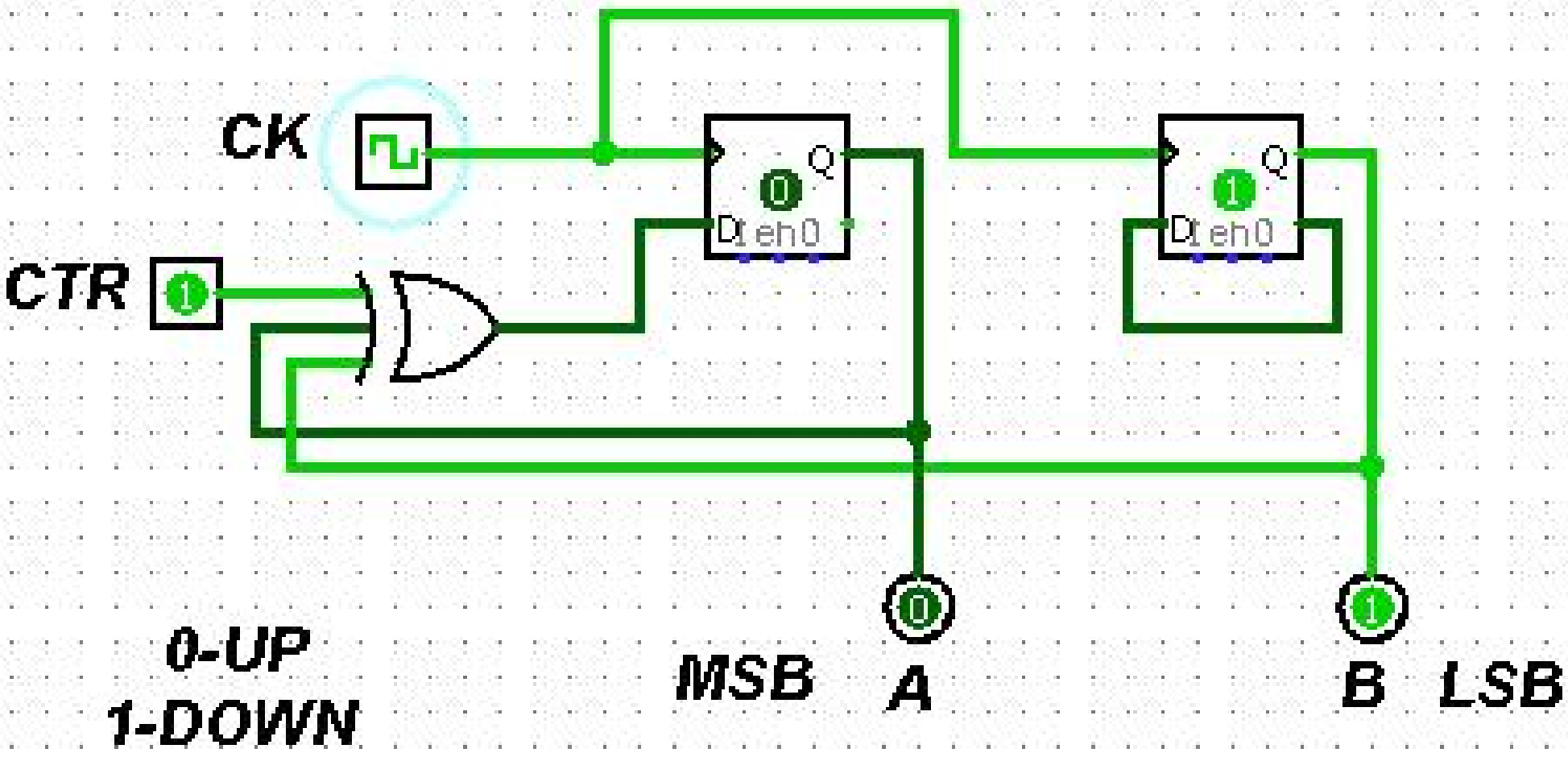

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