EXPERIMENT NUMBER: 10

EXPERIMENT NAME: Design of a mod 16 synchronous up counter using JK FFs.

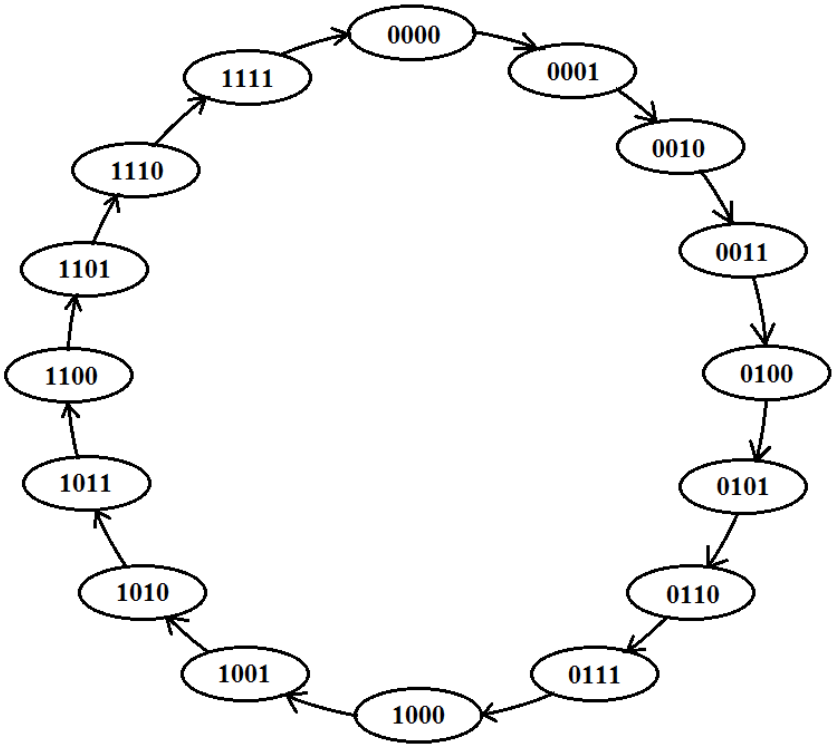
AIM: To design a mod 16 synchronous up counter using JK FFs and verify its state diagram.

APPARATUS REQUIRED:

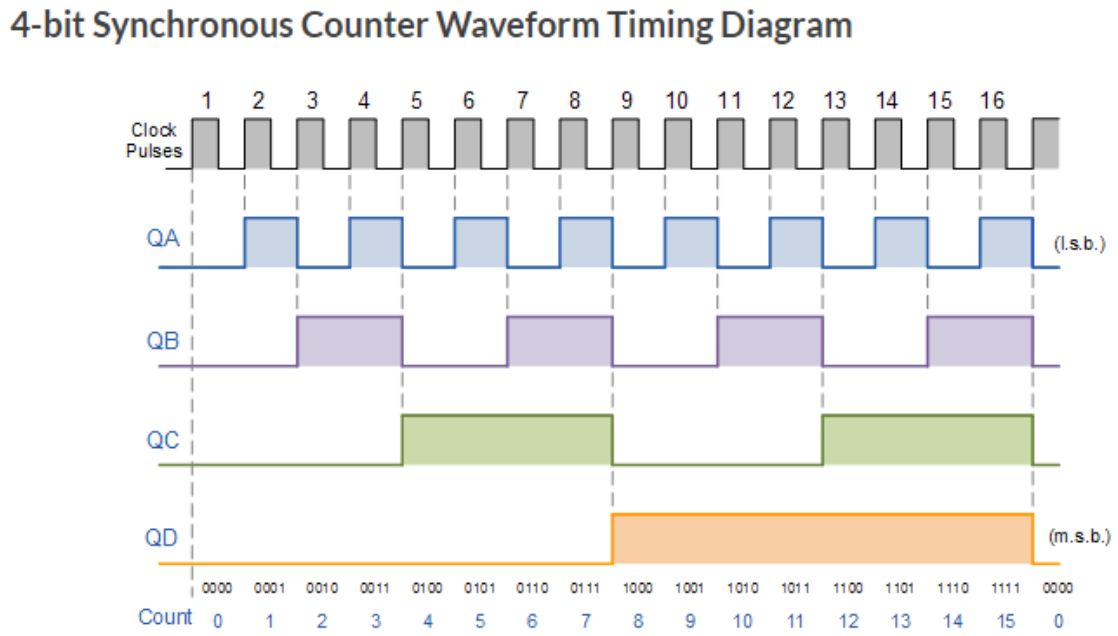
Sl. No.	**COMPONENT**	**SPECIFICATION**	**QUANTITY**
1.	AND GATE	IC 7408	1
2.	JK Flip-flop	IC 7473/IC 7476	2
3.	IC TRAINER KIT	-	1
4.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

STATE DIAGRAM:



TIMING DIAGRAM:



STATE TABLE:

Present State				Next State				Excitation table of JK flip-flop							
Q_A	Q_B	Q_C	Q_D	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

K-Map for J_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

K-Map for K_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

K-Map for J_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

K-Map for K_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	0	X	X	X

K-Map for J_C:

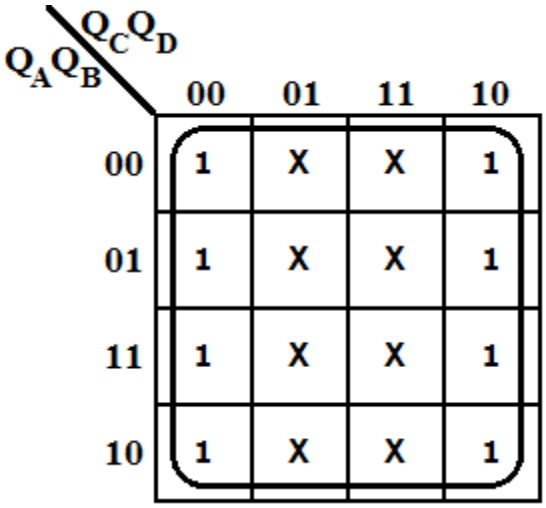
Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

K-Map for K_C:

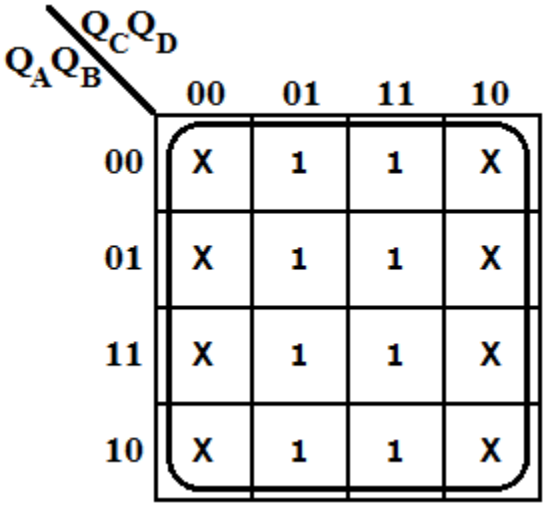
Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

K-Map for J_D:

K-Map for K_D:



Q_AQ_B \ Q_CQ_D	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1



Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

CIRCUIT DIAGRAM OF A MOD 16 SYNCHRONOUS UP COUNTER USING JK FFS:

DESIGN PROCEDURE:

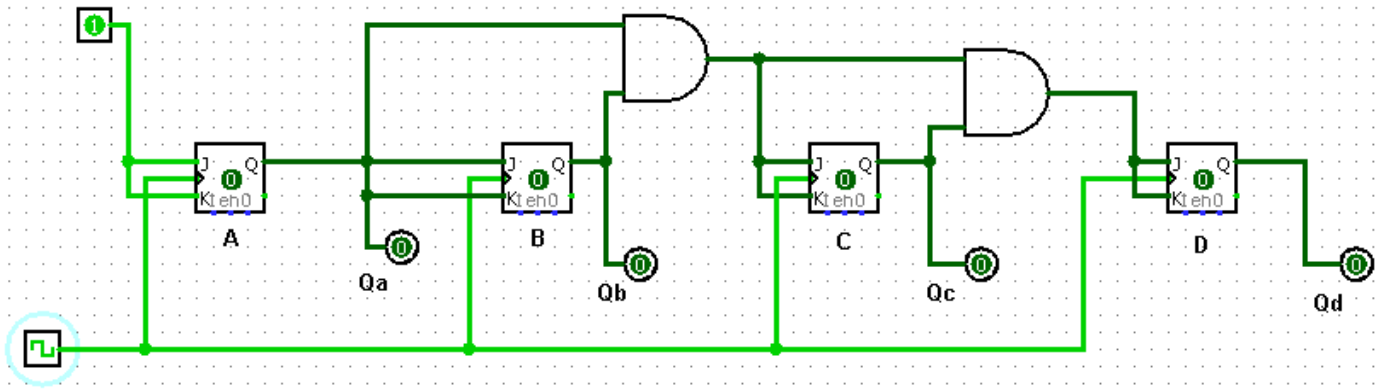
1. Truth table of the 4-bit binary to gray code converter is prepared.
2. K-maps for all the output variables (A, B, C and D) are drawn.
3. Simplified expressions for the output variables are obtained using manual simplification.
4. Circuit diagram is drawn as per the simplified expressions of the output variables obtained in step 3.

PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1

Regd No:201900339 L .Mrinal Raj



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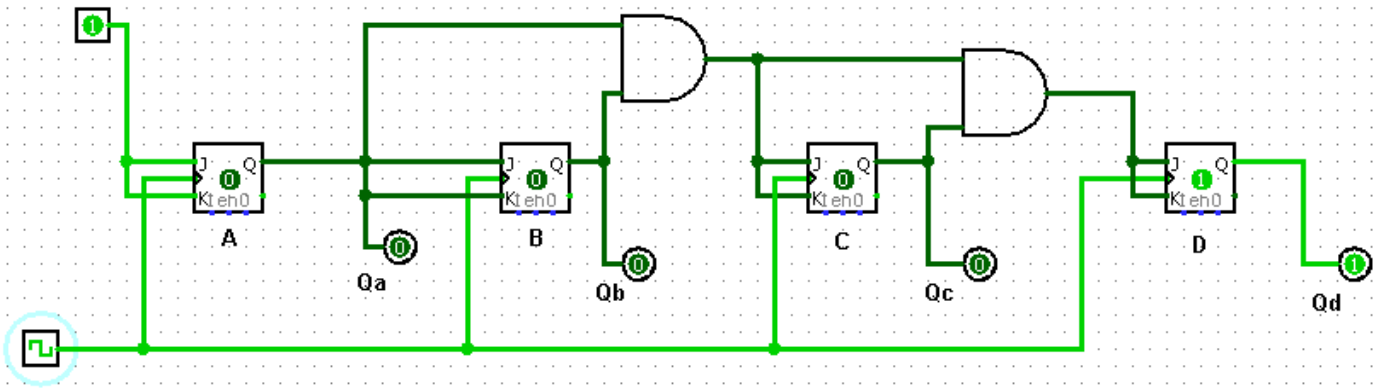

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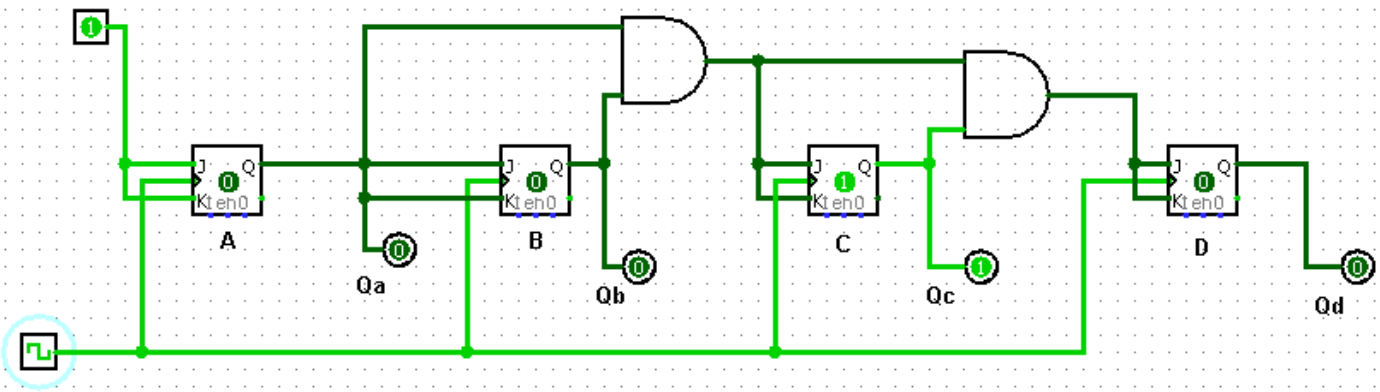

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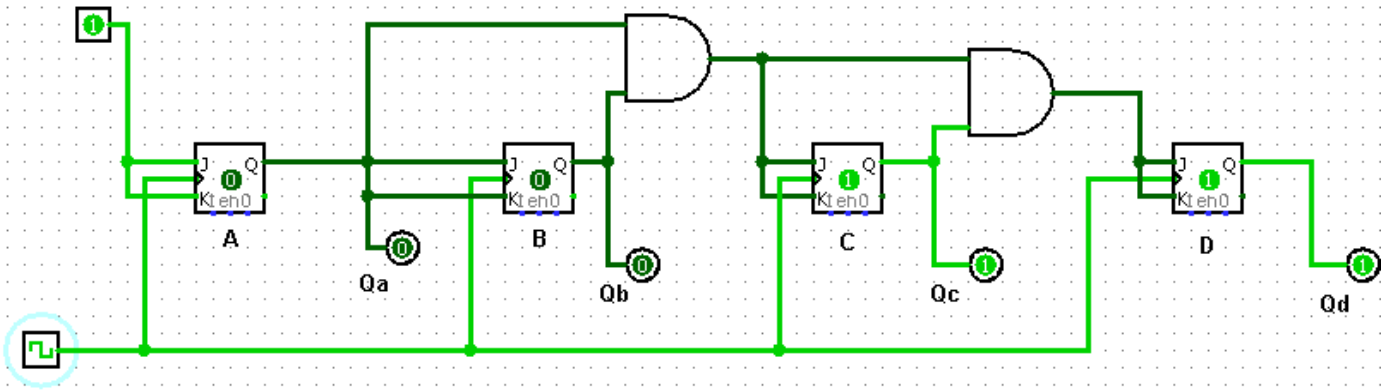

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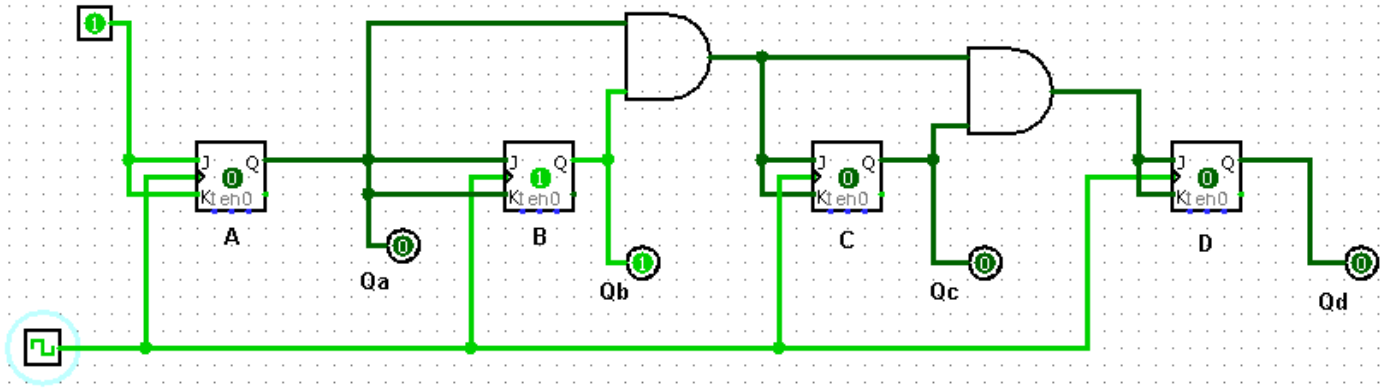

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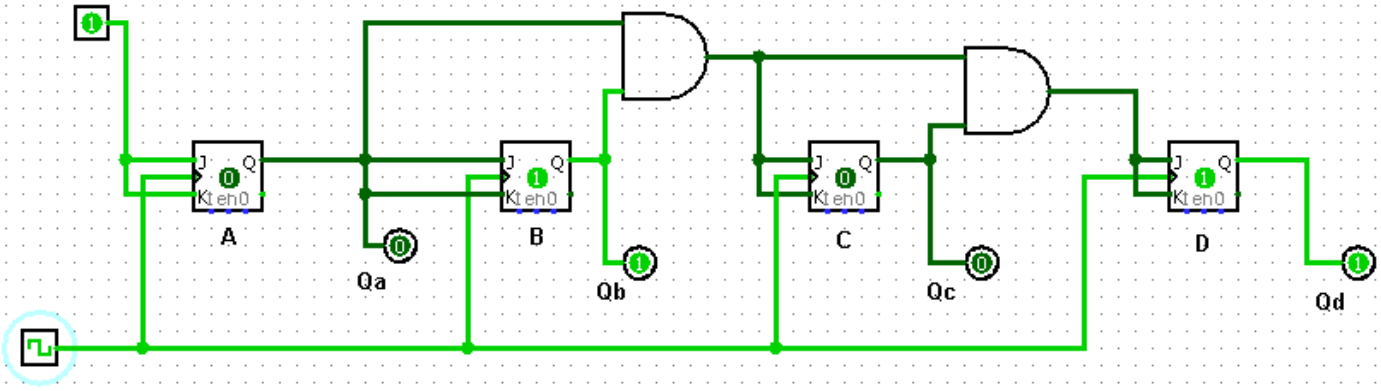

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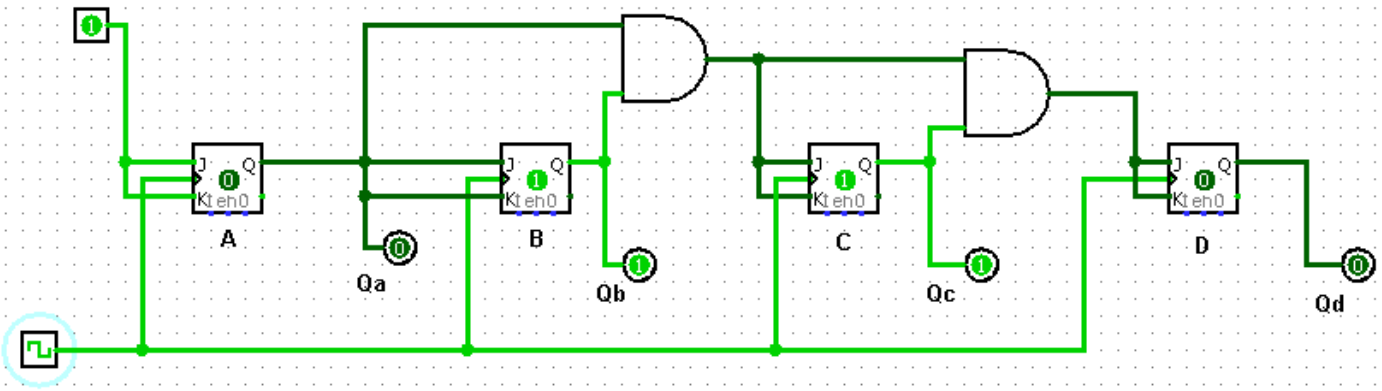

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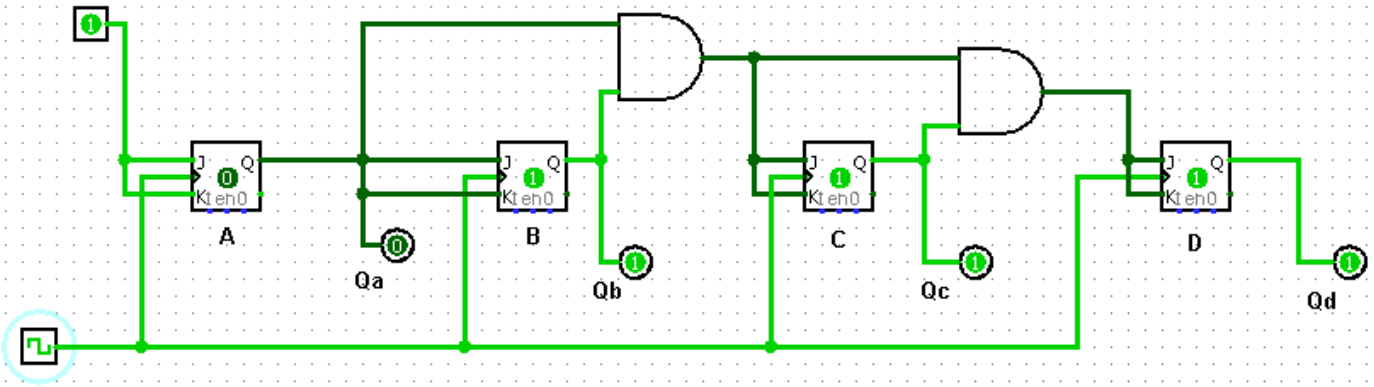

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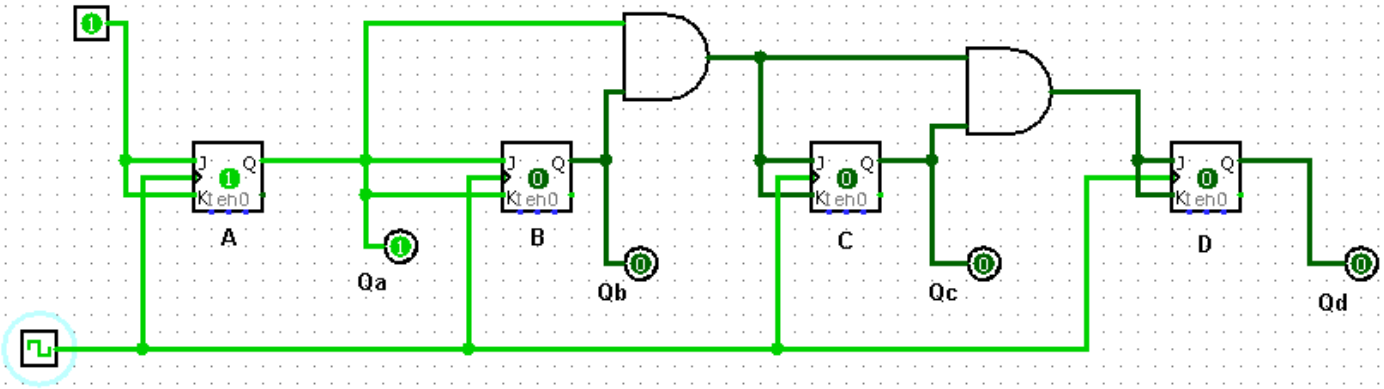

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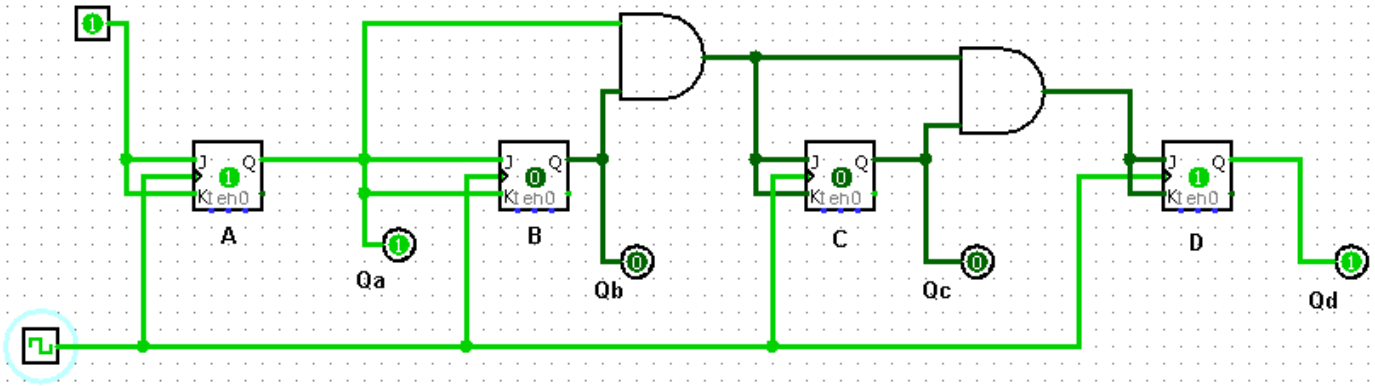

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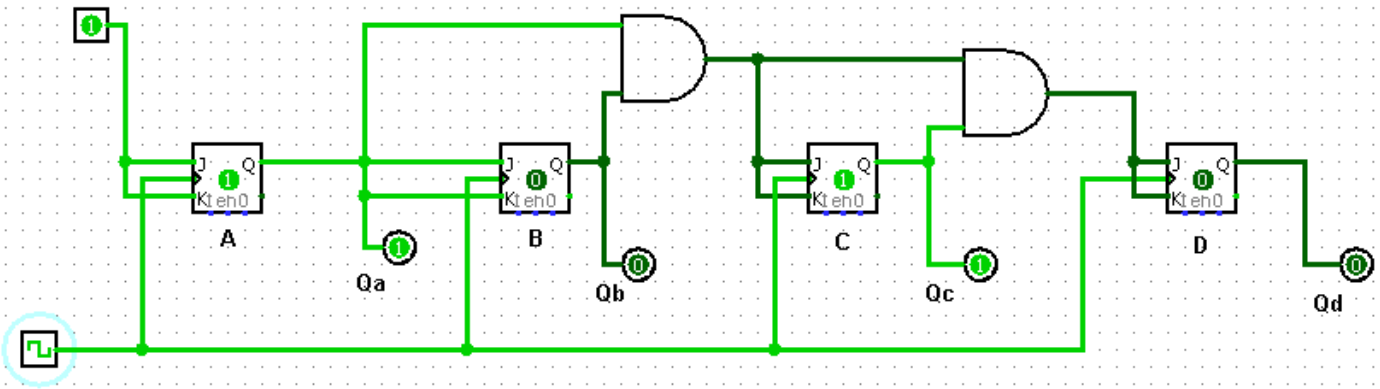

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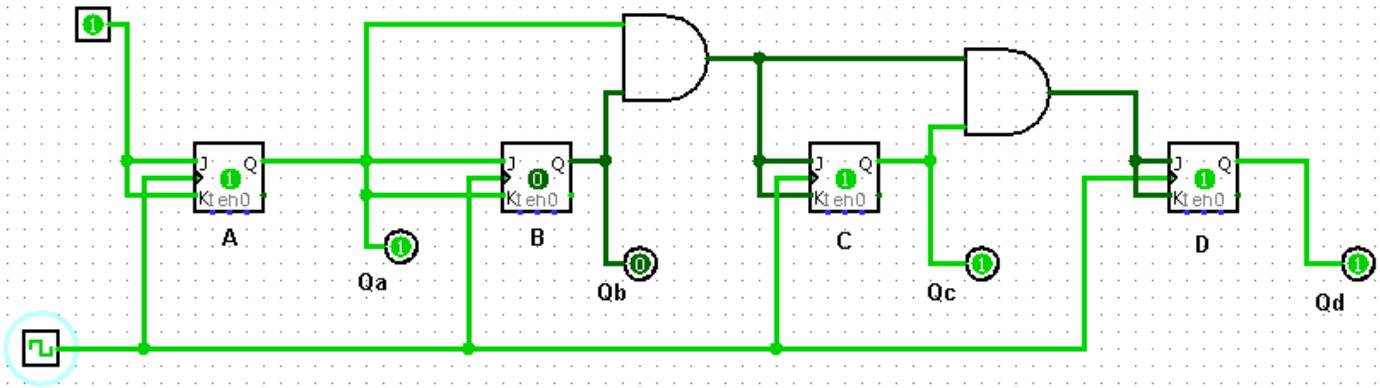

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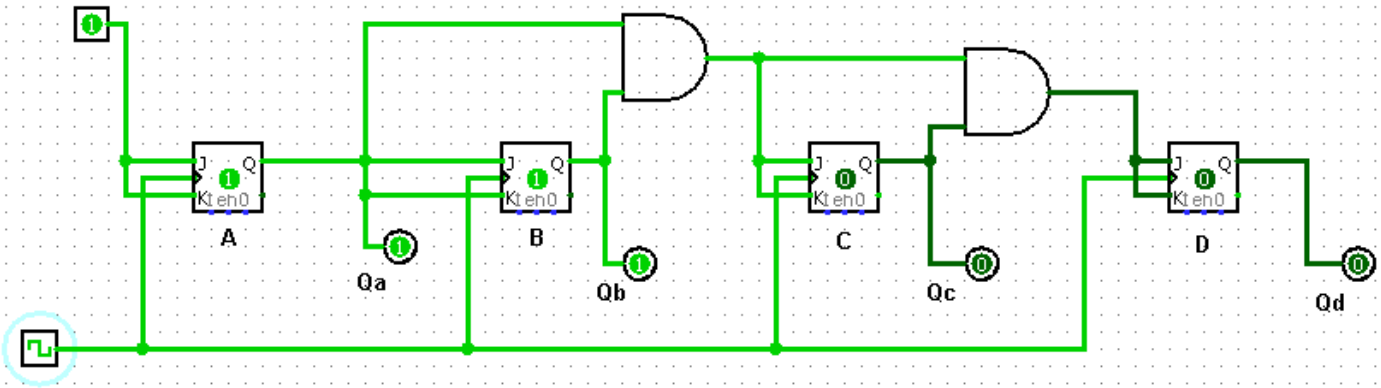

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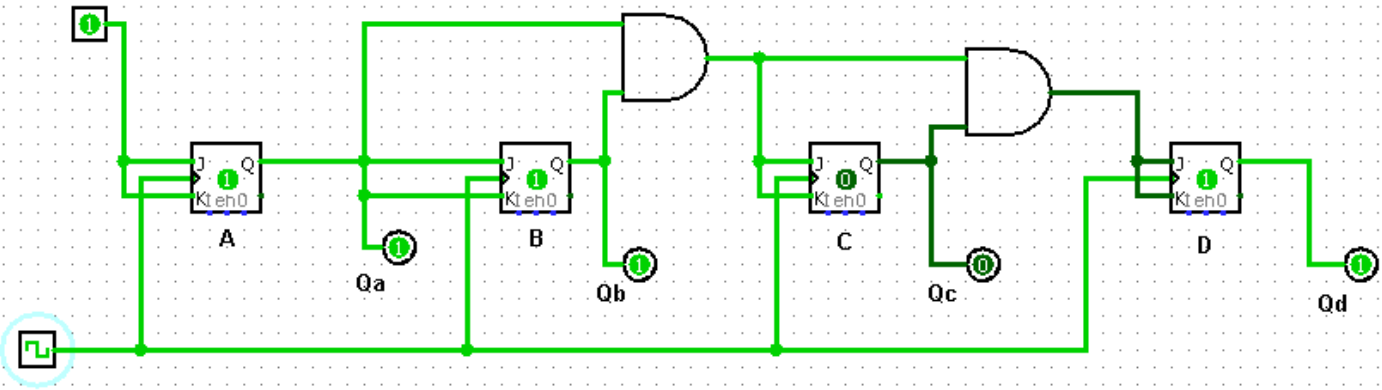

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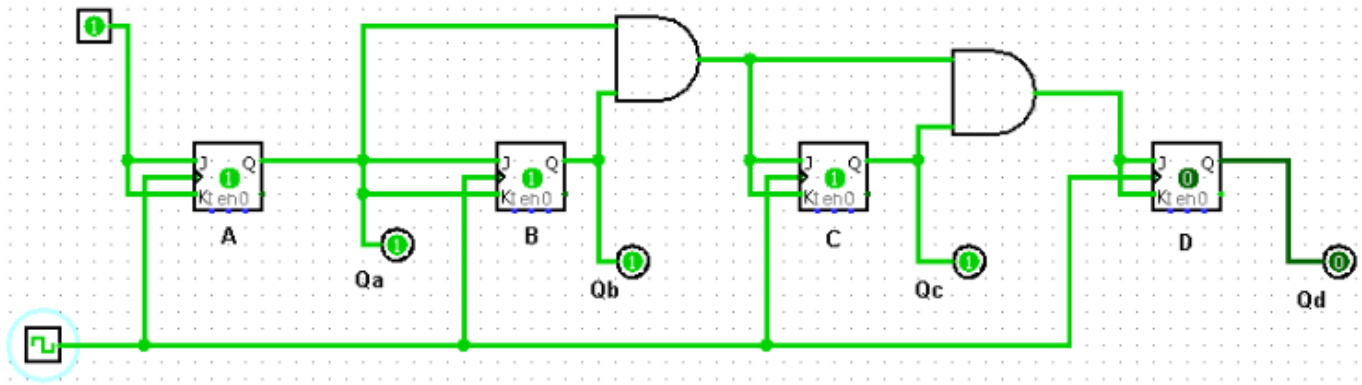

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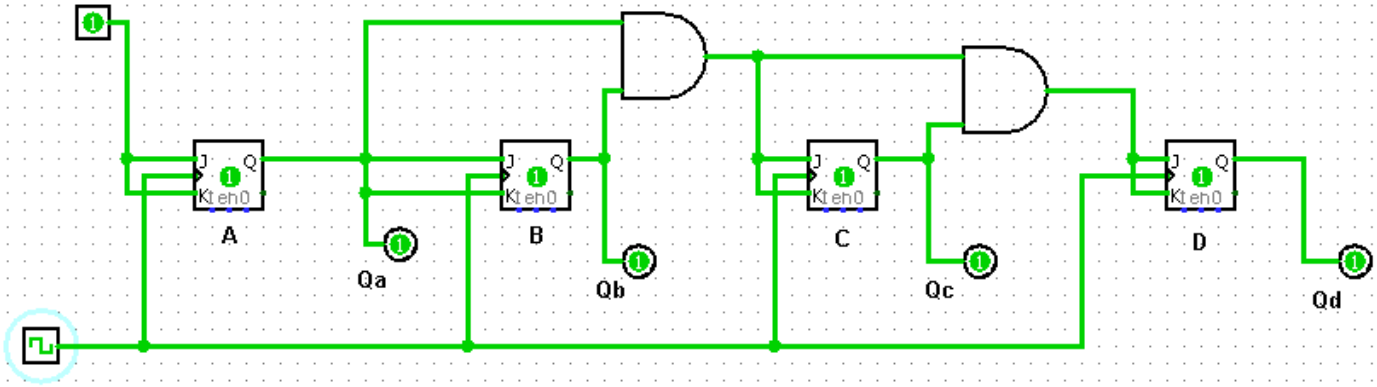
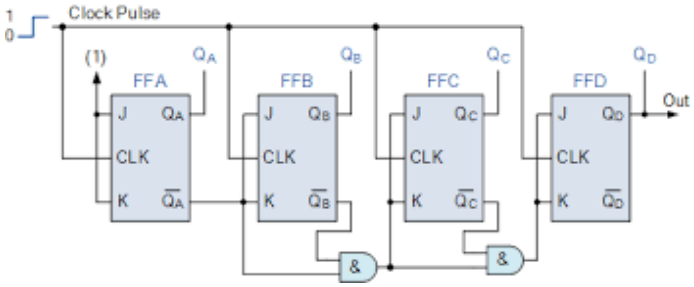


Student's observation and conclusion:

- **Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counter are used in digital electronics for counting purpose, they can count specific event happening in the circuit.**
- **The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.**
- **Synchronous Counters are so called because the clock input of all the individual flip-flops within the counter are all clocked together at the same time by the same clock signal.**

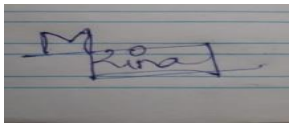


- **MOD Counters are cascaded counter circuits which count to a set modulus value before resetting. The job of a counter is to count by advancing the contents of the counter by one count with each clock pulse.**
- **In this experiment we have use four JK flip flop for the mod counter.**

Name: L. Mrinal Raj

Reg. No.: 201900339

Digital Signature:



Date:21/10/20