Date: 9/2/21

Expno: 2

Name: Convertion of flipflops

(i) (JK)ff to (D)ff

(ii) (JK)ff to (T)ff

(iii) (D)ff to (JK)ff

(iv) (D)ff to (T)ff

Required material:

(i) J-K flip flop (IC 7473/ IC 7476)
(ii) D flip flop (IC 74LS74)
(iii) or gate (IC 7432)
(iv) and gate (IC 7408)
(v) wiring to connect

Theory:

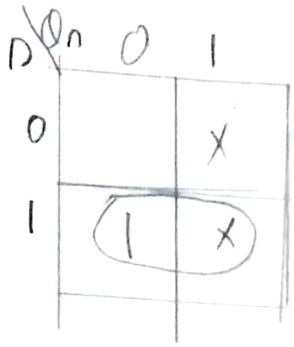
flipflop is a basic storage element used to storage of data
A single flipflop can store one bit (0 or 1) of data.
They are effected by clock which acts as a lock, they are effected by positive edge or negtive edge.
Most commonly used flip flop are JK so to meet our requirments it's needed to learn about their conversion.

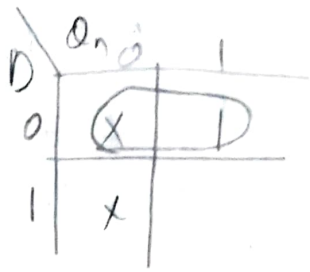
(i) JK flip flop to D flip flop

(i) Construct characteristic of D table & excitation table of JK flip flop:

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

(ii) Using K-map to find J & K expressions to D:

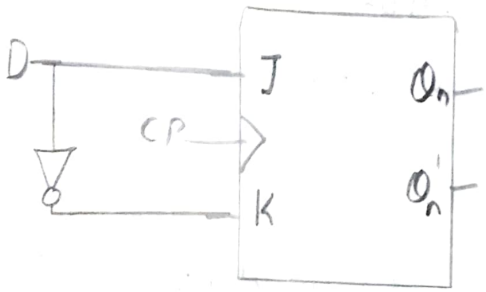




$J = D$

$K = D'$

(iii)

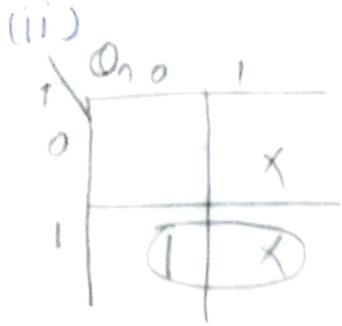


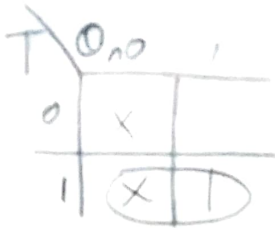
(2) JK flip flop to T flipflop:

(i) Construction of charactertable of T-flipflop & J-K flipflop

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

(ii)

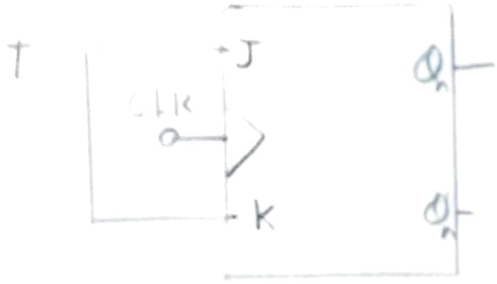




$J = T$

$K = T$

(iii) design of circuit:

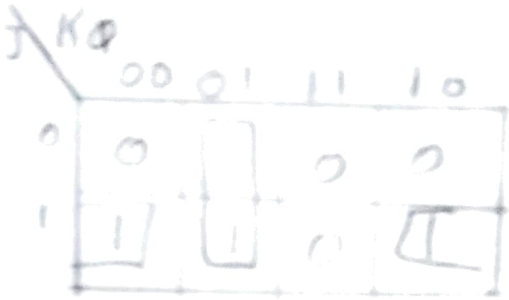


(3) D flip flop to JK flipflop:

(i) Construct characteristic table of JK & exitation table of D:

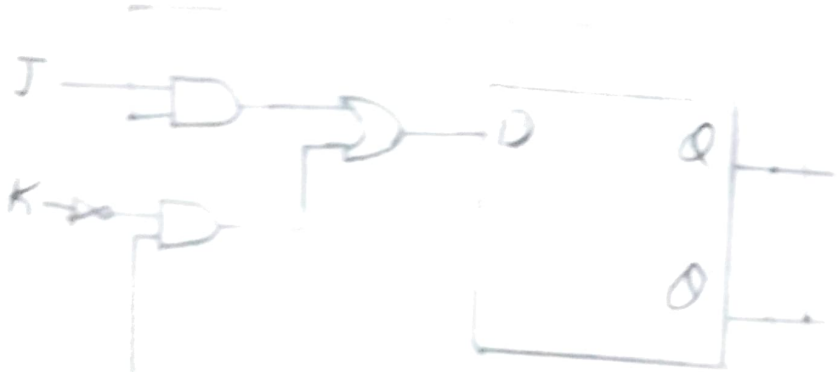
ff data inputs		outputs	Dff inputs
J	K	Q	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0
0	0	0	0
1	0	1	1

(2) K-map for JK FF



$$D = J\bar{Q} + \bar{K}Q$$

(3) Circuit:

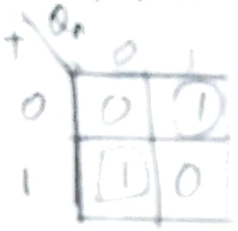


(IV) D flip flop to T flip flop:

(i) excitation table of D flip flop & T flip flop truth table

T input (T)	Present state (Q n)	next state (Q n+1)	D input (D)
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

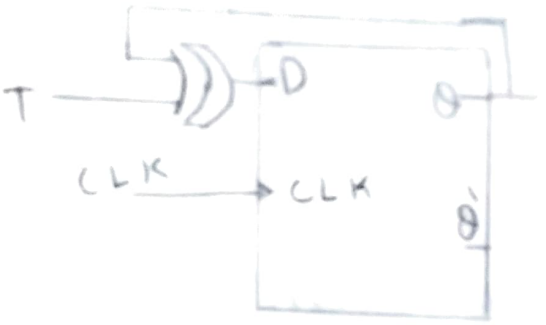
(ii) K map of Q_n & T



$D = T\bar{Q}_n + \bar{T}Q_n$

$= T \oplus Q_n$

(iii) Circuit diagram



Conclusion & observation:

(I) JK flip flop to D flip flop:

(i) The final output circuit behaves as D flip flop but contains only JK flip flop

(ii) D - flip flop is called data flip flop

(iii) D flip flops are widly used in building block of RAM & Registers for ~~Comp~~ Central processing unit

(iv) Only one input D is taking & outputs Q & $\bar{Q}$

(II) JK flip flop to T flip flop:

(i) The final circuit behaves as T-flip flop but contains JK flip flop

(ii) T-flip flop is also called toggle flip flop

(iii) These flip flops are ~~co~~ used in counter designing

(iv) Only one input T & 2 outputs which are toggle Q & $\bar{Q}$

(III) D flip flop to J K flip flop.

1) In this case the final circuit works as J K flip flop with but inside we have D flip flop.

2) JK flip flop is the most commonly used flip flop.

3) Its used in frequency divider circuit & mostly used in designing counters for both Async & Synchronous counter.

(IV) D Flip flop to T flip flop.

(i) The final circuit behaves like T flip flop but contains D flip flop

(ii) Its called Toggle ff flip flop

(iii) They have only one input T & output is Q & Q'

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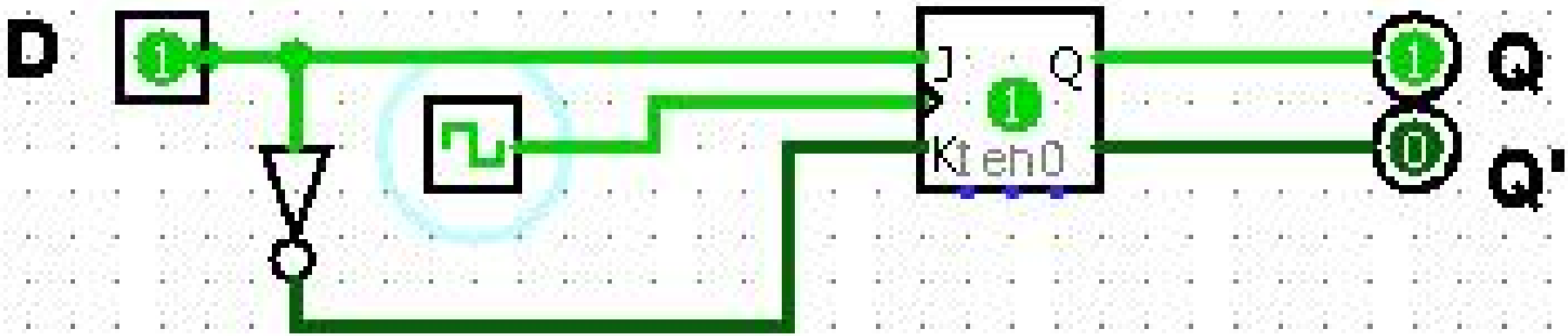
jk to d flip flop



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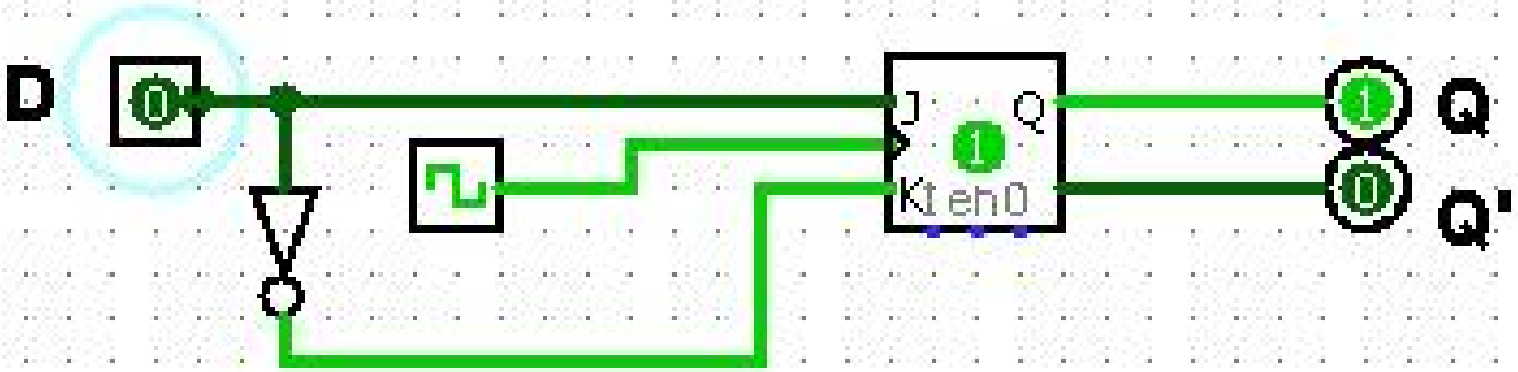
jk to d flip flop



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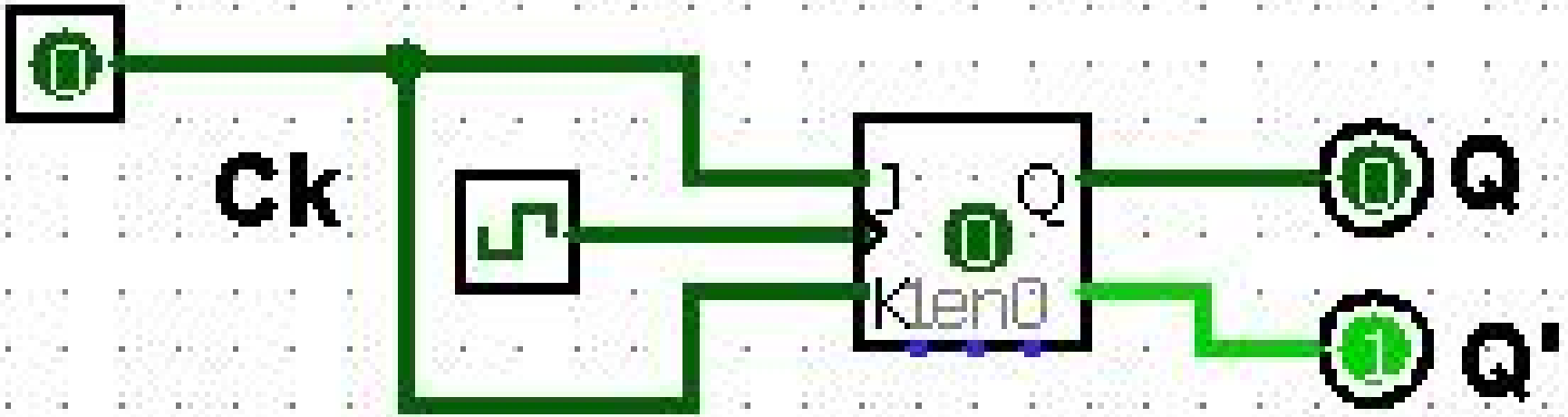
jk to T flip flop



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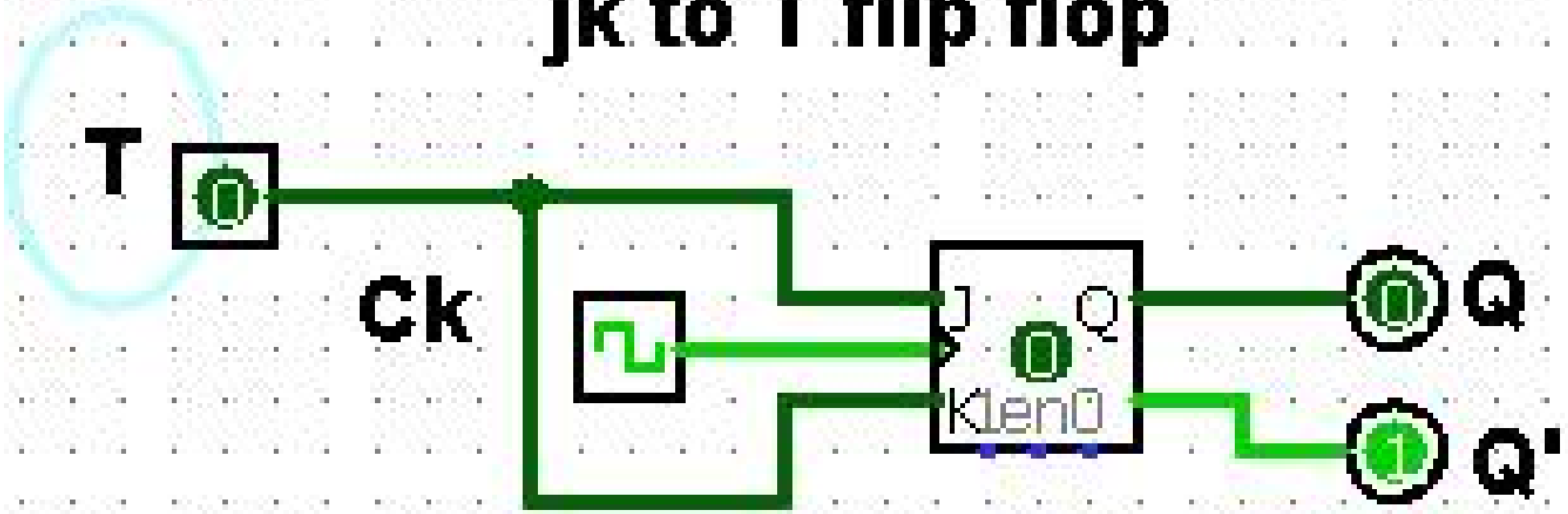
jk to T flip flop



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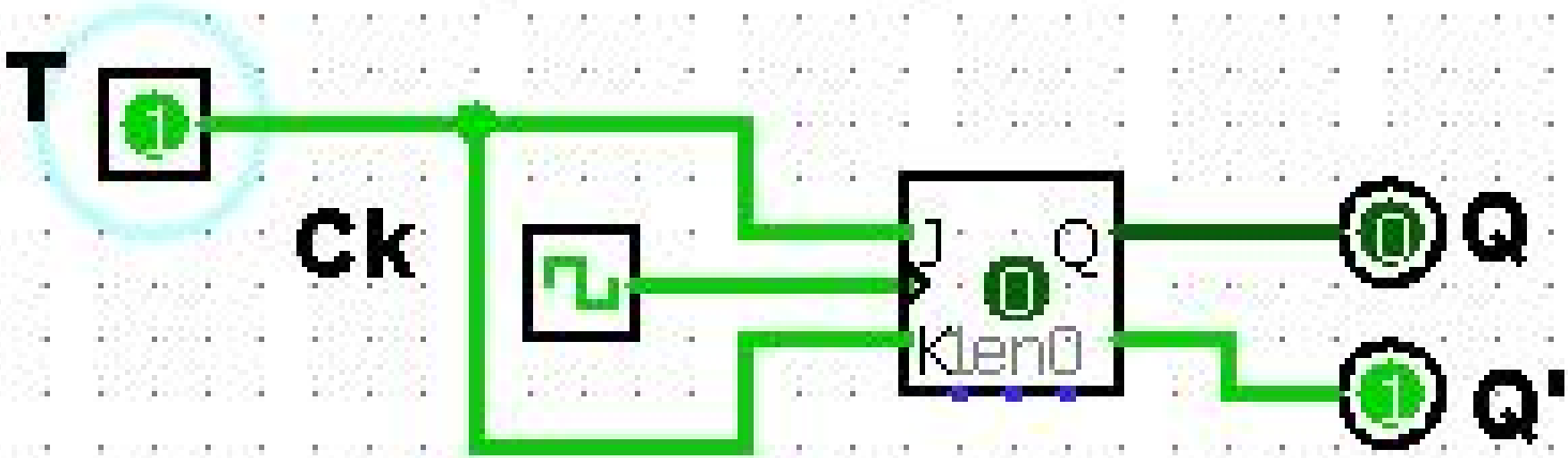
jk to T flip flop



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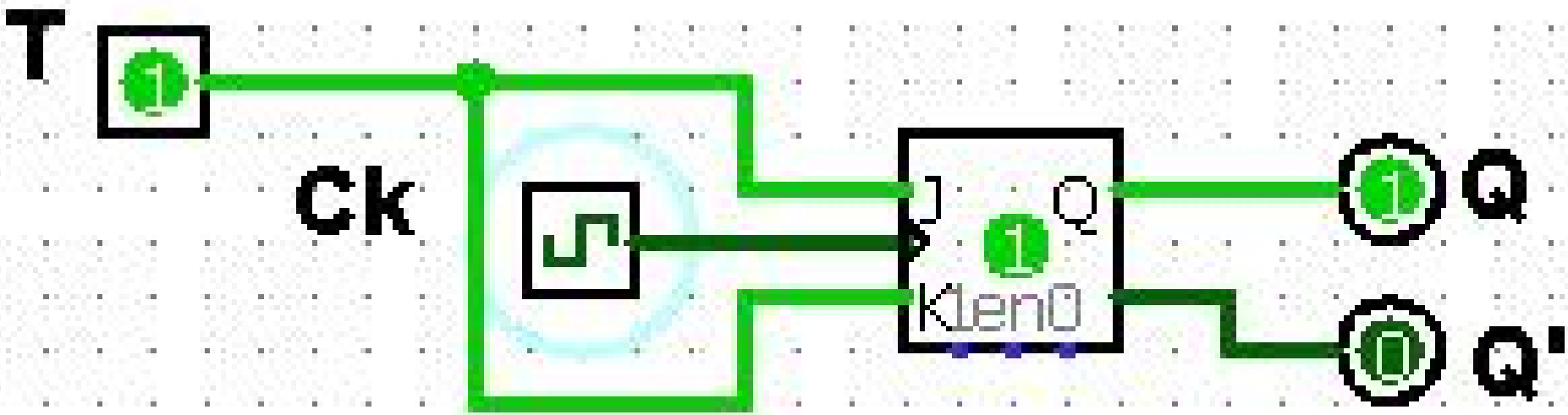
jk to T flip flop



D to JK FF

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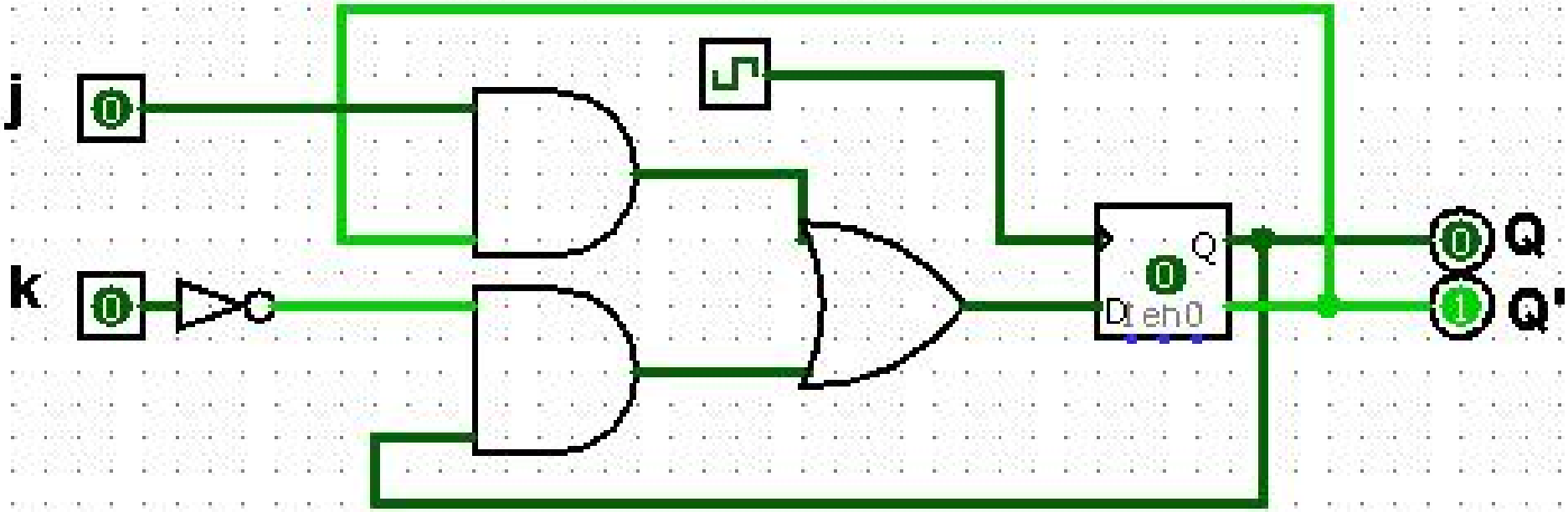

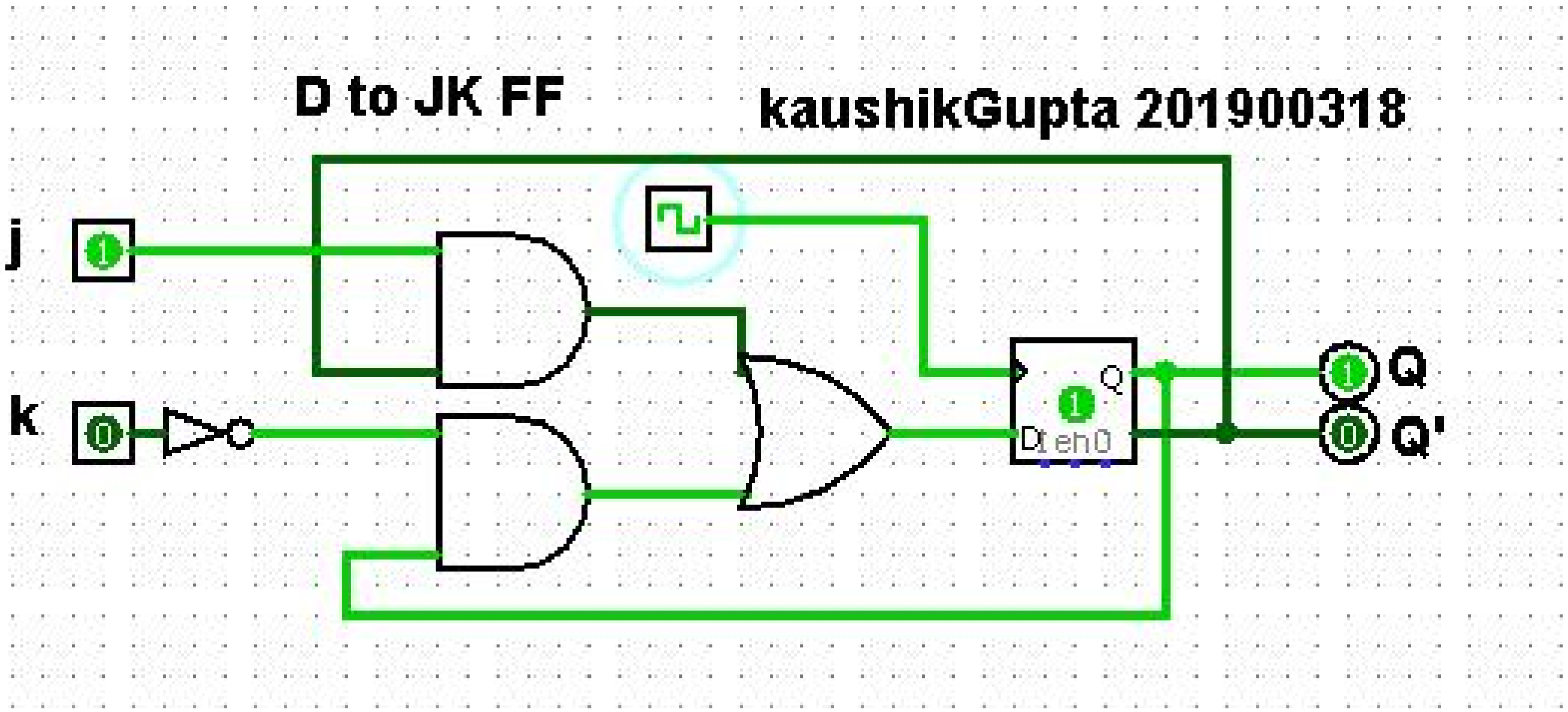
D to JK FF
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j
k
1
0
Q
D
en
Q
Q'

D to JK FF

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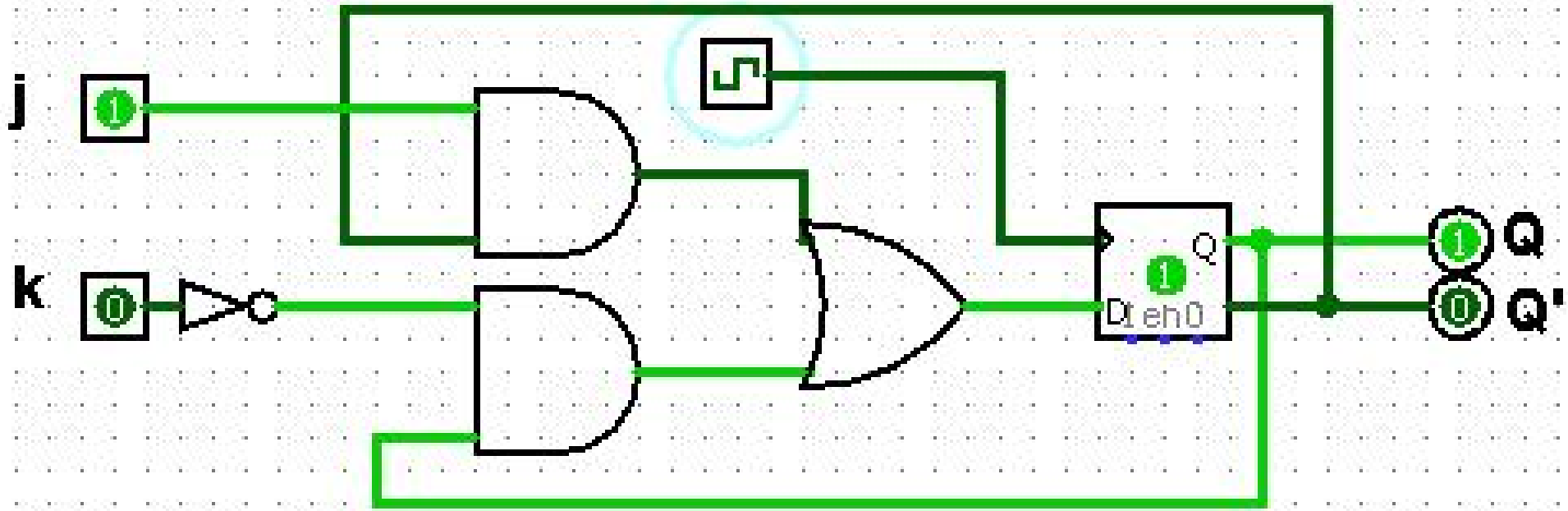

D to JK FF

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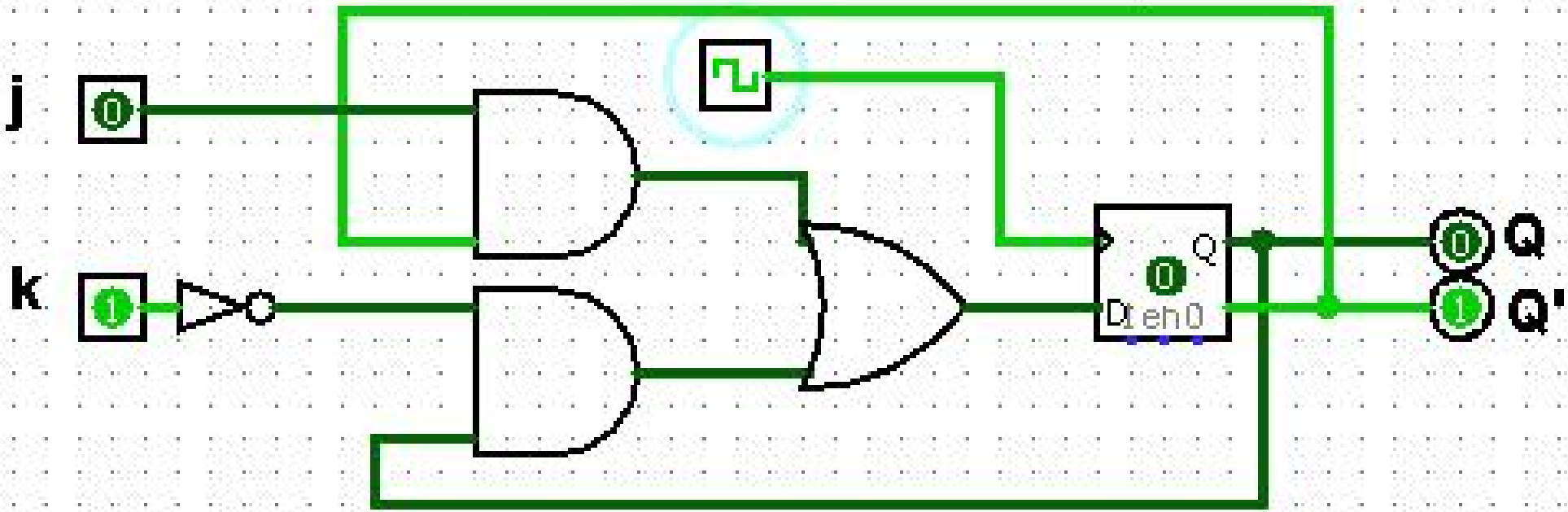

D to JK FF

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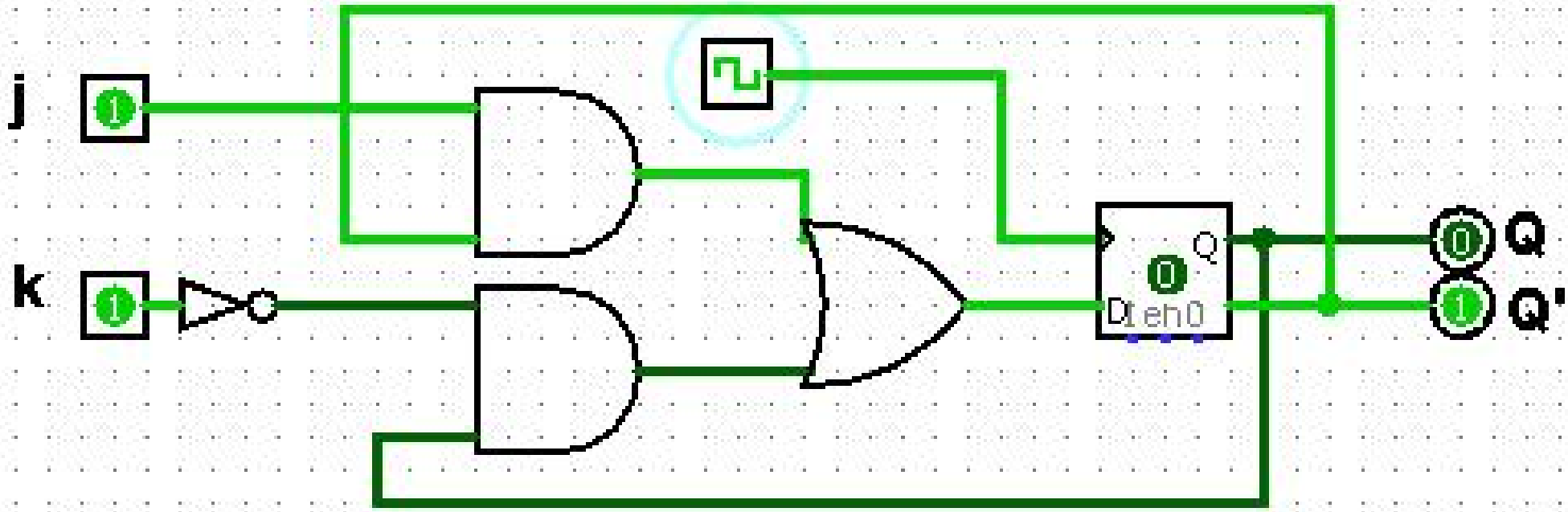

D to JK FF

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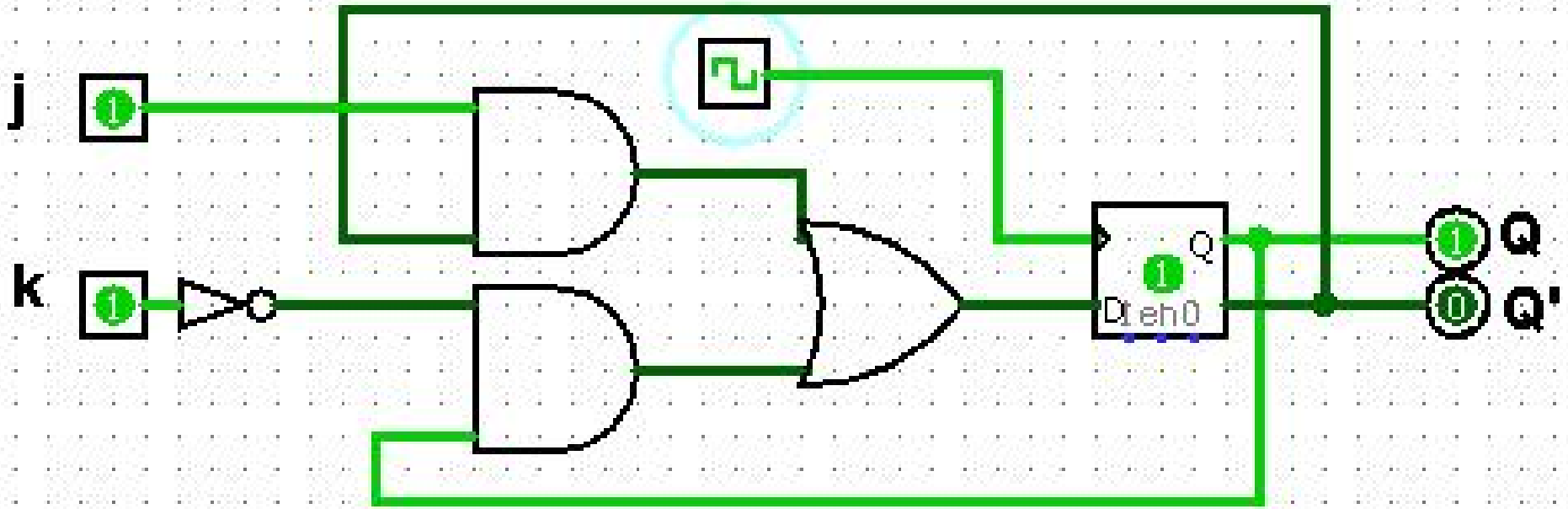

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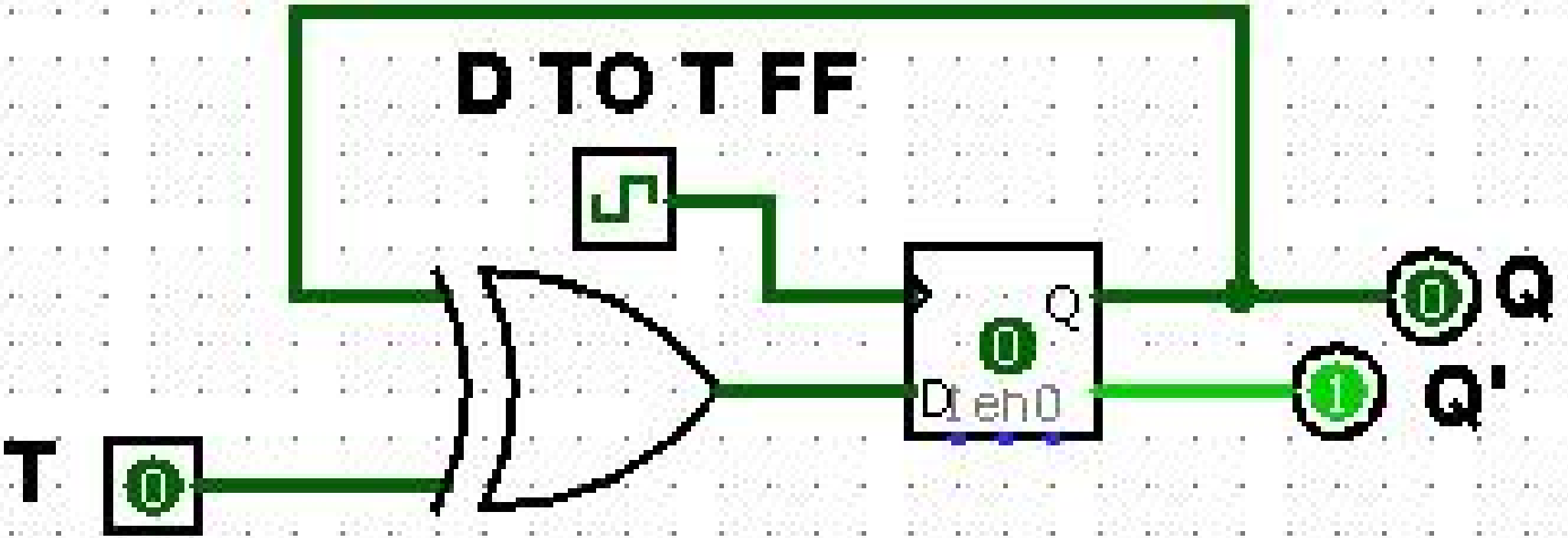

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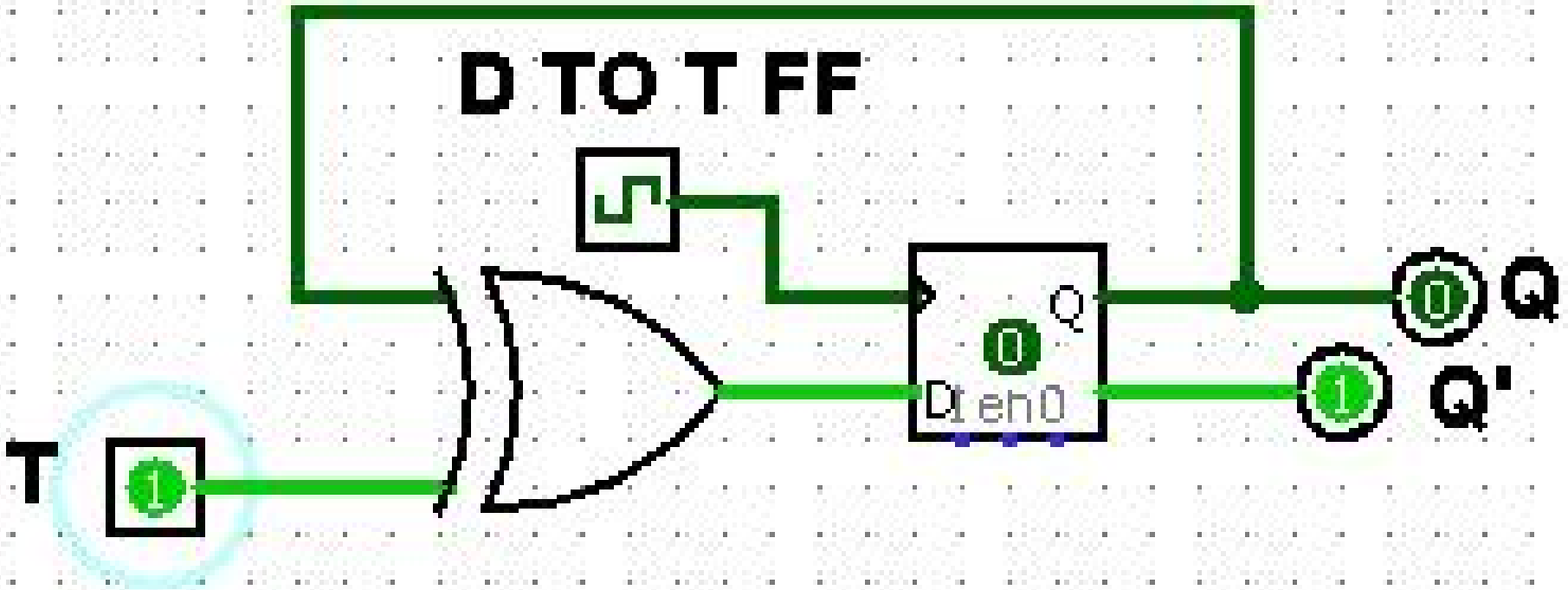

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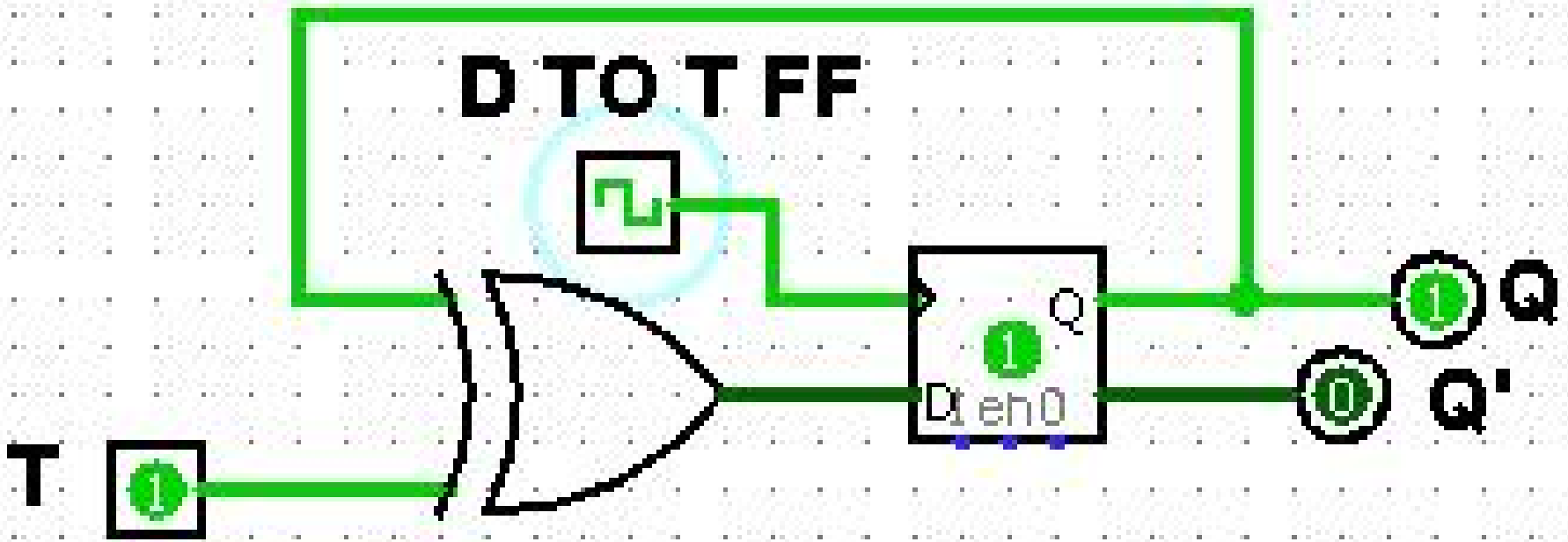

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