

**PSM**

Generate  
Verilog

**Template  
Script**

Generate  
TCL

**Functional Code:**

tx\_chain.v  
rx\_chain.v  
subsystem.v  
timing\_controler.v  
...

**Custom  
Script:**  
model.tcl

**Platform Specific  
Modules:**

usrp\_std.v  
ddc.v  
tx\_buffer.v  
adc\_interface.v

**Binary:**  
model.rbf