Dhirubhai Ambani Institute of Information and Communication Technology

EL203: Embedded Hardware Design

Field Programmable Gate Array (FPGA)

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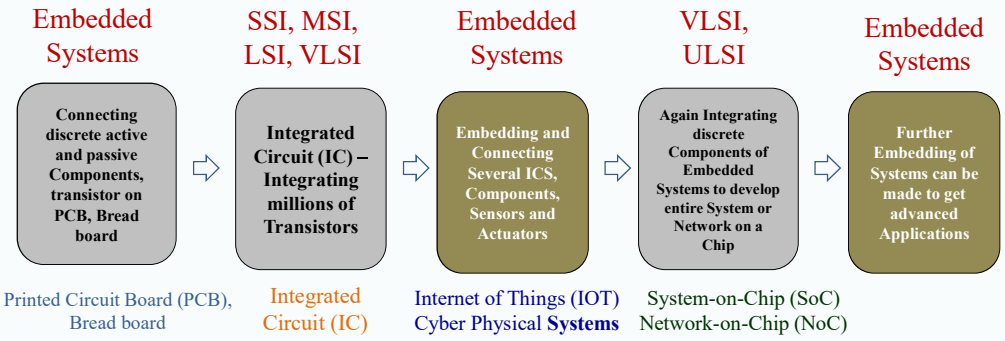
Introduction

Hardware Modeling Devices/Platform

- Bread board
- Printed Circuit Board
- Microprocessor and Microcontrollers (8051, ATMega, ARM…)
- Development Boards -- Arduino, Rapberry Pi, etc.
- Programmable Devices (PROM, PAL, PLA, CPLD, FPGA)
- Application Specific Integrated Circuit

VLSI and Embedded Systems….

Technology Advancement and Need of advanced **Applications…**



Why FPGA…?

Field Programmable Gate Array (FPGA)

A field-programmable gate array (FPGA) is a logic device that contains a two-dimensional array of generic logic cells and programmable switches.

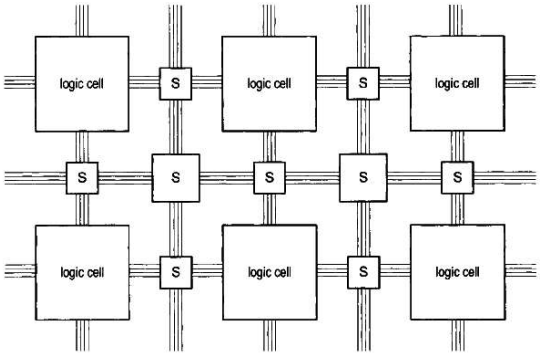


Fig: Conceptual structure of an FPGA device.

Package Marking

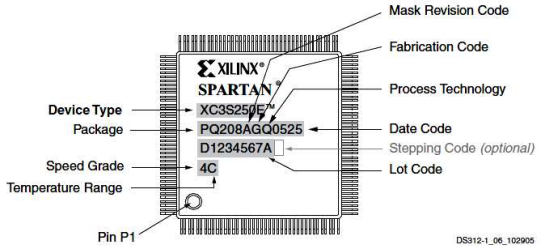


Fig: Spartan-3E QFP Package Marking Example.

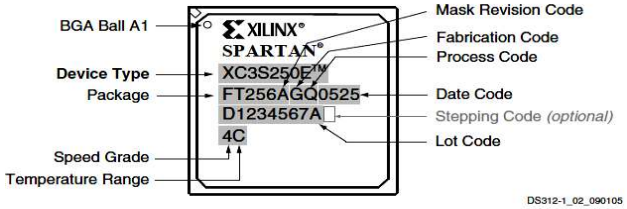
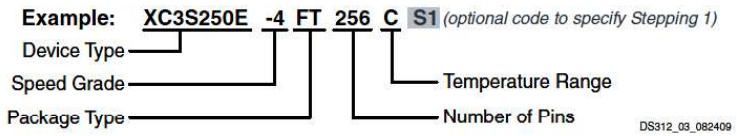


Fig: Spartan-3E BGA Package Marking Example.

Ordering Information



Device	Speed Grade	Package Type / Number of Pins		Temperature Range (T_J)
XC3S100E	-4 Standard Performance	VQ100 VQG100	100-pin Very Thin Quad Flat Pack (VQFP)	C Commercial (0°C to 85°C)
XC3S250E	-5 High Performance(1)	CP132 CPG132	132-ball Chip-Scale Package (CSP)	I Industrial (–40°C to 100°C)
XC3S500E(2)		TQ144 TQG144	144-pin Thin Quad Flat Pack (TQFP)	
XC3S1200E		PQ208 PQG208	208-pin Plastic Quad Flat Pack (PQFP)	
XC3S1600E		FT256 FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	
		FG320 FGG320	320-ball Fine-Pitch Ball Grid Array (FBGA)	
		FG400 FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)	
		FG484 FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)	

Spartan 3E Architecture Overview

Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)**
- **Input/Output Blocks (IOBs)**
- **Block RAM**
- **Multiple Blocks**
- **Digital Clock Manager (DCM) Blocks**

Spartan 3E Architecture Overview

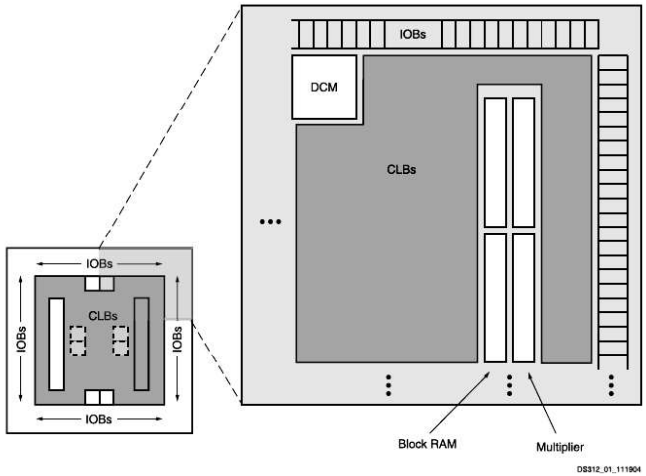


Fig: Spartan-3E Family Architecture.

IOBs Organized into Banks

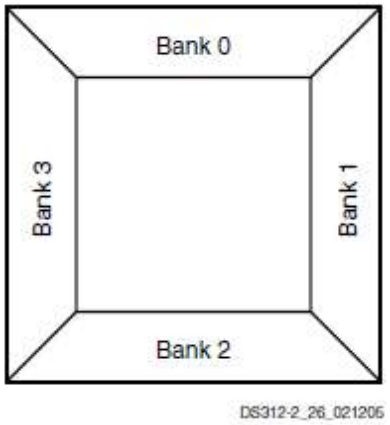


Fig: Spartan-3E I/O Banks (top view).

Configurable Logic Block (CLB) and Slice Resources

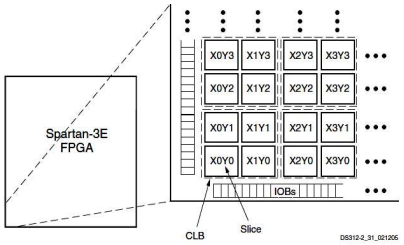


Fig: CLB Locations.

Table: Spartan-3E CLB Resources

Device	CLB Rows	CLB Columns	CLB Total(1)	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360
XC3S250E	34	26	612	2,448	4,896	5,508	2,448	39,168
XC3S500E	46	34	1,164	4,656	9,312	10,476	4,656	74,496
XC3S1200E	60	46	2,168	8,672	17,344	19,512	8,672	138,752
XC3S1600E	76	58	3,688	14,752	29,504	33,192	14,752	236,032

Summary of Spartan-3E FPGA Attributes

Table: Spartan-3E FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Slice Overview

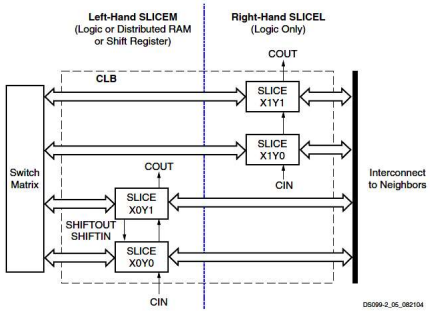


Fig: Arrangement of Slices within the CLB.

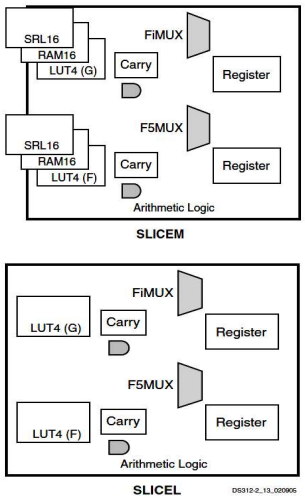


Fig: Resources in Slice.

Digital Clock Managers (DCMs)

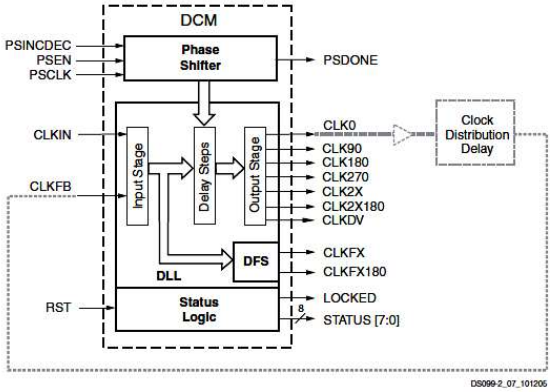


Fig: DCM Functional Blocks and Associated Signals.

Clocking Infrastructure

Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA.
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge.
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge.

Clocking Infrastructure

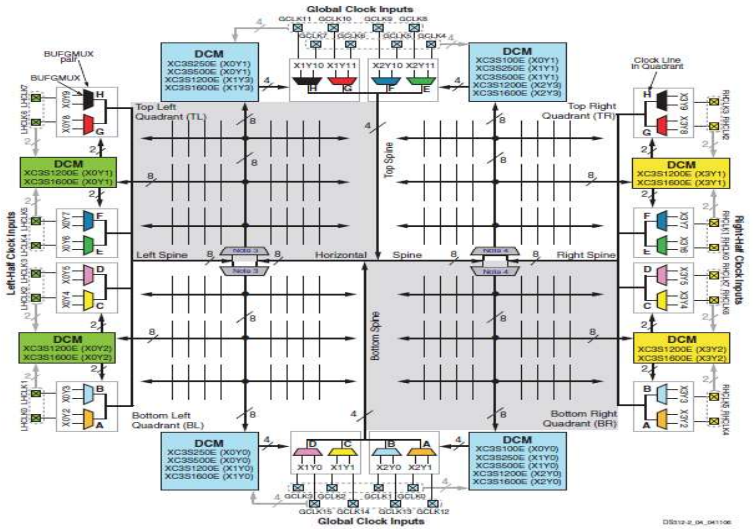
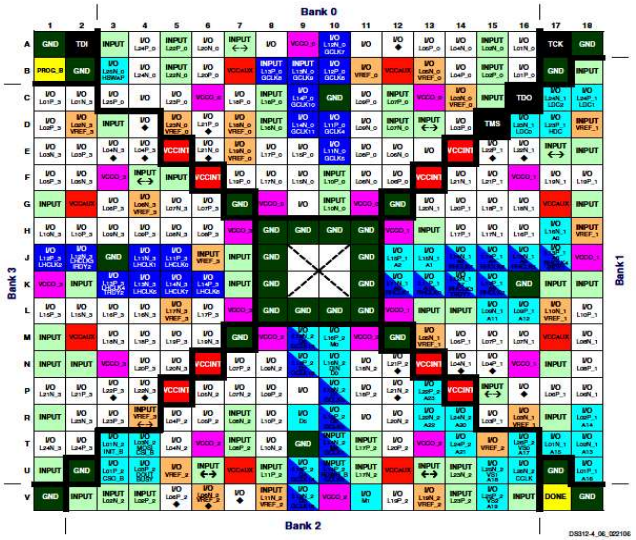


Fig: Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View).

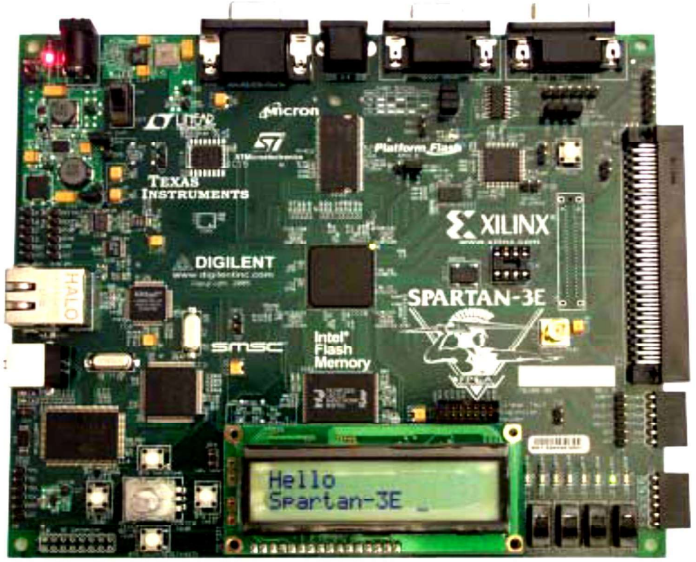
FG320: 320-ball Fine-Pitch Ball Grid Array



102-120	**I/O:** Unrestricted, general-purpose user I/O
47-48	**INPUT:** Unrestricted, general-purpose input pin
2	**CONFIG:** Dedicated configuration pins
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).
46	**DUAL:** Configuration pin, then possible user-I/O
16	**CLK:** User I/O, input, or global buffer input
4	**JTAG:** Dedicated JTAG port pins
28	**GND:** Ground
20-21	**VREF:** User I/O or input voltage reference for bank
20	**VCCO:** Output voltage supply for bank
8	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Fig: FT320 Package Footprint (top view).

Spartan 3E FPGA Board



Spartan 3E Features/Specifications

The key features of the Spartan-3E Starter Kit board are:

- Xilinx XC3S500E Spartan-3E FPGA
- Xilinx 64-macrocell XC2C64A CoolRunner™ CPLD

- Up to 232 user-I/O pins
- 320-pin FBGA package
- Over 10,000 logic cells

- Xilinx 4 Mbit Platform Flash configuration PROM
- 64 MByte (512 Mbit) of DDR SDRAM, x16 data interface, 100+ MHz
- 16 MByte (128 Mbit) of parallel NOR Flash (Intel StrataFlash)
- FPGA configuration storage
- MicroBlaze code storage/shadowing
- 16 Mbits of SPI serial Flash (STMicro)
- FPGA configuration storage

Spartan 3E Features/Specifications

The key features of the Spartan-3E Starter Kit board are:

- 2-line, 16-character LCD screen
- Eight discrete LEDs

- PS/2 mouse or keyboard port
- VGA display port
- 10/100 Ethernet PHY (requires Ethernet MAC in FPGA)
- Two 9-pin RS-232 ports (DTE- and DCE-style)
- On-board USB-based FPGA/CPLD download/debug interface
- Three Digilent 6-pin expansion connectors
- Hirose FX2 expansion connector
- SHA-1 1-wire serial EEPROM for bitstream copy protection

- 50 MHz clock oscillator
- SMA clock input
- 8-pin DIP socket for auxiliary clock oscillator

Spartan 3E Features/Specifications

The key features of the Spartan-3E Starter Kit board are:

- Four-output, SPI-based Digital-to-Analog Converter (DAC)
- Two-input, SPI-based Analog-to-Digital Converter (ADC) with programmable-gain pre-amplifier

- ChipScope™ SoftTouch debugging port
- Rotary-encoder with push-button shaft
- Four slide switches
- Four push-button switches

- Rotary-encoder with push-button shaft
- Four slide switches
- Four push-button switches

Components/Parts of different Company assembled in Spartan 3E board

- Linear Technology for the SPI-compatible A/D and D/A converters, the programmable pre-amplifier, and the power regulators for the non-FPGA Components
- Intel Corporation for the 128 Mbit StrataFlash memory
- Micron Technology, Inc. for the 32M x 16 DDR SDRAM
- SMSC for the 10/100 Ethernet PHY
- STMicroelectronics for the 16M x 1 SPI serial Flash PROM
- Texas Instruments Incorporated for the three-rail TPS75003 regulator supplying most of the FPGA supply voltages
- Xilinx, Inc. Configuration Solutions Division for the XCF04S Platform Flash PROM and their support for the embedded USB programmer
- Xilinx, Inc. for the XC2C64A CoolRunner™-II CPLD

I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards

Spartan-3E FPGAs support the following single-ended standards:
- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, 66 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:
- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

I/O Capabilities

Table: Single-Ended IOSTANDARD Bank Compatibility

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility					Input Requirements	
	1.2V	1.5V	1.8V	2.5V	3.3V	V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	-	-	-	-	Input/ Output	N/R(1)	N/R
LVCMOS33	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS25	-	-	-	Input/ Output	Input	N/R	N/R
LVCMOS18	-	-	Input/ Output	Input	Input	N/R	N/R
LVCMOS15	-	Input/ Output	Input	Input	Input	N/R	N/R
LVCMOS12	Input/ Output	Input	Input	Input	Input	N/R	N/R
PCI33_3	-	-	-	-	Input/ Output	N/R	N/R
PCI66_3	-	-	-	-	Input/ Output	N/R	N/R
HSTL_I_18	-	-	Input/ Output	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/ Output	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/ Output	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/ Output	Input	1.25	1.25

Slew Rate Control

Slew Rate

Each IOB has a slew-rate control that sets the output switching edge-rate for LVCMOS and LVTTL outputs.

The SLEW attribute controls the slew rate and can either be set to SLOW (default) or FAST.

Drive Strength

Drive Strength

Each LVCMOS and LVTTL output additionally supports up to six different drive current strengths as shown in Table.

Table: Programmable Output Drive Current

IOSTANDARD	Output Drive Current (mA)					
	2	4	6	8	12	16
LVTTL	✔	✔	✔	✔	✔	✔
LVCMOS33	✔	✔	✔	✔	✔	✔
LVCMOS25	✔	✔	✔	✔	✔	-
LVCMOS18	✔	✔	✔	✔	-	-
LVCMOS15	✔	✔	✔	-	-	-
LVCMOS12	✔	-	-	-	-	-

Drive Strength

- Each LVCMOS & LVTTL output additionally support upto **Six different drive current** strength.
- The drive attribute is set to desired drive strength: **2, 4, 6, 8, 12, 16**.
- Unless and otherwise mentioned, **default for LVCMOS and LVTTL** is drive strength **12mA** and **Slow Slew rate**.
- **High output current drive strength and Fast O/P Slew rate** generally result in **fastest I/O performance**.

Switches/Buttons

On Board Switches on Spartan 3E Board

There are three types of on-board switches:

- **Slide Switch (4 Nos.)**
- **Push Button Switch (4 Nos.)**
- **Rotary Push Button Switch (1 No.)**

On Board Switches - Switch, Buttons and Knob

Slide Switches

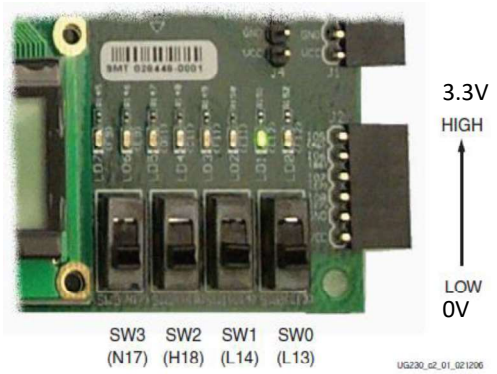


Fig: Four Slide Switches.

```
NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;
```

Fig: User Constraint File (UCF) for Slide Switches.

On Board Switches - Switch, Buttons and Knob

Push-Button Switches

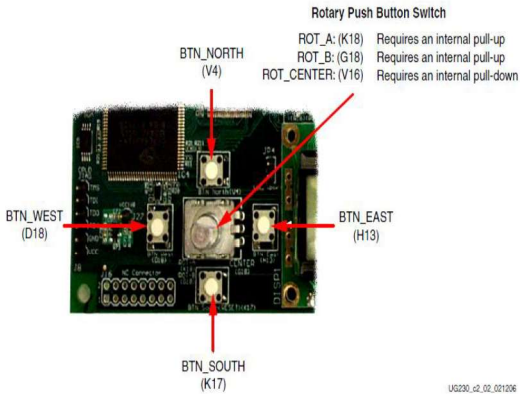


Fig: Four Push-Button switches surrounded Rotary Push Button switch.

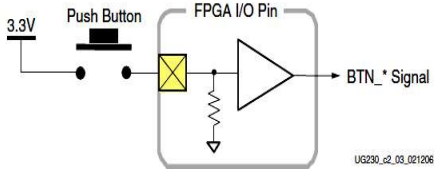


Fig: Push-Button requires an internal Pull-Down resistor in FPGA Input pin.

```
NET "BTN_EAST"  LOC = "H13" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_NORTH" LOC = "V4"  | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_SOUTH" LOC = "K17" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_WEST"  LOC = "D18" | IOSTANDARD = LVTTL | PULLDOWN ;
```

Fig: User Constraint File (UCF) for Push-Button switches.

On Board Switches - Switch, Buttons and Knob

Rotary Push-Button Switch

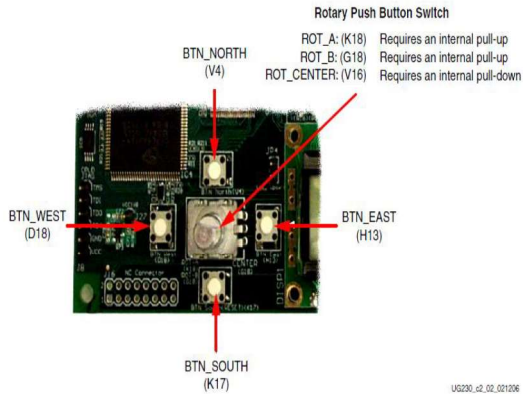


Fig: Rotary Push Button switch at the center of Four Push-Button switches.

The Rotary Push-Button Switch integrates two different function:

- **Rotating shaft produces values whenever the shaft turns.**
- **Push-button switch**

The Rotary Push-Button Switch produces three outputs:

Two Shaft encoder outputs

- **ROT_A**
- **ROT_B**

The center push-button switch output

- **ROT_CENTER**

Rotary Push-Button Switch

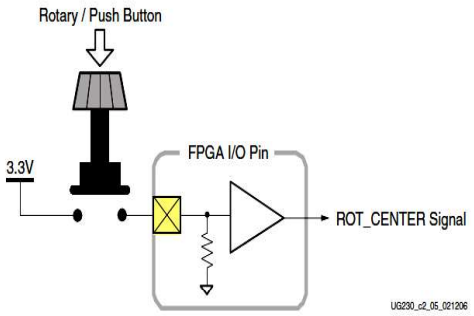


Fig: Push-Button circuitry in Rotary Push-Button switch.

Rotary Switch-Button when **Not Pressed**

ROT_CENTER = Logic '0' (0V)

Rotary Switch-Button when **Pressed**

ROT_CENTER = Logic '1' (3.3V)

Active Pull-down resistor is used for Push button operation

Rotary Push-Button Switch

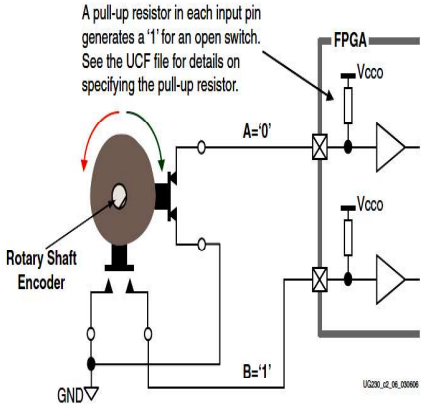


Fig: Rotary shaft encoder circuitry in Rotary Push-Button switch.

Switch Closed = Logic '0'

Switch Open = Logic '1'

Rotary Push-Button Switch when **Not rotating (Detent), both switch closed**

ROT_A= Logic '0'
ROT_B= Logic '0'

Rotary Push-Button Switch when **rotating Right, Switch A opens while B closes**

ROT_A= Logic '0'
ROT_B = Logic '1'

Rotary Push-Button Switch when **rotating Left, Switch A closes while B opens**

ROT_A= Logic 1'
ROT_B = Logic '0'

Active Pull-up resistor is used for Rotary operation

Rotary Push-Button Switch

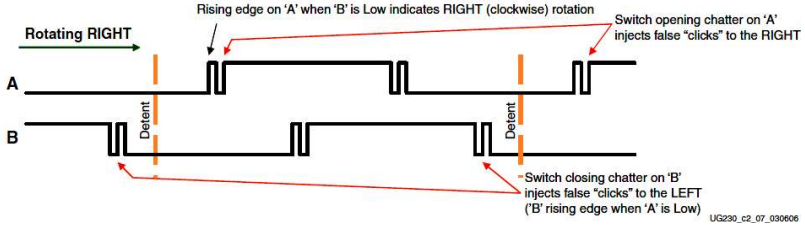


Fig: Outputs from Rotary Shaft Encoder may include Mechanical Chatter.

```
NET "ROT_A"      LOC = "K18" | IOSTANDARD = LVTTL | PULLUP   ;
NET "ROT_B"      LOC = "G18" | IOSTANDARD = LVTTL | PULLUP   ;
NET "ROT_CENTER" LOC = "V16" | IOSTANDARD = LVTTL | PULLDOWN ;
```

Fig: UCF constraints for Rotary Push-button Switch.

On-board Displays

On Board Displays on Spartan 3E Board

There are two types of on-board displays:

- **LED (8 Nos.)**
- **LCD (1 No.)**

On Board Display – LEDs

LEDS

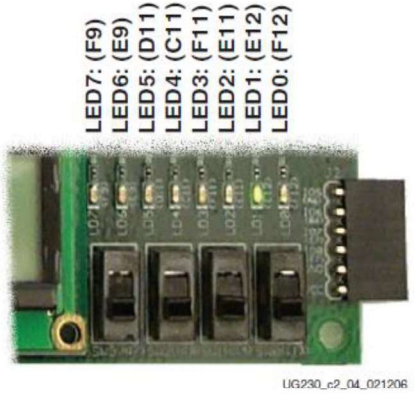


Fig: Eight Discrete LEDs.

```
NET "LED<7>" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
```

Fig: UCF constraints for Eight Discrete LEDs.

On Board Display – LEDs

Liquid Crystal Display (LCD)

- **The Spartan-3E FPGA Starter Kit features a 16x2 LCD with 5x8 pixel matrix (per character).**
- **The character is represented as the ASCII value.**

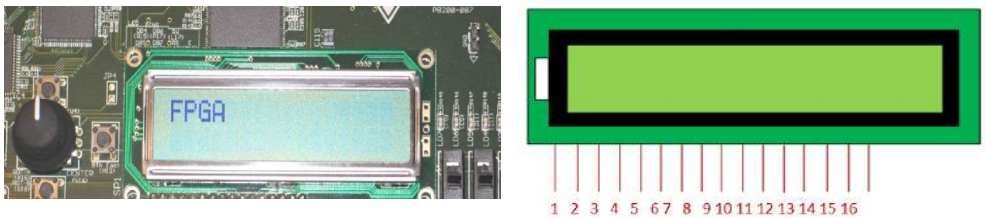


Fig: Liquid Crystal Display (LCD).

On Board Display – LCD

I. FPGA—LCD Interface

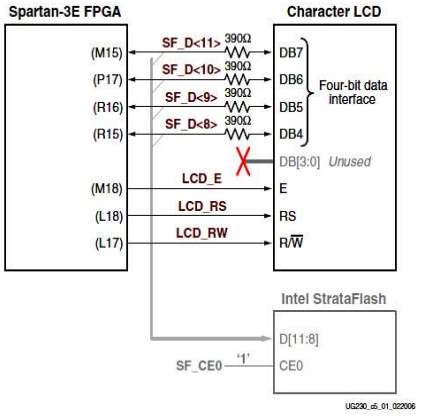


Fig: FPGA—LCD Interface.

Table: Character LCD Interface Signal

Signal Name	FPGA Pin	Function	
SF_D<11>	M15	Data bit DB7	Shared with StrataFlash pins SF_D<11:8>
SF_D<10>	P17	Data bit DB6	
SF_D<9>	R16	Data bit DB5	
SF_D<8>	R15	Data bit DB4	
LCD_E	M18	Read/Write Enable Pulse 0: Disabled 1: Read/Write operation enabled	
LCD_RS	L18	Register Select 0: Instruction register during write operations. Busy Flash during read operations 1: Data for read or write operations	
LCD_RW	L17	Read/Write Control 0: WRITE, LCD accepts data 1: READ, LCD presents data	

1st 2nd 3rd

II. LCD UCF

```
NET "LCD_E"   LOC = "M18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RS"  LOC = "L18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RW"  LOC = "L17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# The LCD four-bit data interface is shared with the StrataFlash.
NET "SF_D<8>"  LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<9>"  LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<10>" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<11>" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
```

Fig: UCF constraints for the Character LCD.

Clock

The Spartan-3E FPGA Board supports three primary clock input sources:

- **50 MHz On-Board Oscillator**
- **SMA Clock Input or Output connector**
- **Auxiliary Clock Oscillator Socket**

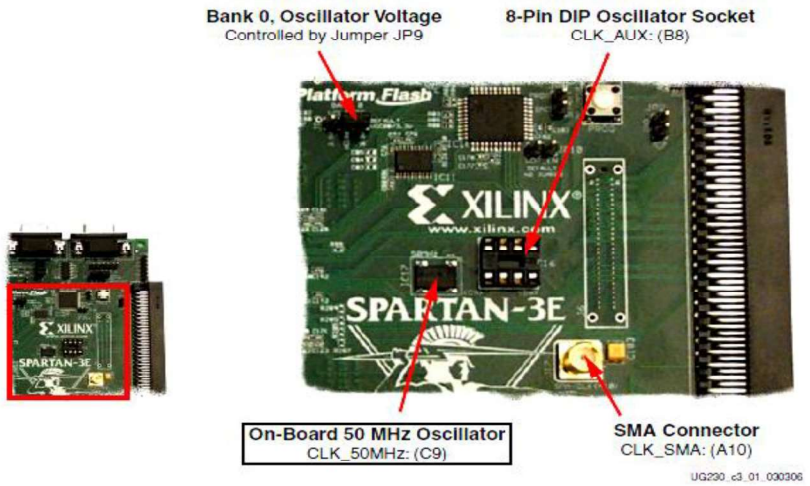


Fig: Available Clock Inputs.

- **50 MHz On-Board Oscillator**
  - The board includes a **50 MHz oscillator** with a **40% to 60% output duty cycle**.
  - The oscillator is accurate to **±2500 Hz or ±50 ppm**.
- **SMA Clock Input or Output connector**
  - Clocks can be supplied off-board via an **SMA-style connector**.
  - The **FPGA can also generate a single-ended clock output** or other high-speed signal on the SMA clock connector for an external device.
- **Auxiliary Clock Oscillator Socket**
  - The provided **8-pin socket** accepts clock oscillators that fit the **8-pin DIP footprint**.
  - Use this socket if the FPGA application requires a frequency **other than 50 MHz**.
  - Alternatively, use the FPGA's **Digital Clock Manager (DCM)** to generate or synthesize other frequencies from the on-board 50 MHz oscillator.

Clock Connections

- **Each of the clock inputs** connect directly to a **global buffer input in I/O Bank 0, along the top of the FPGA**.
- As shown in Table below, each of the **clock inputs also optimally connects to an associated DCM**.

Table: Clock Inputs and Associated Global Buffers and DCM

Clock Input	FPGA Pin	Global Buffer	Associated DCM
CLK_50MHZ	C9	GCLK10	DCM_X0Y1
CLK_AUX	B8	GCLK8	DCM_X0Y1
CLK_SMA	A10	GCLK7	DCM_X1Y1

UCF Constraints

The clock input sources require two different types of constraints:

1) **The location constraints define the I/O pin assignments and I/O standards.**
   - UCF constraints for the three clock input sources, including the I/O pin assignment and the I/O standard used. The settings assume that jumper JP9 is set for 3.3V.
   - If JP9 is set for 2.5V, adjust the IOSTANDARD settings accordingly.

```
NET "CLK_50MHZ" LOC = "C9"  | IOSTANDARD = LVCMOS33 ;
NET "CLK_SMA"   LOC = "A10" | IOSTANDARD = LVCMOS33 ;
NET "CLK_AUX"   LOC = "B8"  | IOSTANDARD = LVCMOS33 ;
```

Fig: UCF constraints for Clock Sources.

UCF Constraints

The clock input sources require two different types of constraints:

2) **The period constraints define the clock period—and consequently the clock frequency—and the duty cycle of the incoming clock signal.**
   - The Xilinx ISE® development software uses timing-driven logic placement and routing. Set the clock PERIOD constraint as appropriate.

```
# Define clock period for 50 MHz oscillator
NET "CLK_50MHZ" PERIOD = 20.0ns HIGH 40%;
```

Fig: UCF Clock Period Constraint.

On-board Clock Sources/Inputs

Voltage Control

- The voltage for all I/O pins in FPGA I/O Bank 0 is controlled by jumper JP9.

- Consequently, these clock resources are also controlled by jumper JP9.
  By default, JP9 is set for 3.3V. The on-board oscillator is a 3.3V device and might not perform as expected when jumper JP9 is set for 2.5V.

FPGA Configuration Options

FPGA Configuration Options

The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

Furthermore, Spartan-3E FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single parallel NOR Flash.
The FPGA application controls which configuration to load next and when to load it.

FPGA Configuration Options

Table: Spartan-3E Configuration Mode Options and Pin Settings

	Master Serial	SPI	BPI	Slave Parallel	Slave Serial	JTAG
M[2:0] mode pin settings	<0:0:0>	<0:0:1>	<0:1:0>=Up <0:1:1>=Down	<1:1:0>	<1:1:1>	<1:0:1>
Data width	Serial	Serial	Byte-wide	Byte-wide	Serial	Serial
Configuration memory source	Xilinx Platform Flash	Industry-standard SPI serial Flash	Industry-standard parallel NOR Flash or Xilinx parallel Platform Flash	Any source via microcontroller, CPU, Xilinx parallel Platform Flash, etc.	Any source via microcontroller, CPU, Xilinx Platform Flash, etc.	Any source via microcontroller, CPU, System ACE™ CF, etc.
Clock source	Internal oscillator	Internal oscillator	Internal oscillator	External clock on CCLK pin	External clock on CCLK pin	External clock on TCK pin
Total I/O pins borrowed during configuration	8	13	46	21	8	0
Configuration mode for downstream daisy-chained FPGAs	Slave Serial	Slave Serial	Slave Parallel	Slave Parallel or Memory Mapped	Slave Serial	JTAG
Stand-alone FPGA applications (no external download host)	✓	✓	✓	Possible using XCFxxP Platform Flash, which optionally generates CCLK	Possible using XCFxxP Platform Flash, which optionally generates CCLK	
Uses low-cost, industry-standard Flash		✓	✓			
Supports optional MultiBoot, multi-configuration mode			✓			

Configuration Bitstream Image Sizes

Table: Number of Bits to Program a Spartan-3E FPGA (Uncompressed Bitstreams)

Spartan-3E FPGA	Number of Configuration Bits
XC3S100E	581,344
XC3S250E	1,353,728
XC3S500E	2,270,208
XC3S1200E	3,841,184
XC3S1600E	5,969,696

FPGA Configuration Options

The Spartan®-3E FPGA Starter Kit board supports a variety of FPGA configuration options:

- Download FPGA designs directly to the Spartan-3E FPGA via JTAG, using the **onboard USB interface**. The on-board USB-JTAG logic also provides in-system programming for the on-board Platform Flash PROM and the Xilinx XC2C64A CPLD.
  SPI serial Flash and StrataFlash programming are performed separately.
- Program the on-board **4 Mbit Xilinx XCF04S serial Platform Flash PROM**, then configure the FPGA from the image stored in the Platform Flash PROM using Master Serial mode.
- Program the on-board **16 Mbit ST Microelectronics SPI serial Flash PROM**, then configure the FPGA from the image stored in the SPI serial Flash PROM using SPI mode.
- Program the on-board **128 Mbit Intel StrataFlash parallel NOR Flash PROM**, then configure the FPGA from the image stored in the Flash PROM using BPI Up or BPI Down configuration modes. Further, an FPGA application can dynamically load two different FPGA configurations using the Spartan-3E FPGA's MultiBoot mode. See the Spartan-3E data sheet (DS312) for additional details on the MultiBoot feature.

FPGA Configuration Options

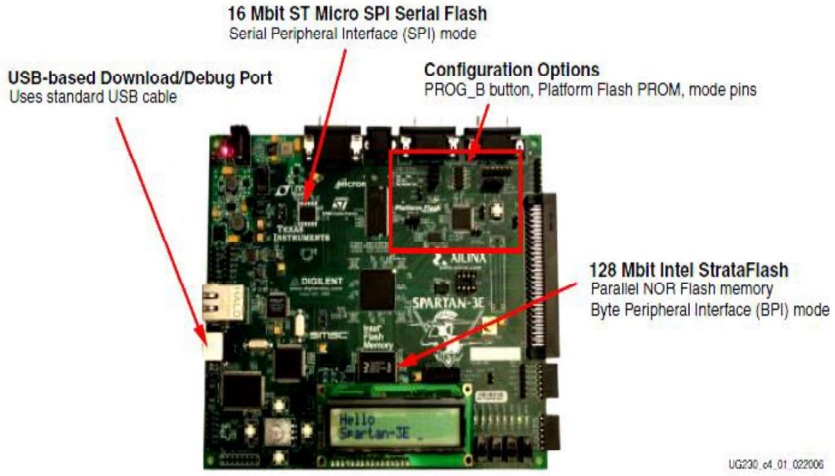


Fig: Spartan 3E FPGA Configuration Options.

FPGA Configuration Options

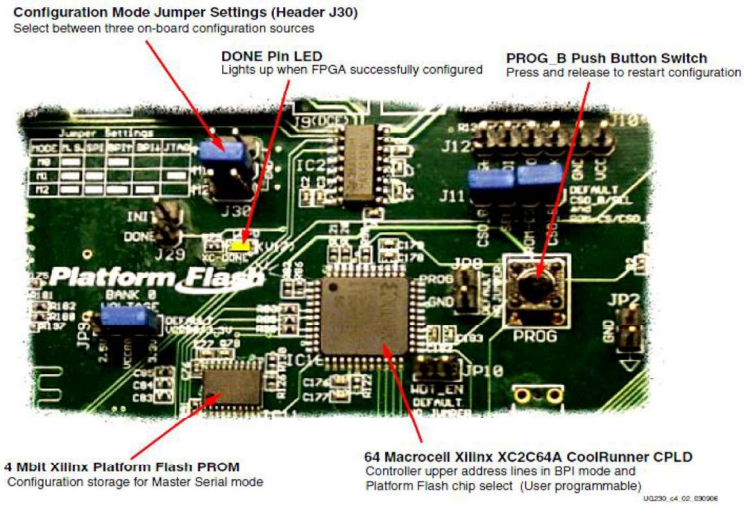


Fig: Detailed Configuration Options.

Configuration Mode Jumpers

Table: Spartan-3E Configuration Mode Jumper Settings (J30)

Configuration Mode	Mode Pins M2:M1:M0	FPGA Configuration Image Source	Jumper Settings
Master Serial	0:0:0	Platform Flash PROM	
SPI (see Chapter 12, "SPI Serial Flash")	1:1:0	SPI Serial Flash PROM starting at address 0	
BPI Up (see Chapter 11, "Intel StrataFlash Parallel NOR Flash PROM")	0:1:0	StrataFlash parallel Flash PROM, starting at address 0 and incrementing through address space. The CPLD controls address lines A[24:20] during BPI configuration.	
BPI Down (see Chapter 11, "Intel StrataFlash Parallel NOR Flash PROM")	0:1:1	StrataFlash parallel Flash PROM, starting at address 0x1FF_FFFF and decrementing through address space. The CPLD controls address lines A[24:20] during BPI configuration.	
JTAG	0:1:0	Downloaded from host via USB-JTAG port