EL203 Embedded Hardware Design

LAB_8

Aim: To implement an Embedded Processor with following specifications

Design a 3-stage and 16-bit embedded processor.

3-stages are Fetch, Decode and Execute.

Specifications for the processor to be designed:
1. Instruction Memory: 8 locations each of 16 bits.
2. Data Memory: 8 bytes (8 registers – each containing 8-bit data).
3. All instructions should be 16 bits.
4. All the instructions should be in ARM instruction format.
5. Instructions that the design should be able to execute:
   - ADD (i.e., ADD R0, R1, R2)
   - SUB (i.e., SUB R0, R1, R2)
   - AND (i.e., AND R0, R1, R2)
   - OR (i.e., OR R0, R1, R2)
   - NOT (i.e., NOT R0, R1)
   - B (unconditional branch) (i.e., B "PC Offset")
   - BZ (branch if Zero flag is set as HIGH) (i.e., BZ R1 "PC Offset")
   - LDR (load data in the register from the data memory)
     (i.e., LDR R0, [R1])
   - STR (store data in the data memory from the register)
   - (i.e., STR R0, [R1])

Example: ADD R0, R1, R2

Here R1 and R2 are source registers and they are of 8-bit data and R0 is the destination register where the result is stored.

Load Instruction

0000	R_D	XXXXXX	Reg Address
Opode [4 bits]	Destination Reg [3 bits]	Unused bit [6 bits]	Source Address [3 bit]

Store Instruction

0000	R_D	XXXXXX	Reg Address
OpCode [4 bits]	Source Reg [3 bits]	Unused bits [6 bits]	Storing Address [3 bit]

ADD

0010	XXX	R_D	R_{S1}	R_{S2}
OpCode [4 bits]	Unused bits [3 bits]	Destination Reg [3 bits]	Source Reg1 [3 bits]	Source Reg2 [3 bits]

SUB

0011	XXX	R_D	R_{S1}	R_{S2}
OpCode [4 bits]	Unused bits [3 bits]	Destination Reg [3 bits]	Source Reg1 [3 bits]	Source Reg2 [3 bits]

AND

0100	XXX	R_D	R_{S1}	R_{S2}
Opcode [4 bits]	Unused bits [3 bits]	Destination Reg [3 bits]	Source Reg1 [3 bits]	Source Reg2 [3 bits]

OR

0101	XXX	R_D	R_{S1}	R_{S2}
OpCode	Unused bits	Destination Reg	Source Reg1	Source Reg2
[4 bits]	[3 bits]	[3 bits]	[3 bits]	[3 bits]

NOT

0110	XXXXXX	R_D	R_S
OpCode	Unused bits	Destination Reg	Source Reg
[4 bits]	[6 bits]	[3 bits]	[3 bits]

Unconditional Branch

0111	XXXXXXXX	Sign of relative address	Address Offset
OpCode	Unused bits	Sign of relative address	Offset
[4 bits]	[8 bits]	[1 bit]	[3 bits]

Branch if zero

1000	XXXXX	Source Reg	Sign of relative address	Address Offset
OpCode	Unused bits	Source Reg	Sign of relative Address	Offset
[4 bits]	[5 bits]	[3 bits]	[1bit]	[3 bits]