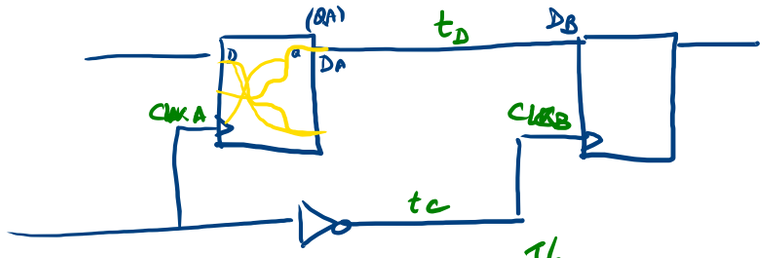
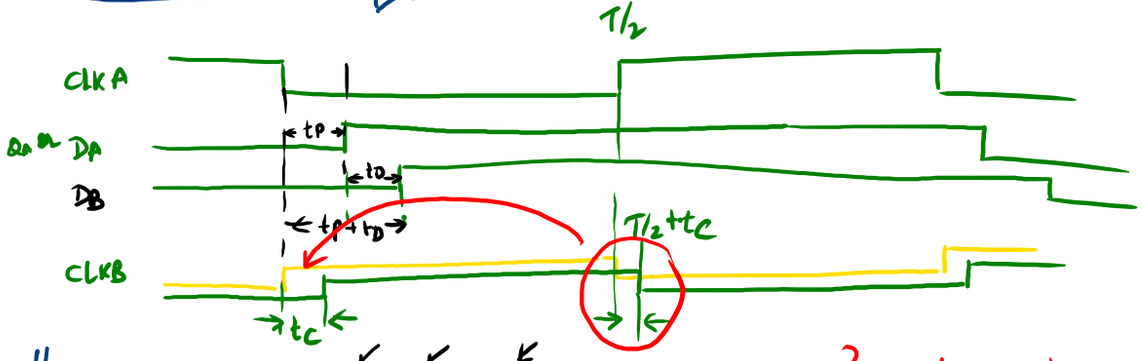
17. 01. 2024.

Ercegovac, Lang, Moreno

Timing Constraint:





Setup Requ.: $t_P + t_D + t_S < T/2 + t_C$

Hold Requ.: $\frac{T}{2} + t_C + t_H < T + t_P + t_D$

t_S & t_H are not equal

$t_P < 40ns$ $t_S = 10ns$ $t_H = 30ns$

$-10 < t_D - t_C < 10$

$\max(t_P + t_D) + t_S < \min(t_C + T/2)$

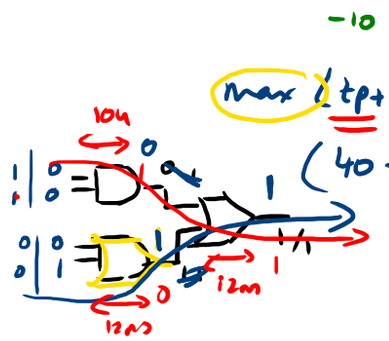
$(40 + 10 + 10)ns < T/2$

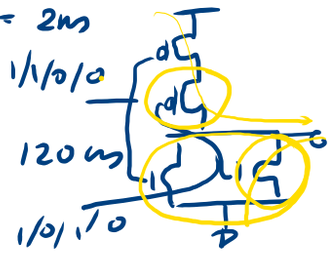
$T > 120ns$

$\frac{1}{120} \approx 8.3\,MHz$

30MHz Processor

$t_C = 2ns$





Asynchronous Bit Interfaces:

• Serial Port on PC –

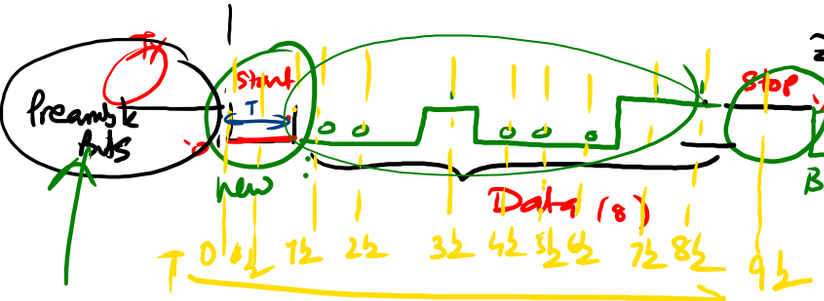
Start / Stop

Tx — Async — Rx

RS 232

Zero 'start'

One '1'



Bit cell duration is based on baud rate - bit rate -

9600 or 19200

$T = 52\,\mu s$