EL203 Embedded Hardware Design

LAB_5

Aim: To perform different Tasks using Verilog HDL.

1. An embedded system requires a clock pulse. For the same, generate a clock pulse signal whose time period is 10 ps using always block

2. For an embedded system having a clock pulse (clk) of 10ns. Using this, implement clk/2 and clk/4 signals.

3. Implement a counter that counts from 0 to 127 using while, for, repeat, forever loops; get output waveform and also display these in the output console window.

4. In a 32 bit number, count the number of zeros using while and for loops.