EL203 Embedded Hardware Design

LAB_6

Aim: To perform different Tasks using Verilog HDL.

1. (i) Design D Flip-flop
   (a) With synchronous reset
   (b) With asynchronous reset and preset with reset having highest priority

   (ii) Write a test-bench to check functionality of the module in 1(i).

2. Generate clka, clkb, clkc pulses as shown in Fig. 1 using behavioral modeling (without using delay assignments).

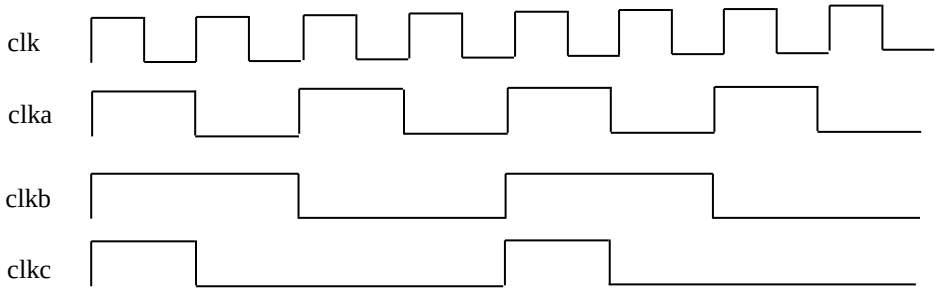

Fig. 1. Clock signals.