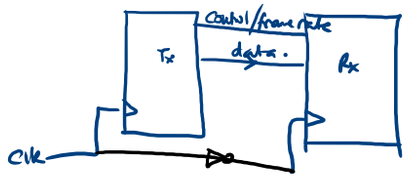
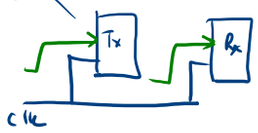
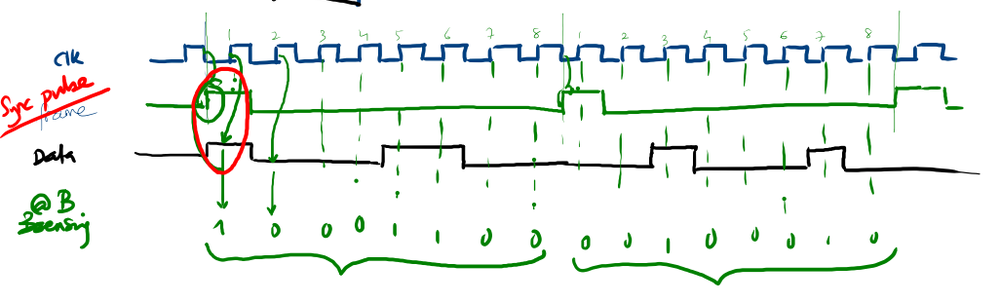
15.01.2024

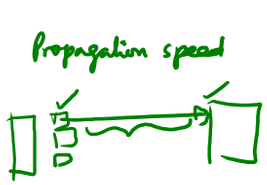
Interfaces/Interfacing :
- Synchronous
- (A)synchronous

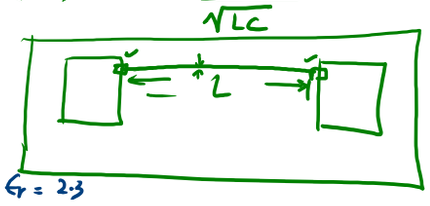


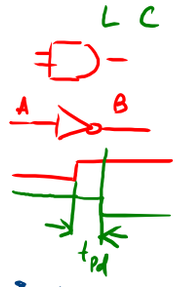




Propagation speed $(LC)^{-1/2}$ or $\frac{1}{\sqrt{LC}}$







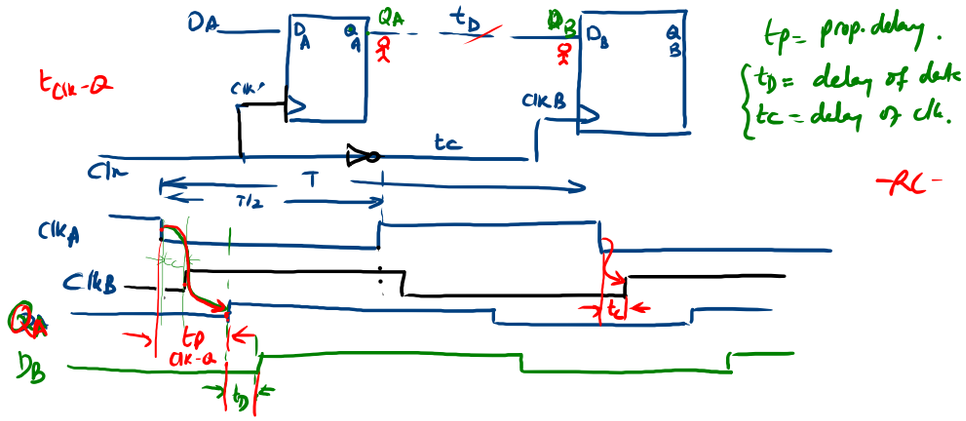
Coaxial cable :

$C \times \epsilon_r^{-1/2}$ cm/ns = ~ 20cm/ns

PCB. $1.4C \times (1+\epsilon_r)^{-1/2}$ cm/ns ~ 17cm/ns

$\epsilon_r = 5$

3×10^8 m/s = 30cm/ns



t_p = prop. delay.
- t_D = delay of data
- t_c = delay of clk.

RC-

Setup & Hold terms :-

Setup Time - Data must reach its stable value/new value at least (t_s) <Setup time> before the clk edge ($\downarrow$)

Hold time → Data must be held constant (stable) for at least (t_h) (hold time) after the clk edge

Ercegovac, Lang, Moreno.