Kaushik Vada

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Education

University of California, Riverside Riverside, CA

Bachelor of Science in Electrical Engineering | University of California Regents Distinguished Scholar *Aug 2023–May 2027*

GPA: 3.93/4.00

Relevant Coursework: Introduction to VLSI, Data Structures and Algorithms, Design and Architecture of Computer Systems, Computer Architecture, Machine Organization and Assembly Language, Digital Logic Design, Signals and Systems, Circuit Analysis, Introduction to Communication Systems

Qualifications

Student in electrical engineering with VLSI focus with experience in **Verilog/SystemVerilog** RTL design and verification, FPGA prototyping with **Xilinx Vivado** (simulation, synthesis, implementation, bitstream generation, board up-up) and early exposure to ASIC flow in RTL Synthesis and Static Timing Analysis. Actively learning Synopsys Design Compiler and PrimeTime for constraint-driven synthesis and static timing closure with production-quality SDC constraints.

Technical Skills

RTL Design & Verification: System Verilog/Verilog, RTL Synthesis, FSMs, self-checking testbenches, Assertions, simulation and waveform debug
FPGA Prototyping: Xilinx Vivado (simulation, synthesis, implementation, timing, bitstream)
EDA Tools: Learning Synopsys Design Compiler, PrimeTime STA fundamentals, introductory SDC authoring
Programming & Tools: C/C++, Python, Linux, Xilinx Vivado
Protocols: UART, APB

Experience

Undergraduate Researcher—VLSI Systems & Computer Architecture Lab (VSCLab) Sep 2025–Present

University of California, Riverside

- Designing and implementing a custom open-source **RISC-V CPU core** while building proficiency in SystemVerilog RTL-to-gate signoff using Synopsys flows.
- Learning constraint-driven synthesis in **Synopsys Design Compiler** alongside graduate mentors, contributing to SDC constraint development, library management, and early optimization passes.
- Reviewing **Design Compiler** timing and power reports with mentor guidance to understand pipeline depth, clock gating, and cell selection trade-offs for balanced PPA.
- Collaborating with graduate mentors to explore **microarchitecture optimization** for performance and area efficiency.

RTL Design Intern @ Intel Corporation Jun 2025–Present

Intel Corporation *San Diego, CA*

- Designed and verified **SystemVerilog RTL modules** for SoC datapaths and control logic, contributing to next-generation compute products.
- Implemented synthesizable RTL from microarchitecture specifications, with emphasis on **low-latency, power-efficient** designs.
- Developed and executed **self-checking testbenches**; ran **simulation, lint, synthesis, and static timing analysis** toward sign-off quality.
- Collaborated with architecture and verification teams to **close functional/timing coverage**, resolving corner cases and CDC issues in industry EDA flows.

Projects

Military-Grade Field Vision Processing System Jun 2025–Present

- Architected and implemented a **real-time field vision system** on FPGA, integrating a custom **RISC-V processing core** with dedicated pipelines for military-grade sensor applications.
- Aided in the implementation of image capture and processing pipelines to support **autonomous navigation and self-driving mechanisms**.
- Leveraged FPGA parallelism for **low-latency visual data processing**, combined with software-controlled RISC-V CPU for **decision logic and system coordination**.
- Focused on **secure, reconfigurable, and mission-adaptable architectures** suitable for defense applications.

Smart Power Monitoring & Control System Nov 2024–Present

- Designed a beginner-level PCB-based power monitoring system using a microcontroller and voltage/current sensors to track energy usage and understand hardware-software integration fundamentals.
- Wrote **embedded C/C++ firmware** to collect, process, and display power usage data, with plans to expand to **wireless monitoring**.
- Created an **iOS app** to visualize real-time **power consumption trends**, integrating with the microcontroller via **Bluetooth and Wi-Fi**.
- Tested and validated circuit performance using **multimeters and oscilloscopes**, ensuring accurate sensor readings and power efficiency.