Kaushik Vada

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Education

University of California, Riverside Riverside, CA

Bachelor of Science in Electrical Engineering — University of California Regents Distinguished Scholar *Aug 2023 – May 2027*

GPA: 3.93/4.00

Relevant Coursework: Introduction to VLSI, Data Structures and Algorithms, Design and Architecture of Computer Systems, Machine Organization and Assembly Language, Digital Logic Design

Qualifications

Student in electrical engineering with a VLSI focus, gaining experience in **Verilog** RTL design, FPGA development using **Xilinx Vivado**, and introductory ASIC flow experience including RTL synthesis and timing analysis using **Synopsys Design Compiler** and **Synopsys VCS**.

Technical Skills

Programming Languages: Verilog, SystemVerilog, C/C++, Python, TCL
Tools: Synopsys Design Compiler, Synopsys VCS, Xilinx Vivado
Concepts: RTL Design, Static Timing Analysis, Computer Architecture, Caches, RISC-V Architecture
Protocols: UART, APB, Valid/Ready Handshake
OS/Envionrment: Unix/Linux, Windows

Projects

Two-Level Cache RTL (L1–L2) Jan 2025 – Present

- Implemented configurable **Verilog RTL** for L1/L2 caches (parameterized sets, ways, and line sizes) with **LRU** replacement and **write-back/write-allocate** policies.
- Designed tag/data/valid arrays and a lightweight memory interface to emulate main-memory latency and hierarchy-level handshakes.
- Developed **directed verification tests** in **Synopsys VCS**, crafting access patterns to stress-hit/miss paths, replacement behavior, and write-back/write-allocate flows.
- Debugged behavior using **Verdi**—instrumented hit/miss counters, traced tag/LRU updates, and inspected waves to ensure functional correctness across cache configurations.
- Analyzed timing and throughput trade-offs through parameter sweeps and monitored correctness under varying associativities and line sizes.

RISC-V Pipeline RTL Modules for Field-Vision Processing System Jun 2025 – Present

- Implemented core RTL modules for a custom **RISC-V processor** on FPGA, including **Instruction Fetch**, **Instruction Decode**, and **ALU** stages.
- Simulated, debugged, and waveform-analyzed pipeline behavior using **Xilinx Vivado**.
- Collaborated with teammates integrating pipeline modules into a larger embedded vision system.

Battery Management & Thermal Control System (BMS) Nov 2024 – Present

- Designing a custom PCB-based **10-cell Li-ion BMS**, integrating voltage, current, and temperature sensing for safe pack operation.
- Performing **CAD modeling and thermal simulations** to evaluate airflow, heat dissipation, and enclosure design for reliable cooling.
- Developing embedded **C/C++ firmware** for data acquisition, fan control, USB communication, and real-time safety protection.
- Validating hardware performance using **oscilloscopes, multimeters, and thermistors** to ensure accurate sensing and thermal response.

Experience

Hardware Design Intern @ Digital Force Technologies (DFT) Jun 2025 – Aug 2025
Digital Force Technologies (DFT) *San Diego, CA*

- Implemented core RTL modules for a custom **RISC-V processor** on FPGA, including **Instruction Fetch**, **Instruction Decode**, and **ALU** stages.
- Verified module correctness through **simulation**, waveform inspection, and iterative debugging.
- Collaborated with engineers integrating processor components into a larger embedded vision system.
- Gained exposure to **synthesis** and EDA workflows used in industry RTL development environments.

Undergraduate Researcher — VLSI Systems & Computer Architecture Lab (VSCLab) Sep 2025 – Present
University of California, Riverside *Riverside, CA*

- Currently designing and implementing a custom open-source **RISC-V CPU core**, actively developing pipeline stages and verification infrastructure.
- Developing proficiency in **Verilog** and Synopsys RTL-to-gate flows through ongoing research work.
- Learning and contributing to **constraint-driven synthesis** in **Synopsys Design Compiler**, including writing and refining SDC timing constraints.