# Multiplexer and Decoder

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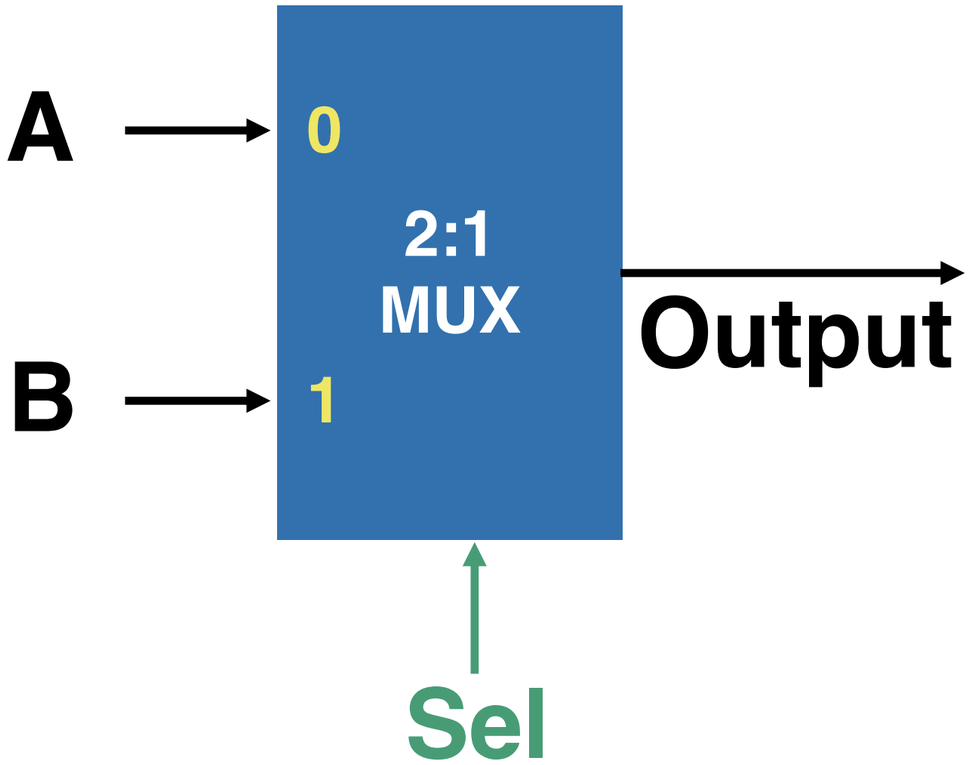
# Multiplexer

# Let's start with a 2-to-1 Multiplexer (MUX)

- The MUX has two input ports — numbered as 0 and 1
- To select from two inputs, you need a 1-bit control/select signal to indicate the desired input port



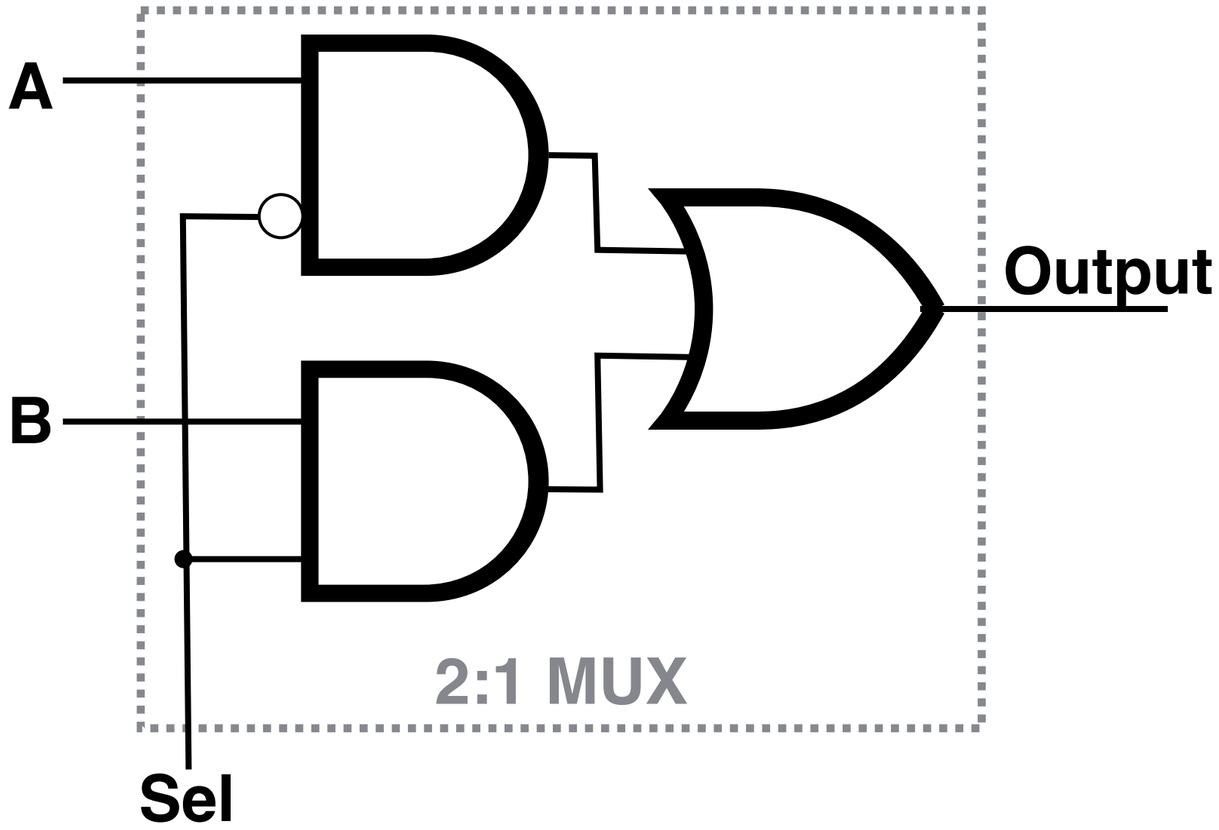

| Input | | | Output |
|---|---|---|---|
| A | B | Sel | |
| 0 | 0 | 0 | **0** |
| 0 | 1 | 0 | **0** |
| 1 | 0 | 0 | **1** |
| 1 | 1 | 0 | **1** |
| 0 | 0 | 1 | **0** |
| 0 | 1 | 1 | **1** |
| 1 | 0 | 1 | **0** |
| 1 | 1 | 1 | **1** |



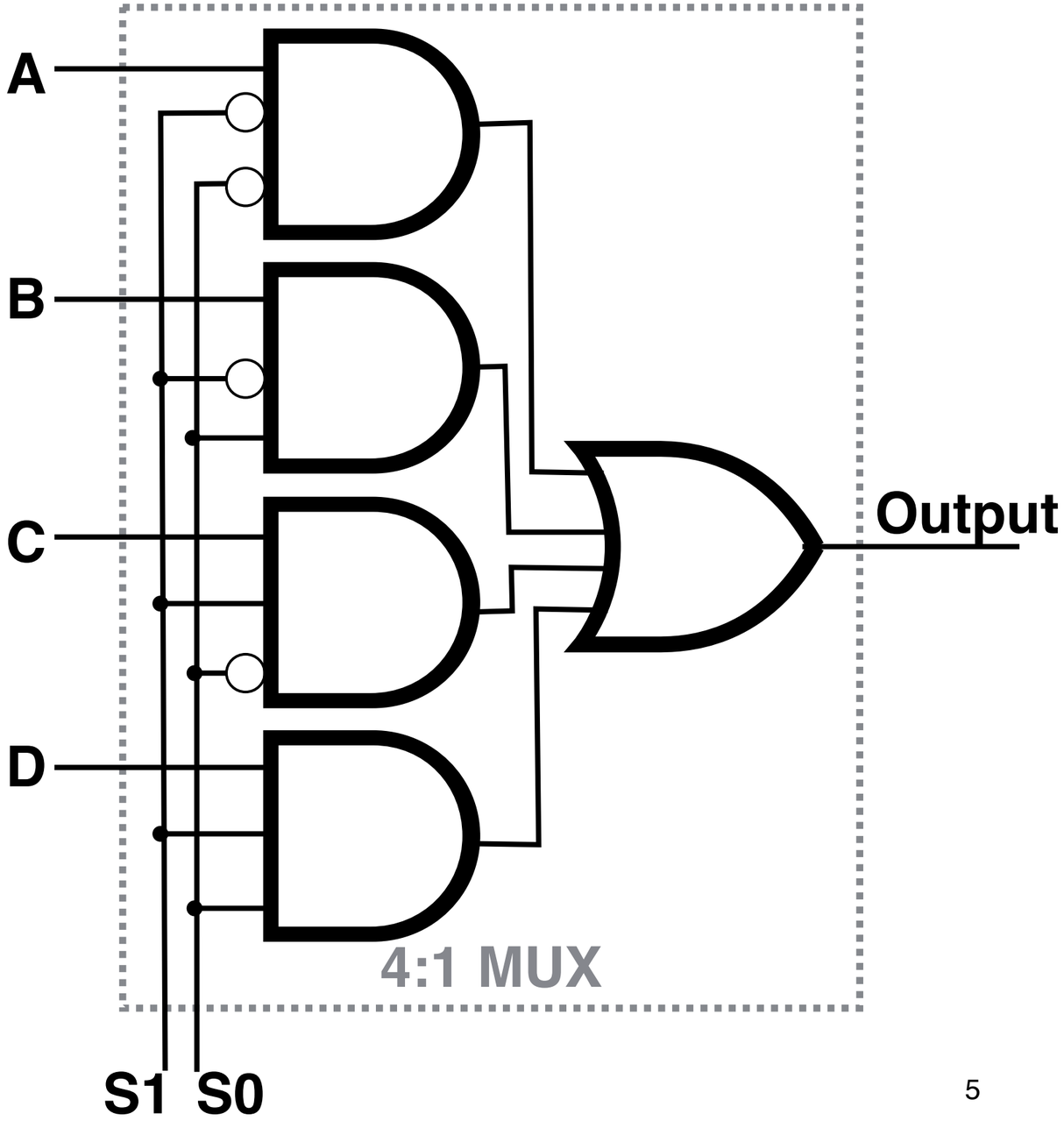
*Slide is adapted from Hung-Wei Tseng*

# 2-to-1 MUX

**Output = ASel’ + BSel**

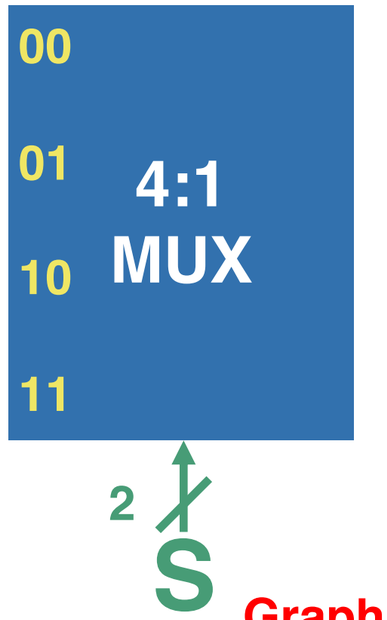


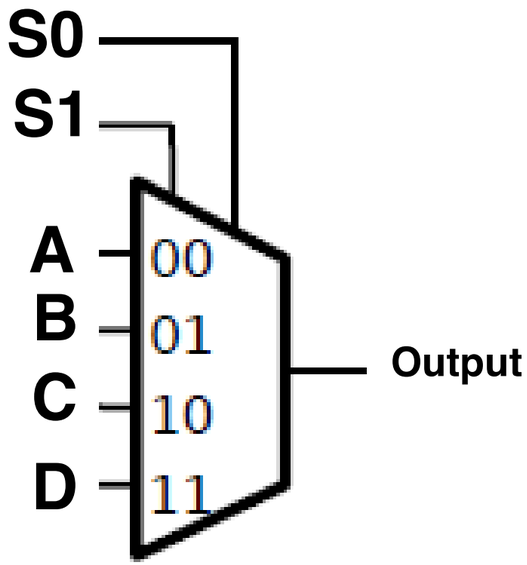
# 4-to-1 MUX




S1==0 && S0==0 output A
S1==0 && S0==1 output B
S1==1 && S0==0 output C
S1==1 && S0==1 output D

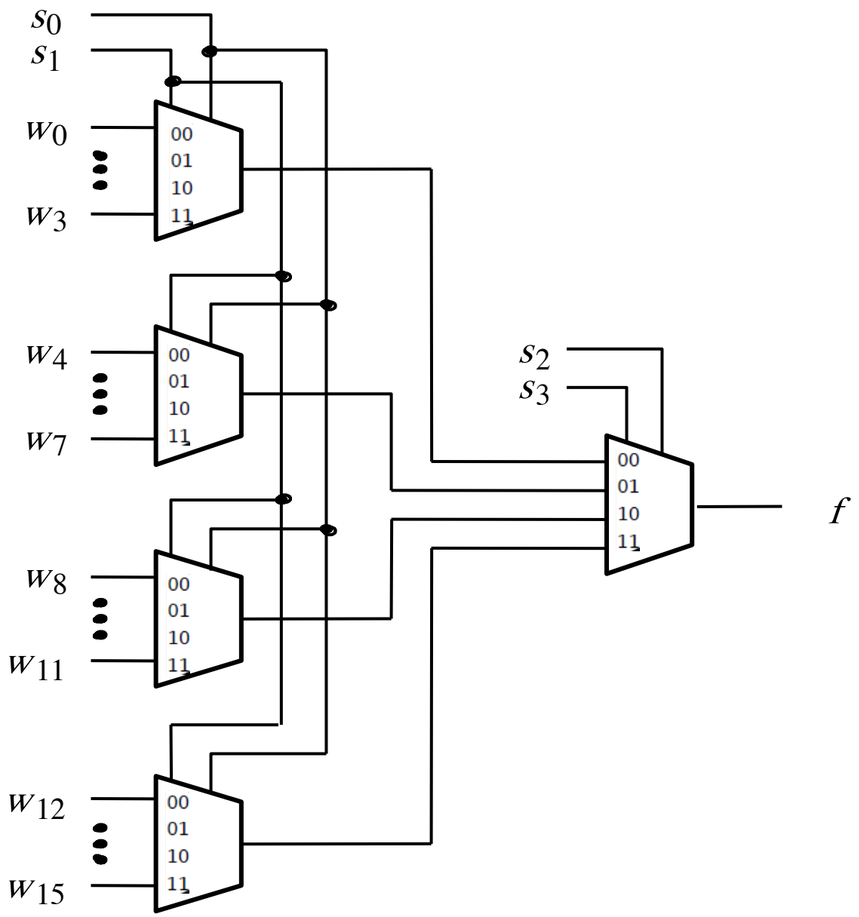
Output = AS0'S1' + BS0S1' +
CS0'S1 + DS0S1




Graphical symbols

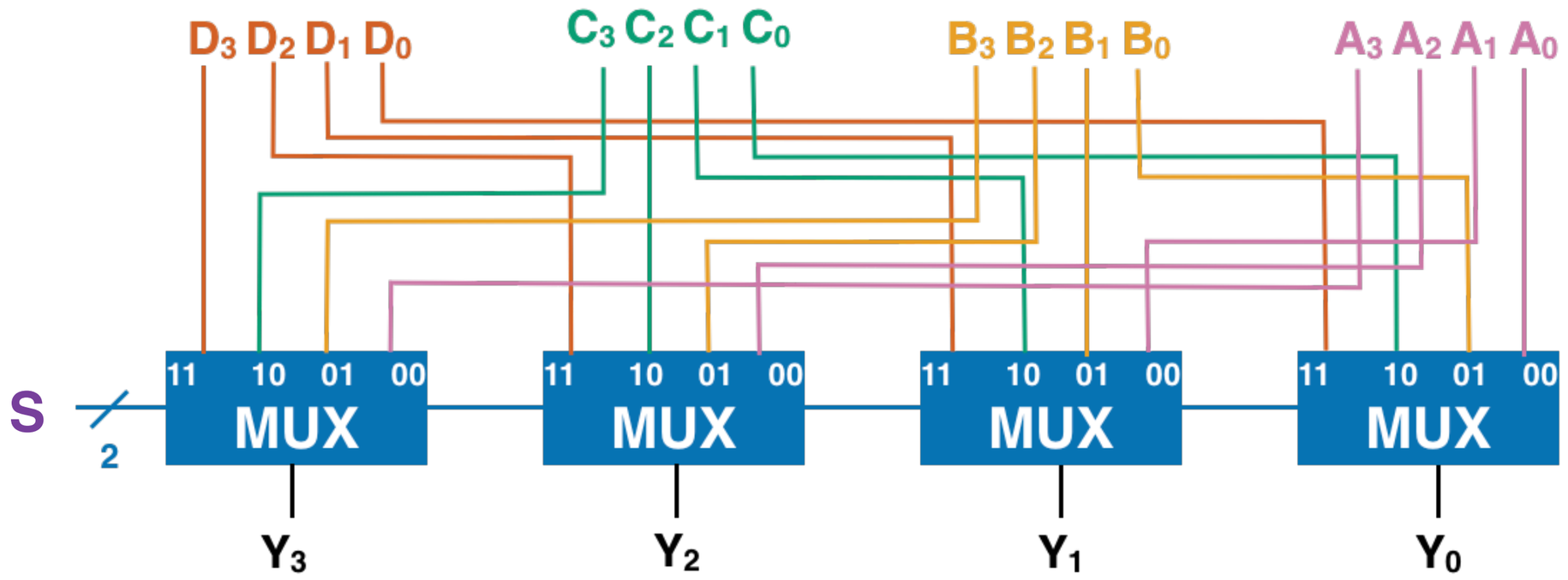
# 16-to-1 MUX




A 16-to-1 multiplexer.

# N-bit MUX

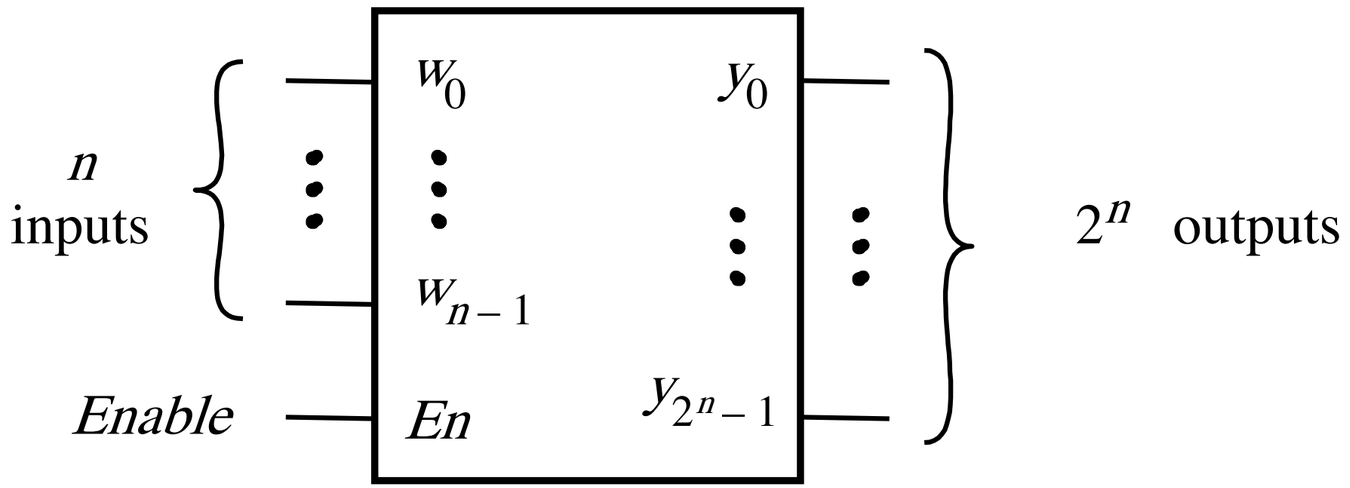
- What if we need to output an N-bit (say 4-bit) number from the input set?



# Decoder

# Decoders

Only one of the outputs is asserted at a time (i.e., which is different from all the others), and each output corresponds to one valuation of the inputs.

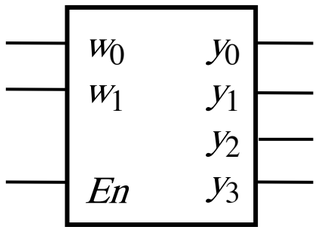



An $n$-to-$2^n$ binary decoder.

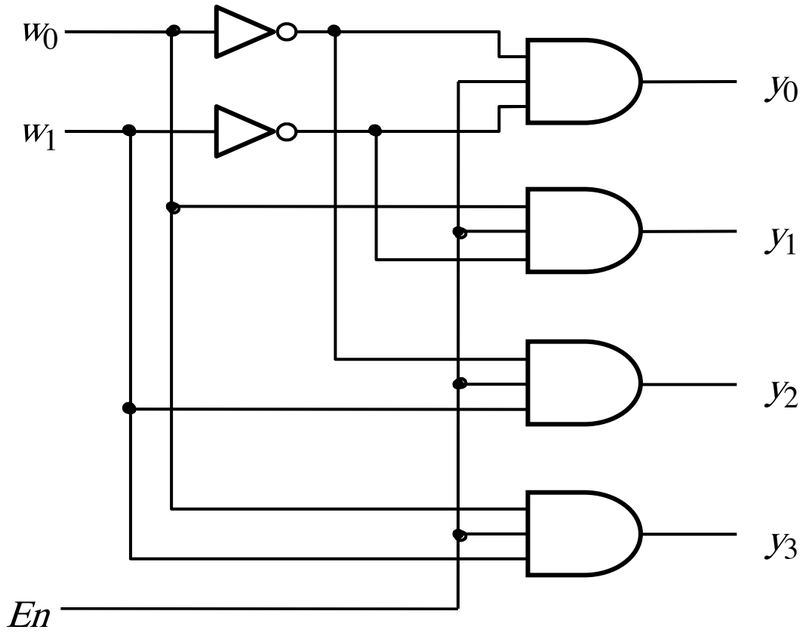
# Decoders

| $En$ | $w_1$ | $w_0$ | $y_0$ | $y_1$ | $y_2$ | $y_3$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | x | x | 0 | 0 | 0 | 0 |

(a) Truth table

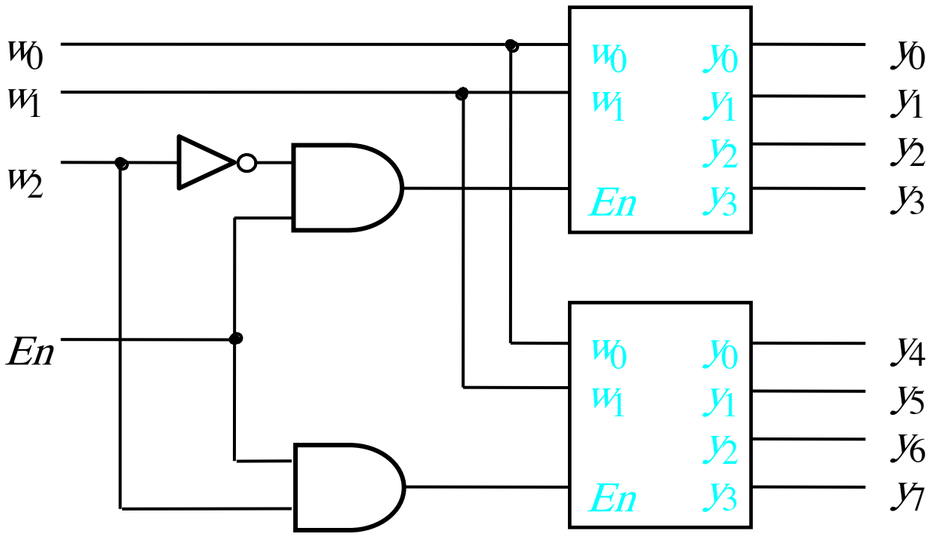



(b) Graphical symbol




(c) Logic circuit

# Decoders




A 3-to-8 decoder using two 2-to-4 decoders.

# Incompletely Specified Functions

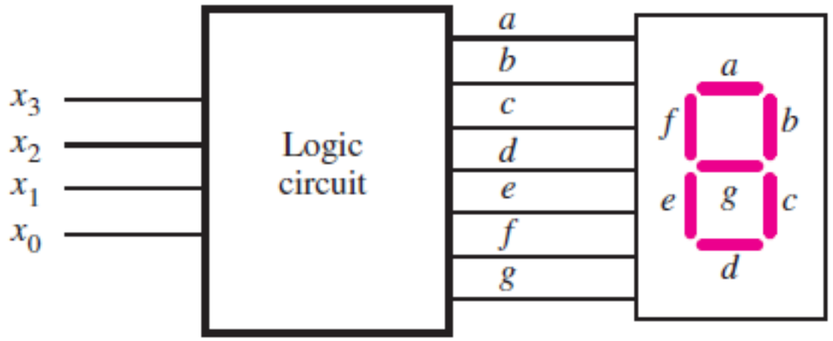
- Certain input conditions can never occur

  E. g. (x1, x2) = 11 is a don't-care condition: a circuit can be designed by ignoring this condition

- A function that has don't-care condition(s) is said to be incompletely specified.

- Assume that the function value for these valuations is either 1 or 0, whichever is more useful

# Truth table with Don't Cares




(a) Logic circuit and 7-segment display

| | $x_3$ | $x_2$ | $x_1$ | $x_0$ | $a$ | $b$ | $c$ | $d$ | $e$ | $f$ | $g$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| Don't-care conditions | 1 | 0 | 1 | 0 | x | x | x | x | x | x | x |
| | 1 | 0 | 1 | 1 | x | x | x | x | x | x | x |
| | 1 | 1 | 0 | 0 | x | x | x | x | x | x | x |
| | 1 | 1 | 0 | 1 | x | x | x | x | x | x | x |
| | 1 | 1 | 1 | 0 | x | x | x | x | x | x | x |
| | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |

- Each "x" for these valuations is either 1 or 0, whichever is more useful