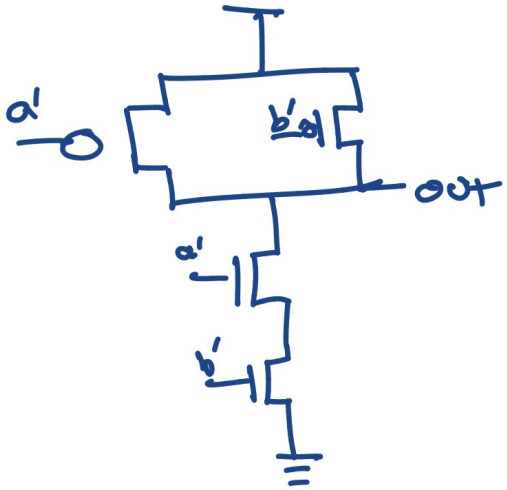
EE 168: Introduction to VLSI
Homework 2

Kaushik Vada

October 29, 2025

Problem 1: Static CMOS Gate Design

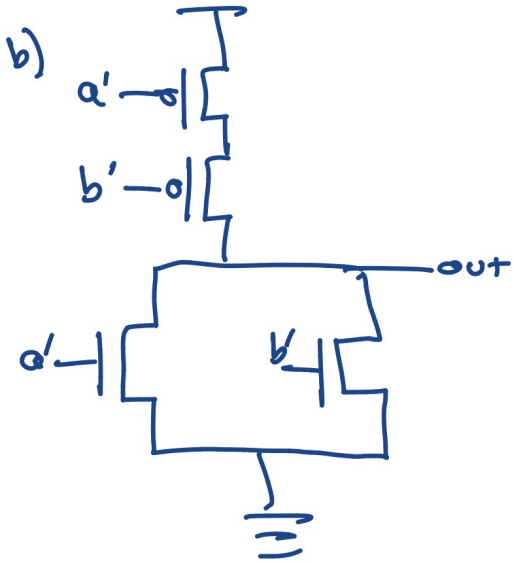
Design the static complementary gates (CMOS gates) for the following logic expressions using pull-up/pull-down networks. Use a truth table to show logical equivalence for converted expressions. Assume inverted variables are available, i.e., you do not have to add inverters for complementary variables.



$a + b = (a' \cdot b')'$

ab	$a'b'$	$a' \cdot b'$	$(a' \cdot b')'$	$a + b$
00	11	1	0	0
01	10	0	1	1
10	01	0	1	1
11	00	0	1	1

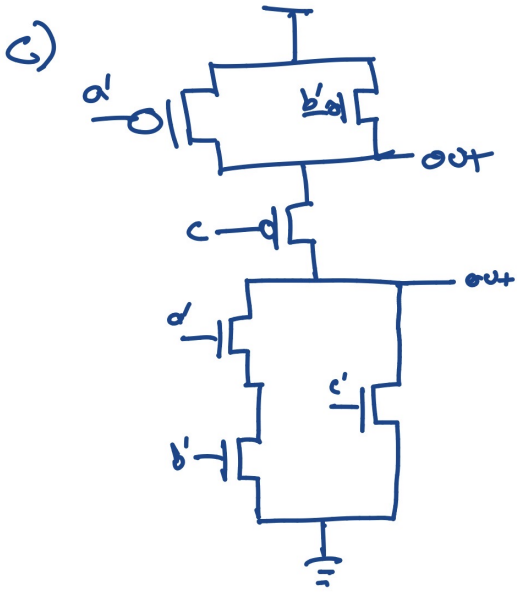
a)



$ab = (a' + b')'$

ab	$a'b'$	$a' + b'$	$(a' \cdot b')'$	$a + b$
00	11	1	0	0
01	10	1	0	0
10	01	1	0	0
11	00	0	1	1

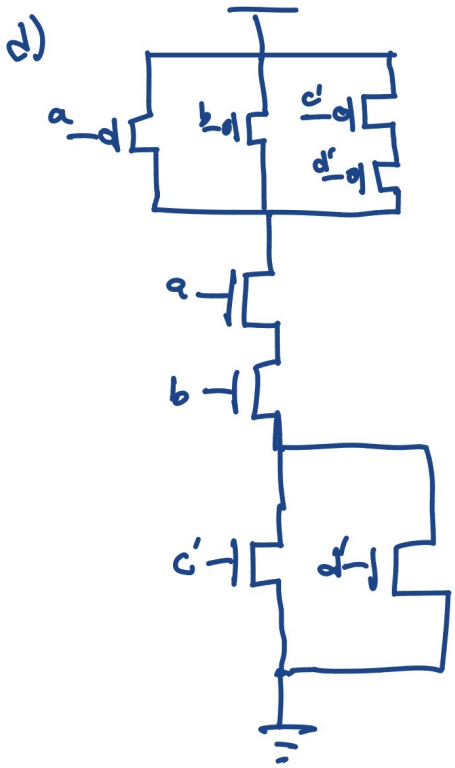
b)



$(a + b)c = ((a + b)' + c')' = ((a' \cdot b') + c')'$

abc	$a'b'c'$	$a' \cdot b'$	$(a' \cdot b') + c'$	$((a' \cdot b') + c')'$	$(a + b)c$
000	111	1	1	0	0
001	110	1	1	0	0
010	101	0	1	0	0
011	100	0	0	1	1
100	011	0	1	0	0
101	010	0	0	1	1
110	001	0	1	0	0
111	000	0	0	1	1

c)



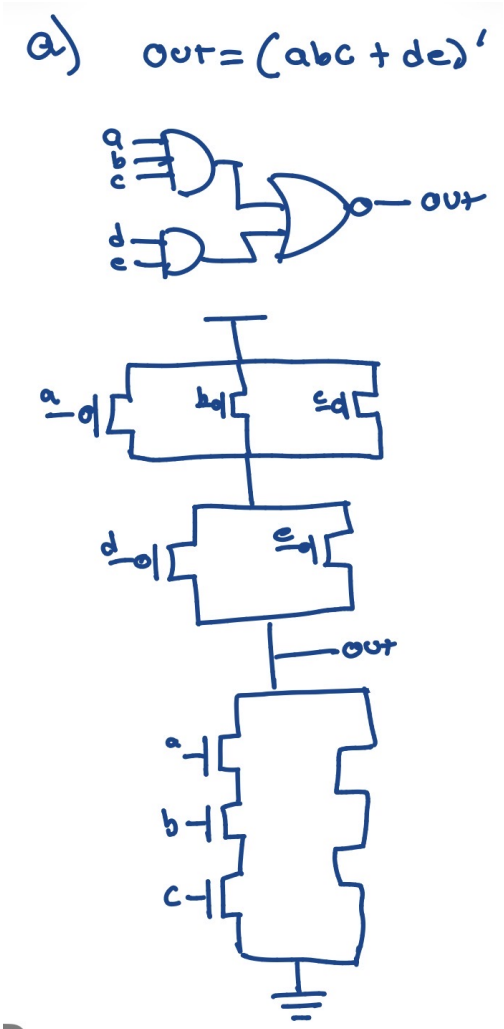
$(ab)' + (cd) = (ab \cdot (c' + d'))'$

$abcd$	ab	$c'd'$	$c' + d'$	$ab \cdot (c' + d')$	$(ab \cdot (c' + d'))'$
0000	0	11	1	0	1
0001	0	10	1	0	1
0010	0	01	1	0	1
0011	0	00	0	0	1
0100	0	11	1	0	1
0101	0	10	1	0	1
0110	0	01	1	0	1
0111	0	00	0	0	1
1000	0	11	1	0	1
1001	0	10	1	0	1
1010	0	01	1	0	1
1011	0	00	0	0	1
1100	1	11	1	1	0
1101	1	10	1	1	0
1110	1	01	1	1	0
1111	1	00	0	0	1

d)

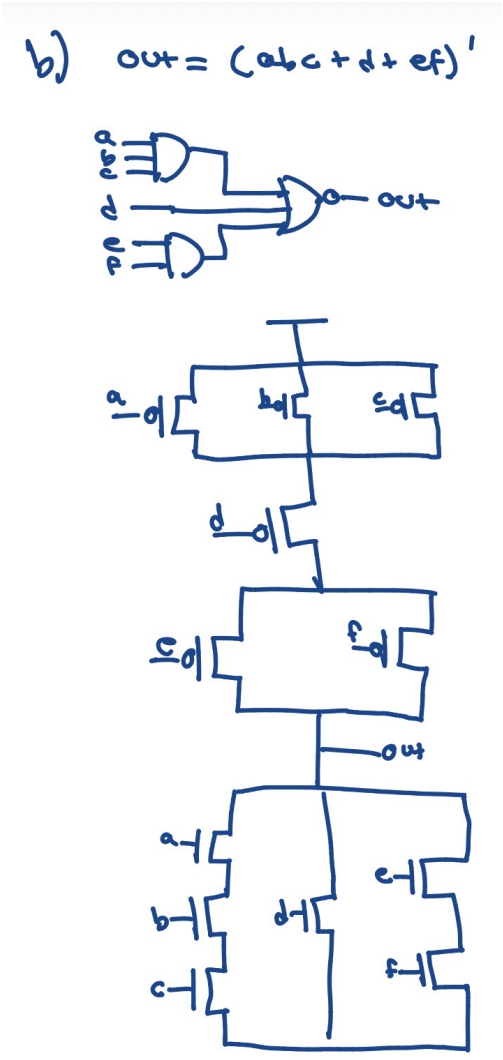
Problem 2: Complex Gate Implementations

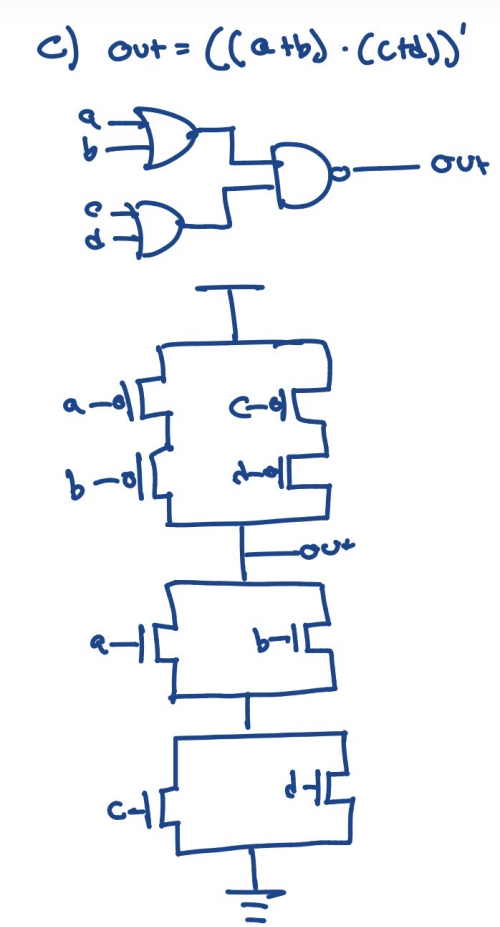
Write the defining logic expressions and draw the transistor level schematic for each complex gate below.



a) 1

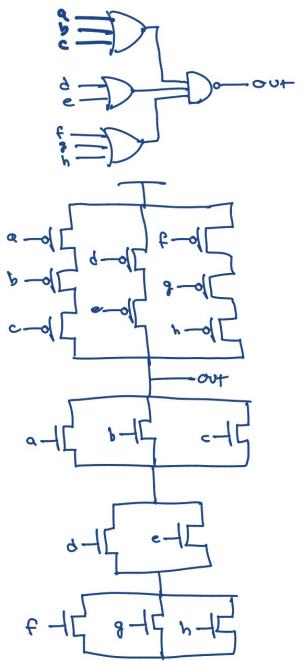
b)





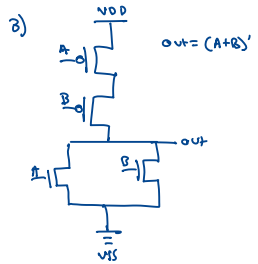
c)

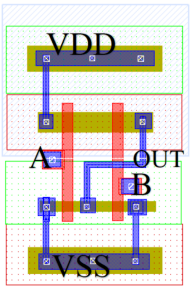
d) $out = \left((a+b+c)\cdot(d+e)\cdot(f+g+h)\right)'$



d)

3. Draw the circuit level schematic from the follow layout design. Write the logic expression of the extracted logic. The inputs are indicated by 'A' and 'B' and the output by the "OUT" label.





4. Size the transistors in each of those gates so that its pullup and pulldown times are approximate equal. Assume effective resistances for NMOS as $R_n = 6.47K\Omega$, for PMOS as $R_p = 29.6K\Omega$. The loading capacitance for the network is C_L. Please show all the steps. Please consider the following two cases:

(1) In the worst case

(2) In the best case

a) f = a'b'c'+d'

b) f = a'b'+c'd'

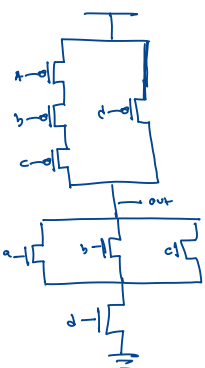
c) f = a'b+bc

$t_r = t_f \Rightarrow (R_{up} + R_n) C_L = (R_{down} + R_n) C_L$

$R_n = 0 \Rightarrow R_{up} C_L = R_{down} C_L$

$\frac{R_p}{R_n} = \frac{29.6}{6.47} = \frac{2960}{647} = 4.575$

a) $f = a'b'c' + d' = ((a+b+c)\cdot d)'$



worst case: 2 NMOS, 3 PMOS

$R_{up} = 3 \cdot \frac{L_p}{W_p} \cdot R_p$

$R_{down} = 2 \cdot \frac{L_n}{W_n} \cdot R_n$

$R_{up} C_L = R_{down} C_L$

$\Rightarrow 3 \cdot \frac{2960}{647} \cdot \frac{L_p}{W_p} = 2 \cdot \frac{L_n}{W_n}$

$6.86 \cdot \frac{L_p}{W_p} = \frac{L_n}{W_n}$

$\frac{W_p}{L_p} = 6.86 \cdot \frac{W_n}{L_n}$

Best case: 2 NMOS, 1 PMOS

$R_{up} = 1 \cdot \frac{L_p}{W_p} \cdot R_p$

$R_{down} = 2 \cdot \frac{L_n}{W_n} \cdot R_n$

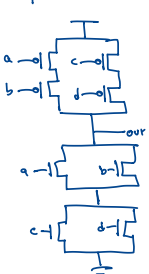
$R_{up} C_L = R_{down} C_L$

$1 \cdot \frac{2960}{647} \cdot \frac{L_p}{W_p} = 2 \cdot \frac{L_n}{W_n}$

$= 2.29 \cdot \frac{L_p}{W_p} = \frac{L_n}{W_n}$

$= \frac{W_p}{L_p} = 2.29 \cdot \frac{W_n}{L_n}$

b) $f = a'b' + c'd' = ((a+b)\cdot(c+d))'$



worst case

$R_{up} = 2 \cdot \frac{L_p}{W_p} \cdot R_p$

$R_{down} = 2 \cdot \frac{L_n}{W_n} \cdot R_n$

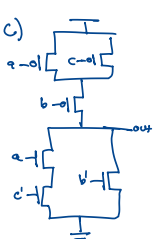
$R_{up} C_L = R_{down} C_L$

$= 2 \cdot \frac{2960}{647} \cdot \frac{L_p}{W_p} = 2 \cdot \frac{L_n}{W_n}$

$= \frac{2960}{647} \cdot \frac{L_p}{W_p} = \frac{L_n}{W_n}$

$\frac{W_p}{L_p} = 4.57 \cdot \frac{W_n}{L_n}$

c)



worst case

$R_{up} = 2 \cdot \frac{L_p}{W_p} \cdot R_p$

$R_{down} = 2 \cdot \frac{L_n}{W_n} \cdot R_n$

$R_{up} C_L = R_{down} C_L$

$2 \cdot \frac{2960}{647} \cdot \frac{L_p}{W_p} = 2 \cdot \frac{L_n}{W_n}$

$\frac{2960}{647} \cdot \frac{L_p}{W_p} = \frac{L_n}{W_n}$

$\frac{W_p}{L_p} = 4.57 \cdot \frac{W_n}{L_n}$

Best case

$R_{up} = 2 \cdot \frac{L_p}{W_p} \cdot R_p$

$R_{down} = 1 \cdot \frac{L_n}{W_n} \cdot R_n$

$R_{up} C_L = R_{down} C_L$

$2 \cdot \frac{2960}{647} \cdot \frac{L_p}{W_p} = 1 \cdot \frac{L_n}{W_n}$

$9.16 \cdot \frac{L_p}{W_p} = \frac{L_n}{W_n}$

$\frac{W_p}{L_p} = 9.16 \cdot \frac{W_n}{L_n}$

Problem 5: Effective Resistance with Varying Load Capacitance

Compute the value of R_{eff} required to model the behavior of an inverter that reaches 50% of its output value at 20 ps with load C_L equal to $3C_1$, $4C_1$, and $5C_1$. What effect does load capacitance have on the effective resistance? ($C_1 = 0.89 \times 10^{-15}$)

$$C_1 = 0.89\,\text{fF}, \qquad t_s = 20\,\text{ps}, \qquad \frac{V_f}{V_0} = 0.5$$

$$R_{\text{eff}} = \frac{t_s}{C_L \ln\left(\frac{V_f}{V_0}\right)}$$

$$C_L = 3C_1 \implies R_{\text{eff}} = \frac{20 \times 10^{-12}}{3 \times 0.89 \times 10^{-15} \ln(0.5)} = 1.081 \times 10^4\,\Omega = 10.81\,\text{k}\Omega$$

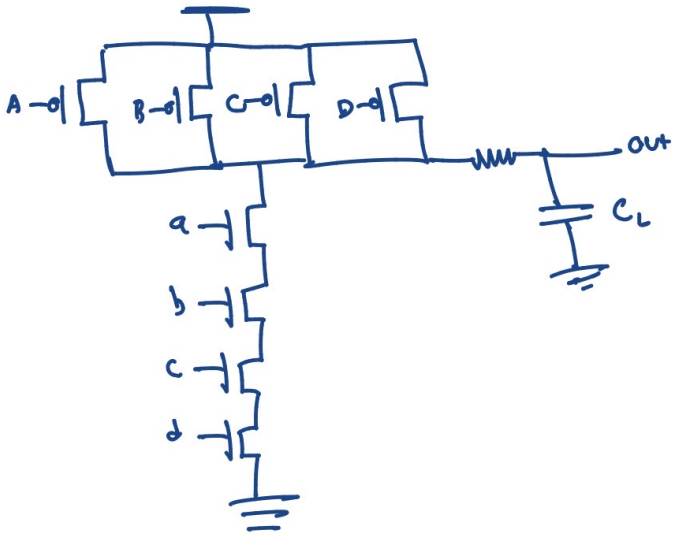
$$C_L = 4C_1 \implies R_{\text{eff}} = \frac{20 \times 10^{-12}}{4 \times 0.89 \times 10^{-15} \ln(0.5)} = 8.11 \times 10^3\,\Omega = 8.11\,\text{k}\Omega$$

$$C_L = 5C_1 \implies R_{\text{eff}} = \frac{20 \times 10^{-12}}{5 \times 0.89 \times 10^{-15} \ln(0.5)} = 6.48 \times 10^3\,\Omega = 6.48\,\text{k}\Omega$$

Larger $C_L \Rightarrow$ smaller R_{eff}.

Problem 6: Transition Times for Four-Input NAND Driving NOR Gate

Compute transition times for a four-input NAND gate with 8/2 pulldown (the $W/L = 8/2$ for n-type transistors) and 8/2 pullup that drives an identically sized NOR four-input gate (the NAND gate only drives one input of the NOR gate).



$$R_{\text{up}} = 1 \cdot \frac{L_p}{W_p} \cdot R_p = 1 \times \frac{2}{8} \times 29.6 = 7.40\,\text{k}\Omega$$

$$R_{\text{down}} = 4 \cdot \frac{L_n}{W_n} \cdot R_n = 4 \times \frac{2}{8} \times 6.47 = 6.47\,\text{k}\Omega$$

$$R_L = 0, \qquad C_L = \left(\frac{W_p}{L_p} + \frac{W_n}{L_n}\right) C_1 = \left(\frac{8}{2} + \frac{8}{2}\right) \cdot 0.89 \times 10^{-15} = 7.12\,\text{fF}$$

$$t_r = -(R_{\text{up}} + R_L)C_L \ln(0.1) = -7.40 \times 10^3 \cdot 7.12 \times 10^{-15} \ln(0.1) = 121.32\,\text{ps}$$

$$t_f = -(R_{\text{down}} + R_L)C_L \ln(0.1) = -6.47 \times 10^3 \cdot 7.12 \times 10^{-15} \ln(0.1) = 106.07\,\text{ps}$$

Problem 7: Rise Time with Different Interconnects

Compute rise time for a two-input NAND gate with 8/2 pull-down and 8/2 pull-up that drives the interconnects described below (assume the wire impedance is modeled as a single lump):

$$R_{\text{up}} = 1 \cdot \frac{L_p}{W_p} \cdot R_p = 1 \times \frac{2}{8} \times 29.6 = 7.4\,\text{k}\Omega, \qquad \lambda = \frac{180}{2} = 90\,\text{nm} = 0.09\,\mu\text{m}$$

$$A = WL, \qquad P = 2(W + L)$$

a) Poly interconnect ($W = 3\lambda$, $L = 300\lambda$):

$$\begin{aligned} R_L &= 8\frac{L}{W} = 8\frac{3000\lambda}{3\lambda} = 800\ \Omega, \\ C_L &= 63 \times 10^{-18}\big(27 \cdot 0.27 + 2(27 + 0.27)\big) = 3.90 \times 10^{-15}\,\text{F}, \\ t_r &= -\big(7.4 \times 10^3 + 800\big)\, C_L\, \ln 0.1 = 73.55\ \text{ps}. \end{aligned}$$

b) Metal-1 interconnect ($W = 4\lambda$, $L = 600\lambda$):

$$\begin{aligned} R_L &= 0.08\frac{L}{W} = 0.08\frac{600\lambda}{4\lambda} = 12\ \Omega, \\ C_L &= 36 \times 10^{-18}(54 \cdot 0.36) + 54 \times 10^{-18}\, 2(54 + 0.36) = 6.57 \times 10^{-15}\,\text{F}, \\ t_r &= -\big(7.4 \times 10^3 + 12\big)\, C_L\, \ln 0.1 = 111.98\ \text{ps}. \end{aligned}$$

c) Metal-2 interconnect ($W = 4\lambda$, $L = 1200\lambda$):

$$\begin{aligned} R_L &= 0.08\frac{L}{W} = 0.08\frac{1200\lambda}{4\lambda} = 24\ \Omega, \\ C_L &= 36 \times 10^{-18}(108 \cdot 0.36) + 51 \times 10^{-18}\, 2(108 + 0.36) = 1.245 \times 10^{-14}\,\text{F}, \\ t_r &= -\big(7.4 \times 10^3 + 24\big)\, C_L\, \ln 0.1 = 212.25\ \text{ps}. \end{aligned}$$

Problem 8: Buffer Insertion Delay Optimization

For a metal 1 wire with $R_{\text{int}} = 500\,\Omega$, $C_{\text{int}} = 200\,\text{fF}$, and minimum-size buffer parameters $R_0 = 6.47\,\text{k}\Omega$ and $C_0 = 1.78\,\text{fF}$, determine the 50% delay in the following cases:

a) One buffer inserted, one section ($k = 1$), buffers at minimum size ($h = 1$).

b) Two buffers inserted, wire divided into two sections ($k = 2$), buffers at minimum size ($h = 1$).

c) Two buffers inserted, wire divided into two sections ($k = 2$), buffers sized to twice minimum ($h = 2$).

d) Optimal number of buffers, buffer size, and the resulting minimum 50% delay.

$$T_{50\%}(k,h) = k\left[0.7\frac{R_0}{h}\left(\frac{C_{\text{int}}}{k} + hC_0\right) + R_{\text{int}}\left(0.4\frac{C_{\text{int}}}{k} + 0.7hC_0\right)\right]$$

a) Minimum-size single buffer ($k = 1, h = 1$):

$$\begin{aligned}
\alpha &= 0.7R_0 = 4.529 \times 10^3\,\Omega,\\
C_\Sigma &= C_{\text{int}} + C_0 = 201.78 \times 10^{-15}\,\text{F},\\
\beta &= 0.4C_{\text{int}} + 0.7C_0 = 81.246 \times 10^{-15}\,\text{F},\\
T_{50\%} &= \alpha C_\Sigma + R_{\text{int}}\beta = 9.5448 \times 10^{-10}\,\text{s} = 954.48\ \text{ps}.
\end{aligned}$$

b) Two sections with minimum buffers ($k = 2, h = 1$):

$$\begin{aligned}
C_{\text{stage}} &= \frac{C_{\text{int}}}{2} + C_0 = 101.78 \times 10^{-15}\,\text{F},\\
\beta_{\text{stage}} &= 0.4\frac{C_{\text{int}}}{2} + 0.7C_0 = 41.246 \times 10^{-15}\,\text{F},\\
T_{50\%} &= 2\left[\alpha C_{\text{stage}} + \frac{R_{\text{int}}}{2}\beta_{\text{stage}}\right] = 9.4255 \times 10^{-10}\,\text{s} = 942.55\ \text{ps}.
\end{aligned}$$

c) Two sections with buffers twice minimum ($k = 2, h = 2$):

$$\begin{aligned}
\alpha_2 &= 0.7\frac{R_0}{2} = 2.2645 \times 10^3\,\Omega,\\
C_{\text{stage}} &= \frac{C_{\text{int}}}{2} + 2C_0 = 103.56 \times 10^{-15}\,\text{F},\\
\beta_{\text{stage}} &= 0.4\frac{C_{\text{int}}}{2} + 0.7(2C_0) = 42.492 \times 10^{-15}\,\text{F},\\
T_{50\%} &= 2\left[\alpha_2 C_{\text{stage}} + \frac{R_{\text{int}}}{2}\beta_{\text{stage}}\right] = 4.9027 \times 10^{-10}\,\text{s} = 490.27\ \text{ps}.
\end{aligned}$$

d) Optimal buffering:

$$\begin{aligned}
k_{\text{opt}} &= \sqrt{\frac{0.4R_{\text{int}}C_{\text{int}}}{0.7R_0C_0}} = 2.23,\\
h_{\text{opt}} &= \frac{R_0C_{\text{int}}}{R_{\text{int}}C_0} = 38.13,\\
T_{50\%}^{\text{min}} &= 2.5\sqrt{R_0C_0R_{\text{int}}C_{\text{int}}} = 8.484 \times 10^{-11}\,\text{s} = 84.84\ \text{ps}.
\end{aligned}$$