Modern VLSI Design — Chapter 2 (180 nm CMOS)

A thorough explainer with the pictures, the math, and the pitfalls — plus practice prompts.

0) Orientation: the mental model

- **Target process: generic 180 nm CMOS**, $V_{DD} = 1.2\,\mathbf{V}$.
- **Layout ruler:** $\lambda = 90\,\text{nm}$ (half of min feature). *Minimum device for this class:* $W = 3\lambda$, $L = 2\lambda \Rightarrow W/L = 1.5$.
- **PDKs in lab:** 90 nm and 28 nm (Synopsys). Concepts transfer; rules and numbers change.
- **Edu shuttles:** MOSIS, EuroPractice, CIC, VDEC. (*Foundry* = fab-for-hire.)

Key Idea

Think in layers: substrate → gate (poly) → S/D diffusions → interconnect metals → vias that stitch it all together.

1) Fabrication: from sand to shapes

Materials & roles.

- Silicon substrate; dope *regions* n-type/p-type ($n+$ = heavy).
- Conductors: polysilicon (gates) + multi-layer Al/Cu (wires).
- Insulator: SiO_2 (gate oxide, inter-layer dielectrics).

Photolithography in one line: masks + photoresist + etch/deposit = patterned layers.

Process flow (conceptual):

1. **Wells/tubs** for NMOS/PMOS: create p-well and n-well base regions.
2. **Poly gate** is patterned (defines channel length).
3. **Self-aligned S/D** implants: n^+ and p^+ formed beside the gate edge.
4. **Metals + vias**: stack M1, M2, …; vias provide vertical connections.

Checklist

Name the big three layers you'll sketch constantly: **diffusion**, **poly**, **metal**. Remember: **poly over active** = a *gate*.

Quick Test

If $\lambda = 90\,\text{nm}$, what drawn gate length corresponds to 2λ? What about a minimum drawn gate width 3λ in nm?

2) MOSFET essentials (NMOS/PMOS)

Terminals: Gate (G), Source (S), Drain (D), Bulk (B).
NMOS: carriers are electrons; conventional current *drain* $\rightarrow$ *source*.
PMOS: carriers are holes; conventional current *source* $\rightarrow$ *drain*.

Threshold (V_t): channel forms under the gate when inversion occurs; body bias shifts effective threshold.

Checklist

Spot the symbol set: enhancement vs. depletion; bulk-tied vs. bulk-floating symbols. Always label G,S,D,B.

2.1 Layout view and device geometry

- W is gate *width* (into/out of page for single-finger; sum across fingers).
- L is gate *length* (critical dimension; set by lithography).
- Minimum class device: $W = 3\lambda,\ L = 2\lambda \Rightarrow W/L = 1.5$.

3) I–V behavior you actually use

Define **overdrive** $V_{\text{ov}} \equiv V_{\text{GS}} - V_{\text{t}}$.

$$\textbf{Linear (triode)} \quad (V_{\text{DS}} < V_{\text{ov}}): \quad I_{\text{D}} = k' \left(\frac{W}{L}\right) \left[(V_{\text{GS}} - V_{\text{t}})V_{\text{DS}} - \tfrac{1}{2}V_{\text{DS}}^2\right]$$

$$\textbf{Saturation} \quad (V_{\text{DS}} \geq V_{\text{ov}}): \quad I_{\text{D}} = \tfrac{1}{2}k' \left(\frac{W}{L}\right) (V_{\text{GS}} - V_{\text{t}})^2$$

Ideal sat: I_{D} is nearly independent of V_{DS} (pinch-off at drain end).

3.1 Quick region test (use every time)

1. Compute $V_{\text{ov}} = V_{\text{GS}} - V_{\text{t}}$.
2. Compare V_{DS} to V_{ov}: if $V_{\text{DS}} < V_{\text{ov}}$ use **linear**; else **sat**.

At the boundary ($V_{\text{DS}} = V_{\text{ov}}$), both equations "meet" (useful for normalization).

3.2 Hand numbers for 180 nm (back-of-envelope)

	NMOS	PMOS
k' (transconductance parameter)	$k'_n \approx 170\ \mu\text{A/V}^2$	$k'_p \approx -30\ \mu\text{A/V}^2$
V_t	$\approx +0.5\,\text{V}$	$\approx -0.5\,\text{V}$
Class minimum	$W = 3\lambda,\ L = 2\lambda \Rightarrow W/L = 1.5$	

3.3 Direction/sign conventions that trip people up

- PMOS equations mirror NMOS with sign flips: $V_{GS,p} = -|V_{GS}|$, $V_{DS,p} = -|V_{DS}|$, $V_{t,p} = -|V_t|$, $I_{D,p}$ flows from *source to drain*.
- When comparing magnitudes, use absolute values for clarity.

Key Idea

Use V_{ov} **as your anchor**. First decide the region, *then* pick the formula.

4) Worked pattern you'll reuse (sanity-check math)

At $W/L = 1.5$, boundary between linear/sat ($V_{\text{DS}} = V_{\text{ov}}$):

$$I_{\text{D}} = \tfrac{1}{2}k'\left(\frac{W}{L}\right)(V_{\text{GS}} - V_{\text{t}})^2$$

So with $V_{\text{GS}} = 0.7\,\text{V}, V_{\text{t}} = 0.5\,\text{V}$ (NMOS, typical): $V_{\text{ov}} = 0.2\,\text{V} \Rightarrow I_{\text{D}} \approx 5.3\,\mu\text{A}$; with $V_{\text{GS}} = 1.2\,\text{V}$: $V_{\text{ov}} = 0.7\,\text{V} \Rightarrow I_{\text{D}} \approx 62\,\mu\text{A}$.
(*Use these to check your calculator and region pick.*)

Gotcha

For PMOS, don't copy numbers blindly—carry the sign convention or switch to magnitudes consistently.

5) Parasitics (why delay shows up)

What always exists:

- **Gate capacitance C_g:** scales with active area ($W \times L$).
- **Overlap caps C_{gs}, C_{gd}:** from gate overlap over S/D; *independent of* L, roughly $\propto W$ ($C_{gs} \approx C_{ol}\,W$).
- **Diffusion** resistance/capacitance at S/D junctions.

Checklist

Delay intuition: $t_{pd} \sim R_{\text{drive}}\big(C_g + C_{\text{overlap}} + C_{\text{load}}\big)$. Wider $W \downarrow R$ but $\uparrow$ overlap caps—don't over-width tiny drivers into long wires.

6) Latch-up (and how we avoid magic smoke)

CMOS wells + substrate form a parasitic **SCR (PNP+NPN)** path. If triggered, it creates a low-resistance path from V_{DD} to GND and can destroy the chip.

Fix in practice: tub/well ties — tie n-well to V_{DD} and p-sub/p-well to GND with enough density (low impedance) to kill the gain loop. Guard rings and spacing rules help too.

Gotcha

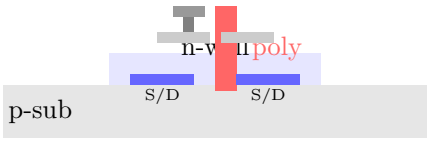
Latch-up is rare in modern flows if you follow rules—but if it happens, it's catastrophic. Respect the well-tie density rules.

7) What you might be asked to sketch (and why)

1. **Via M1↔M2:** shows vertical connection and via stud.
2. **Poly↔n-diff via:** contact from poly to diffusion through contact/via.

3. **PMOS cross-section:** p-channel in n-well; label S/D/G and the n-well tie to V_{DD}.

Tiny TikZ cartoons (not to scale; conceptual only)



(PMOS in n-well with poly gate; conceptual only.)

8) Design patterns you'll reuse

8A) Classify the region fast

1. Compute V_{ov}.
2. Compare V_{DS} vs. V_{ov} to pick linear vs. saturation.

8B) Size a PMOS for $m\times$ NMOS current (linear region)

1. Assume same $|V_{\text{GS}}|, |V_{\text{DS}}|, |V_{\text{t}}|$ magnitudes (signs differ for PMOS).
2. Set $|I_{\text{D}}|_p = m\,|I_{\text{D}}|_n$ using the *linear* equations.
3. Solve for $\left(\frac{W}{L}\right)_p$ in terms of $\left(\frac{W}{L}\right)_n$ and $\left|\frac{k'_p}{k'_n}\right|$.
4. Expect a wider PMOS since $|k'_p| \ll k'_n$ in 180 nm.

8C) Delay tradeoffs you can feel

First order, $t_{pd} \propto R_{\text{drive}}\,(C_g + C_{\text{overlap}} + C_{\text{load}})$. Increasing W reduces R *but* increases overlaps and input capacitance seen by the previous stage. Pick W for the real downstream load/wire.

9) Common pitfalls (and how to dodge them)

- Mixing carriers vs. conventional current (NMOS: electrons; current D→S. PMOS: holes; current S→D).
- Forgetting the λ grid when sketching—always annotate $3\lambda/2\lambda$ once.
- Using the wrong region formula—always test V_{DS} vs. V_{ov} first.

10) Formula card (grab-and-go)

$$\textbf{Linear:}\quad I_{\text{D}} = k'\left(\frac{W}{L}\right)\left[(V_{\text{GS}} - V_{\text{t}})V_{\text{DS}} - \tfrac{1}{2}V_{\text{DS}}^2\right]$$

$$\textbf{Sat:}\quad I_{\text{D}} = \tfrac{1}{2}k'\left(\frac{W}{L}\right)(V_{\text{GS}} - V_{\text{t}})^2$$

$$\textbf{180 nm cheats:}\quad k'_n \approx 170\ \mu\text{A/V}^2,\quad k'_p \approx -30\ \mu\text{A/V}^2,\quad V_t \approx \pm 0.5\ \text{V},\quad W/L_{\min} = 1.5$$

11) Glossary (fast)

- λ: half-min feature; your sketch ruler.
- via: vertical interconnect between metals.
- well/tub tie: n-well$\rightarrow V_{DD}$, p-sub/p-well$\rightarrow$GND to prevent latch-up.

Appendix: Practice (unsolved; bring to class)

A) Cross-sections

Sketch carefully and label layers/terminals:

1) Metal1 $\leftrightarrow$ Metal2 via (show dielectric and stud).
2) Poly $\leftrightarrow$ n-diffusion via (contact stack).
3) PMOS in n-well with S/D/G labels and well tie to V_{DD}.

B) PMOS Id–Vds curves

Plot $|I_{\mathrm{D}}|$ vs. $|V_{\mathrm{DS}}|$ for *minimum* PMOS at $V_{GS} = -0.6, -0.9, -1.2\,\mathrm{V}$; assume $V_t = -0.5\,\mathrm{V}$. Mark the linear/sat boundary $|V_{\mathrm{DS}}| = |V_{\mathrm{ov}}|$ on each curve.

C) PMOS sizing vs. NMOS (linear region)

With the same terminal magnitudes and NMOS at $W/L_{\mathrm{min}} = 1.5$, choose $(W/L)_p$ so $|I_{\mathrm{D}}|_p = 2\,|I_{\mathrm{D}}|_n$. Give the algebra in terms of $\left|k'_p/k'_n\right|$, then evaluate with the 180 nm cheats.

D) Quick region checks

For each case, compute V_{ov} and state the operating region of an *NMOS* at $W/L = 1.5$:

1. $V_{\mathrm{GS}} = 0.8\,\mathrm{V}, V_{\mathrm{t}} = 0.5\,\mathrm{V}, V_{\mathrm{DS}} = 0.1\,\mathrm{V}$
2. $V_{\mathrm{GS}} = 1.2\,\mathrm{V}, V_{\mathrm{t}} = 0.5\,\mathrm{V}, V_{\mathrm{DS}} = 0.8\,\mathrm{V}$

End of notes — bring these to class; fill the practice sections there.