Homework 4 Solution

Problem 1: What is the simplest SOP and POS expressions for $F = \Sigma_{A,B,C}(0, 1, 3, 4, 6) + D(2, 5)$, where "D" represents "Don't care"; see the K-map of F below.

		A'B'	A'B	AB	AB'
		0,0	**0,1**	**1,1**	**1,0**
C'	**0**	1	X	1	1
C	**1**	1	1	0	X

Answer:

		A'B'	A'B	AB	AB'
		0,0	**0,1**	**1,1**	**1,0**
C'	**0**	1	X	1	1
C	**1**	1	1	0	X

C'

A'

The simplest SOP: F = A' + C'

		A'B'	A'B	AB	AB'
		0,0	**0,1**	**1,1**	**1,0**
C'	**0**	1	X	1	1
C	**1**	1	1	0	X

A' + C'

The simplest POS: F = A' + C'

Problem 2: Sketch the outputs Q and QN (aka, draw the output waveforms for Q and QN) of an SR-Latch (the basic latch) of the type shown in Figure 1 for the input waveforms shown below. Assuming that initially Q=0 and QN=1. In your solution, please include the waveforms of R and S so that the alignment between inputs and outputs is clear.

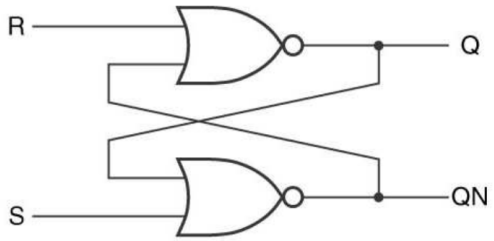
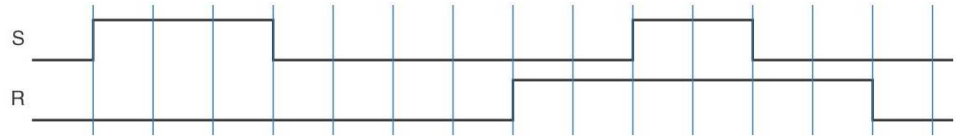
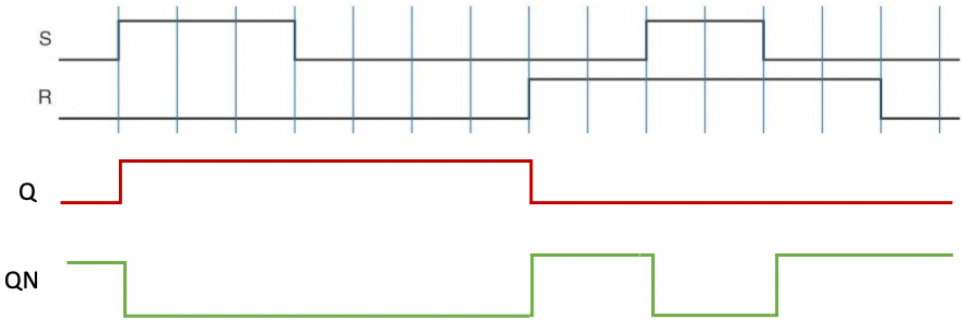


Figure 1: Circuit of the SR-Latch



Answer:



Problem 3: For the circuit in Figure 2, please draw the waveforms for Q_a, Q_b, and Q_c given the timing diagrams of Clock and D signals in Figure 3, where the initial values of Q_a, Q_b, and Q_c are zeros.

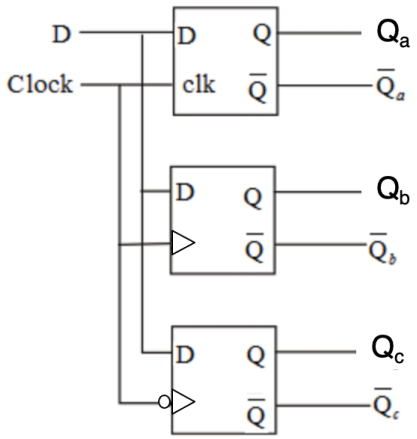


Figure 2

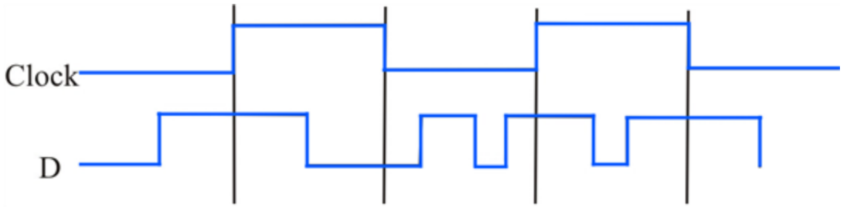
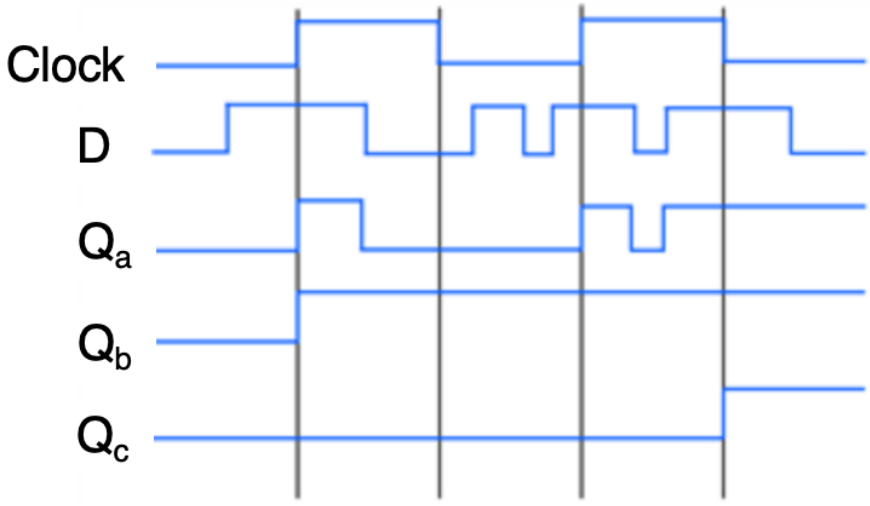


Figure 3

Answer:



Problem 4: Please find the state table for the state diagram in Figure 4. What is the minimum number of states in the state table? Does the state diagram represent a Mealy or Moore FSM?

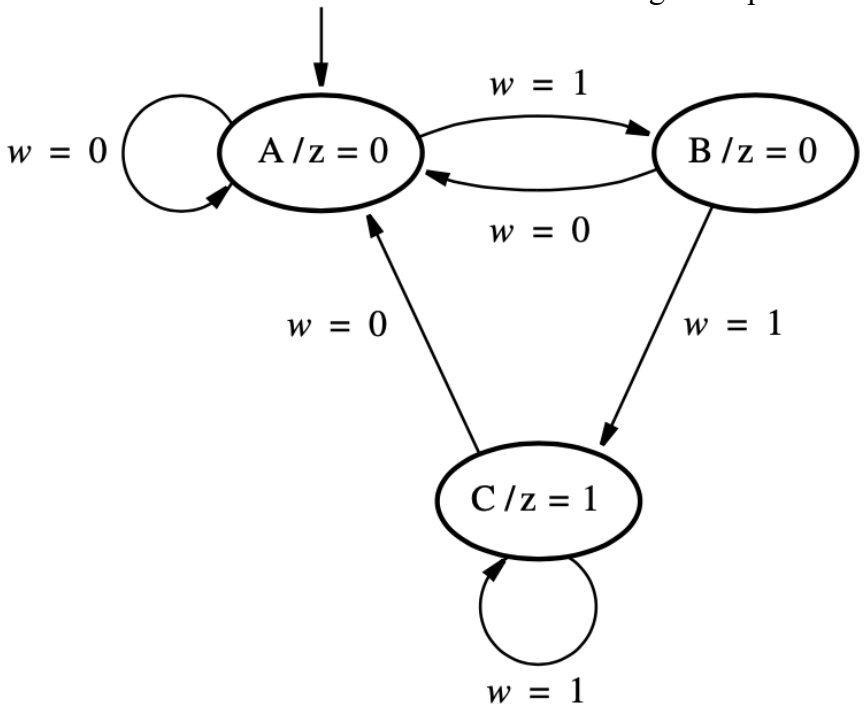


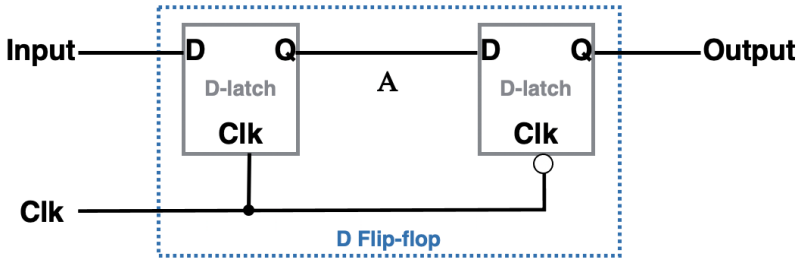
Figure 4

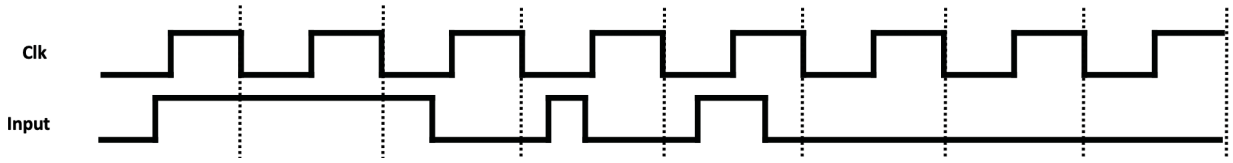
Answer:

The state table is as follows. The minimum number of states is 3 as there are no equivalent states. The state diagram represents a Moore machine as the output z depends only on the current state.

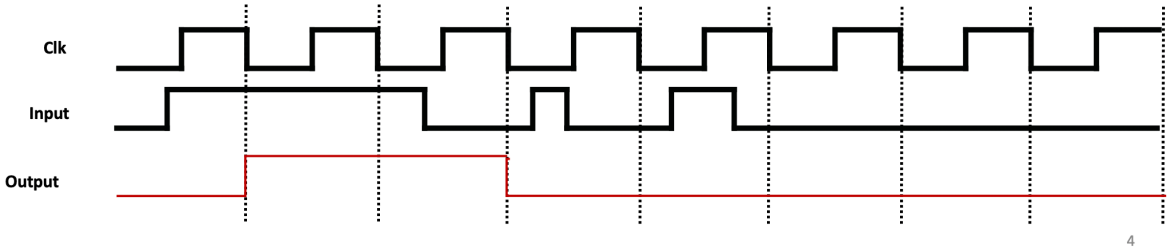
Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	A	B	0
B	A	C	0
C	A	C	1

Problem 5: Sketch/draw the Output waveform of a D Flip-flop for the input waveforms shown below. Assuming that initially Output=0.

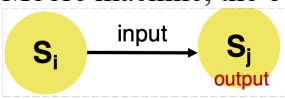




Answer:



Problem 6: Draw a state diagram for the Moore state machine described by Table 1. Hint: for Moore machine, the output depends only on the current state and an example of state transition is



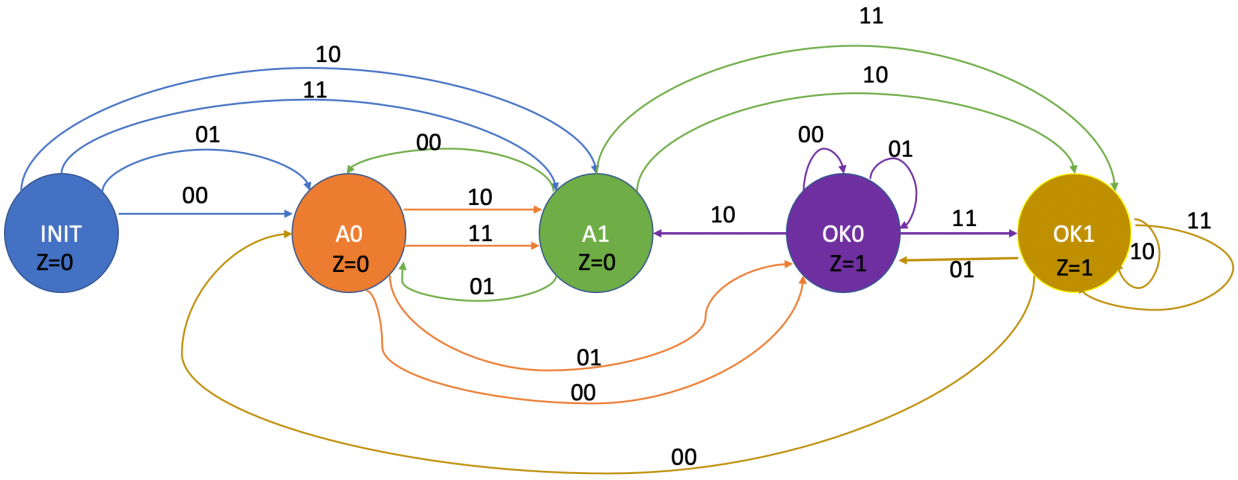
where S_i and S_j are the starting and ending states of such a transition.

Current State	Next State Inputs A and B				Output Z
	00	01	11	10	
INIT	A0	A0	A1	A1	0
A0	OK0	OK0	A1	A1	0
A1	A0	A0	OK1	OK1	0
OK0	OK0	OK0	OK1	A1	1
OK1	A0	OK0	OK1	OK1	1

Table 1

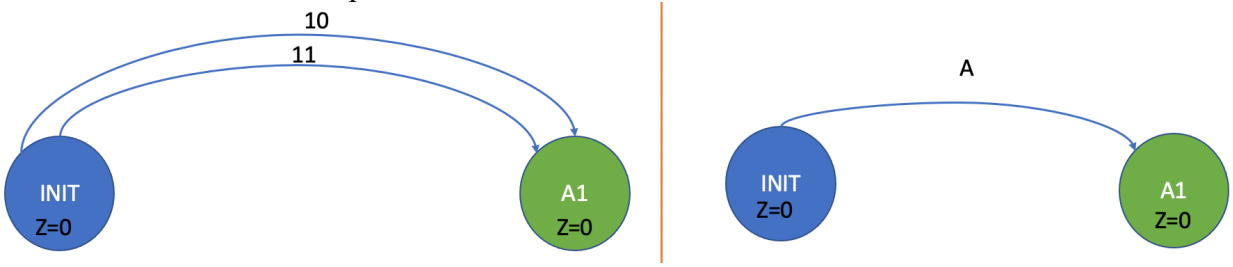
Answer:

Method 1: Directly draw each transition where the two numbers on top of each transition represent the values of A and B.



Method 2: Summarize all the cases of one state moving to another state by using a single transition, where the transition happens when the logic expression on top of each transition equals "1".

For example, if the current state is "INIT", when A=1, B=0 or A=1, B=1, the next state will be "A1", which means if A=1 regardless of B, the next state will be "A1". Thus, the following transitions on the LHS is equivalent to that in the RHS:



Finally, we have