CS 061 – Computer Organization — Winter - 2019

Quiz 4 – Thursday 2/14 — solution

1. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would force the character stored in R0 to upper case - i.e. convert a character stored in R0 from lower case into upper case, or preserve the case if it was upper case already (so 'a' would become 'A', and 'A' would remain unchanged).
Note: the LC-3 stores ASCII characters in the lower byte of a 16-bit word, with the upper byte set to zero.

a. and R0 with x0020
b. and R0 with x005F
c. or R0 with x0020
d. or R0 with x005F
e. xor R0 with x0020

2. A "gate delay" can be described as the time needed for the output of a gate to "settle" to its correct level after one of its inputs has been changed. The full-adder circuit we have designed would therefore result in a maximum gate delay of 3 units (including NOT gates).
How many units of gate delay would a 32-bit ripple-carry adder display (max)?

a. 3
b. 32
c. 96
d. 192
e. 4G

3. In order to overcome the gate delay problem of the simple ripple-carry adder circuit, we can design an adder with the following design improvement:

a. Make each full-adder smaller so as to reduce the gate delay of each.
b. "Recursively" pre-calculate the carry bit for each column.
c. Add an n-bit register to hold intermediate results, where n is the number of digits being added.
d. Use a multiplexer to distribute the carry bits to subsequent columns
e. Use a decoder to separately address each column of the addition.

4. How many separate locations can be addressed by a decoder circuit with 8-bit input?

a. 8 **b.** 16 **c.** 64 **d.** 256 **e.** 64k

5. Which of the condition code registers will be set following the operation `LDR R4, R2, #0;` given: `(R2) = x4000; Mem[x4000] = xA200`

a. N
b. Z
c. P
d. none of them: a load instruction does not affect the condition code registers

6. You have to implement a digital circuit module that can perform either of two possible operations:
output = a + b; or output = a + c
where a, b, c and output are all 16-bit 2's comp. numbers, and the operation + is 2's comp. addition *(not OR).*
Which of the following circuits would you use to make the selection between inputs b and c?

a. Full adder
b. Multiplexer
c. Decoder
d. Multi-input and gate
e. Direct Memory Access circuit

7. What is the total memory available to a microprocessor whose ISA specifies 18-bit addressing and word-addressability, given a word size of 32 bits?

a. 18 kbytes
b. 64 kbytes
c. 256 kbytes
d. 512 kbytes
e. 1 Mbytes

8. How do we turn 8 separate gated D-latches into a single 8-bit register?

a. connect their inputs together
b. connect their outputs together
c. connect them to an 8-bit bus
d. connect their Write-Enable lines together
e. mount them next to each other

The next 2 questions use the following settings:

```
(R4) = xA600, (R6) = xA500
DATA   .Fill xA400
Address xA400 contains value xA600
Address xA500 contains value x0000
Address xA600 contains value xFFFF
```

9. What value will be stored in R4 following execution of the instruction :

```
LDI    R4,  DATA
```

a. xA400
b. xA500
c. xA600
d. xFFFF
e. x0000

10. What value will be stored in R5 following execution of the instruction :

```
LDR    R5,  R6, x0
```

a. xA400
b. xA500
c. xA600
d. xFFFF
e. x0000