EECS 168 Introduction to VLSI Design

Dr. Sheldon Tan

www.ece.ucr.edu/~stan

Email: stan@ece.ucr.edu

Topics

- Basic fabrication steps.
- Transistor structures.
- Basic transistor behavior.
- Latch up.

Our technology

- We will study a generic 180 nm technology.
  - Assume 1.2V supply voltage.
  - $\lambda = 90nm$ (half of the minimum feature)
- Parameters are typical values.
- Parameter sets/Spice models are often available for 180 nm, harder to find for 90 nm.
- For labs, we have both 90nm and 28nm physical design kit (PDK) from Synopsys.

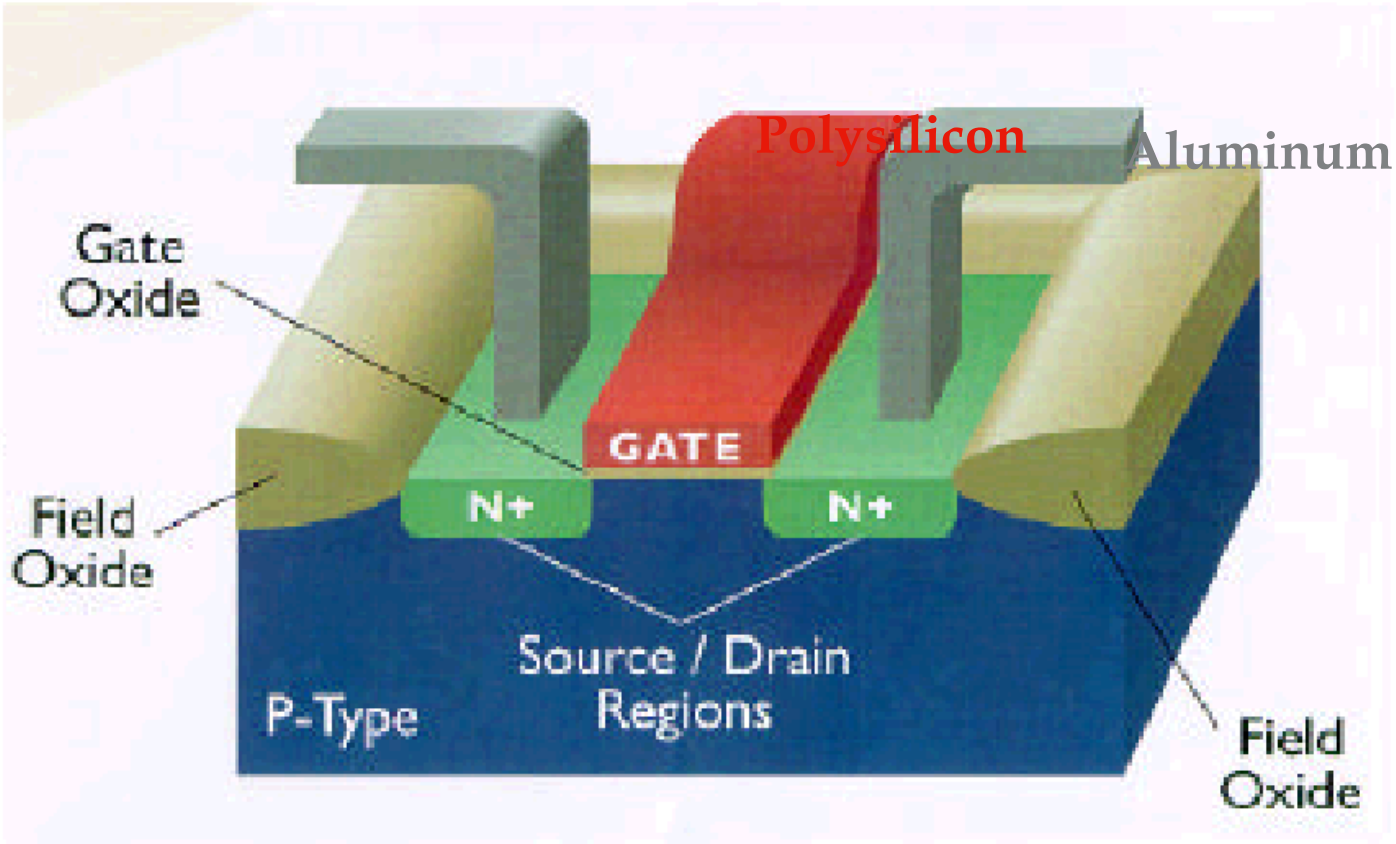
Fabrication services

- Educational services:
  - U.S.: MOSIS (MOS Implementation Service)
  - EC: EuroPractice
  - Taiwan: CIC
  - Japan: VDEC
- Foundry = fabrication line for hire.
  - Foundries are major source of fab capacity today.

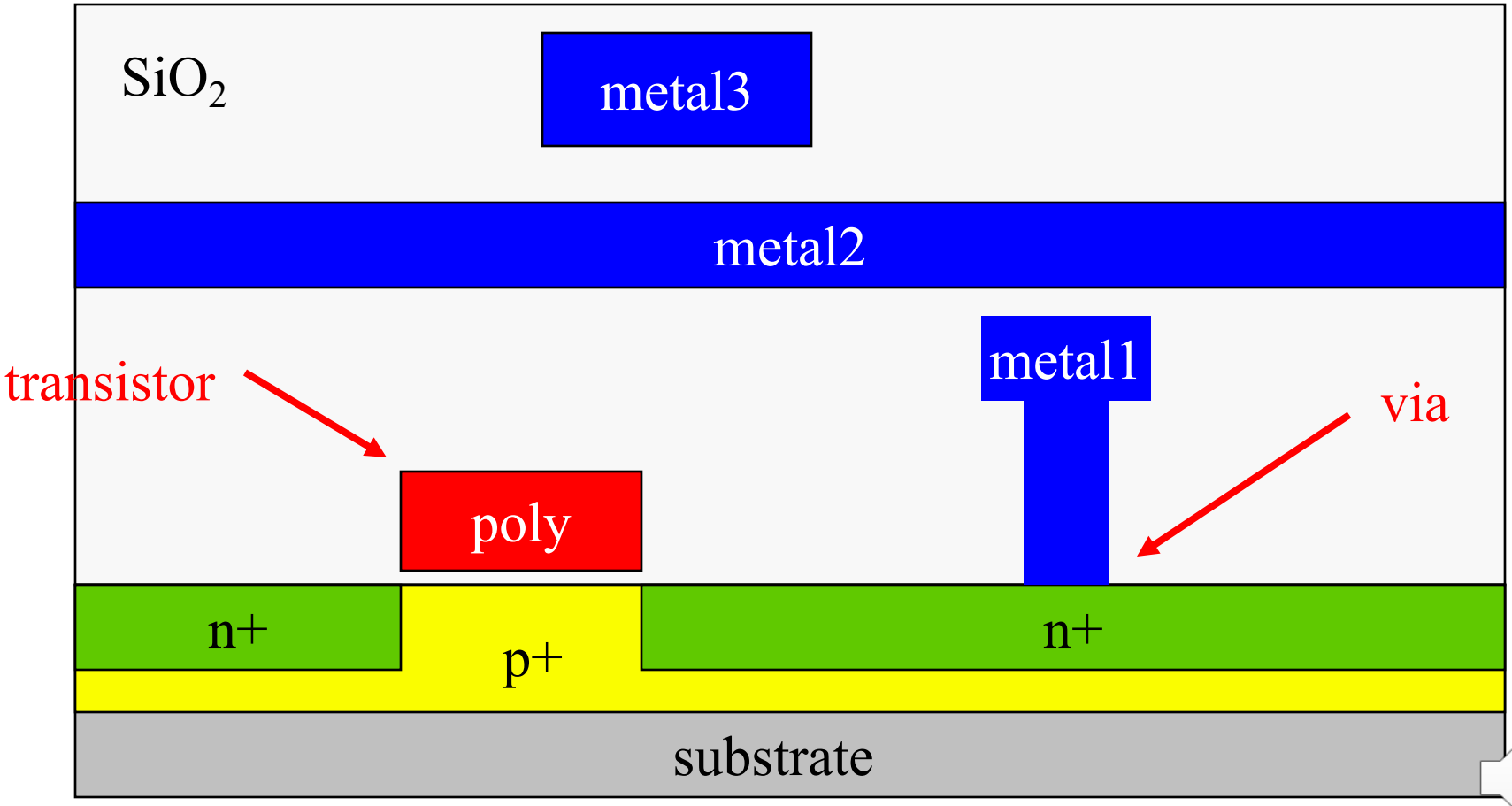
Fabrication processes

- IC built on silicon substrate:
  - some structures diffused into substrate;
  - other structures built on top of substrate.
- Substrate regions are doped with n-type and p-type impurities. (n+ = heavily doped)
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum or copper (metal).
- Silicon dioxide (SiO_2) is insulator.

The MOS Transistor



Simple cross section



Photolithography

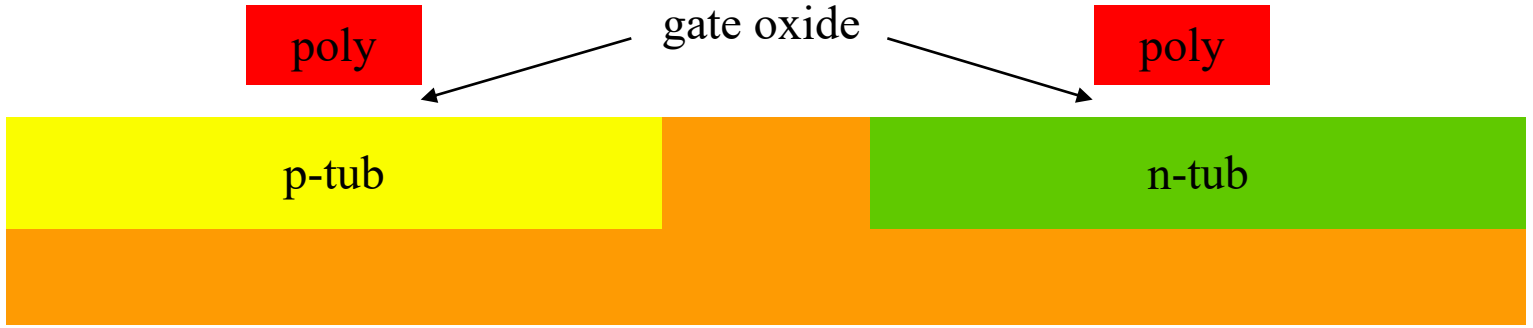
Mask patterns are put on wafer using photo-sensitive material:

Process steps

First place tubs to provide properly-doped substrate for n-type, p-type transistors:

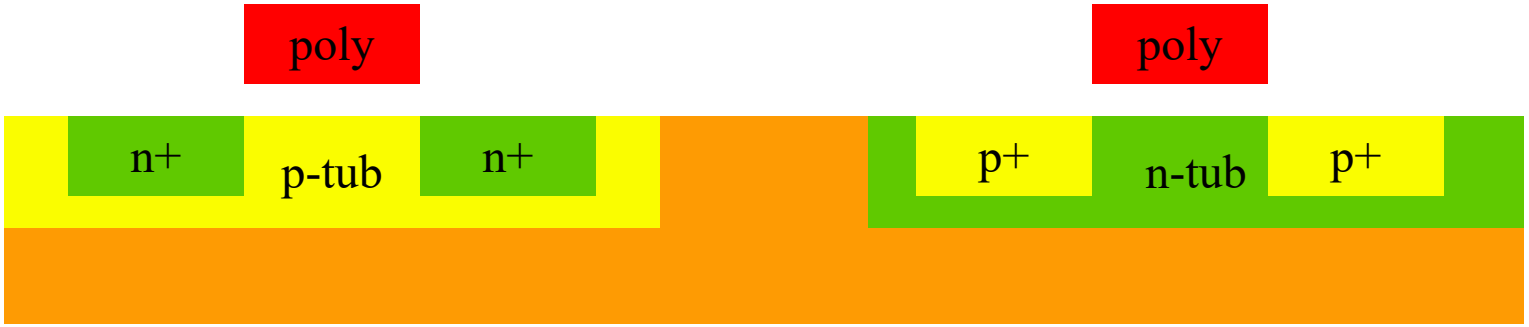
Process steps, cont'd.

Pattern polysilicon before diffusion regions:



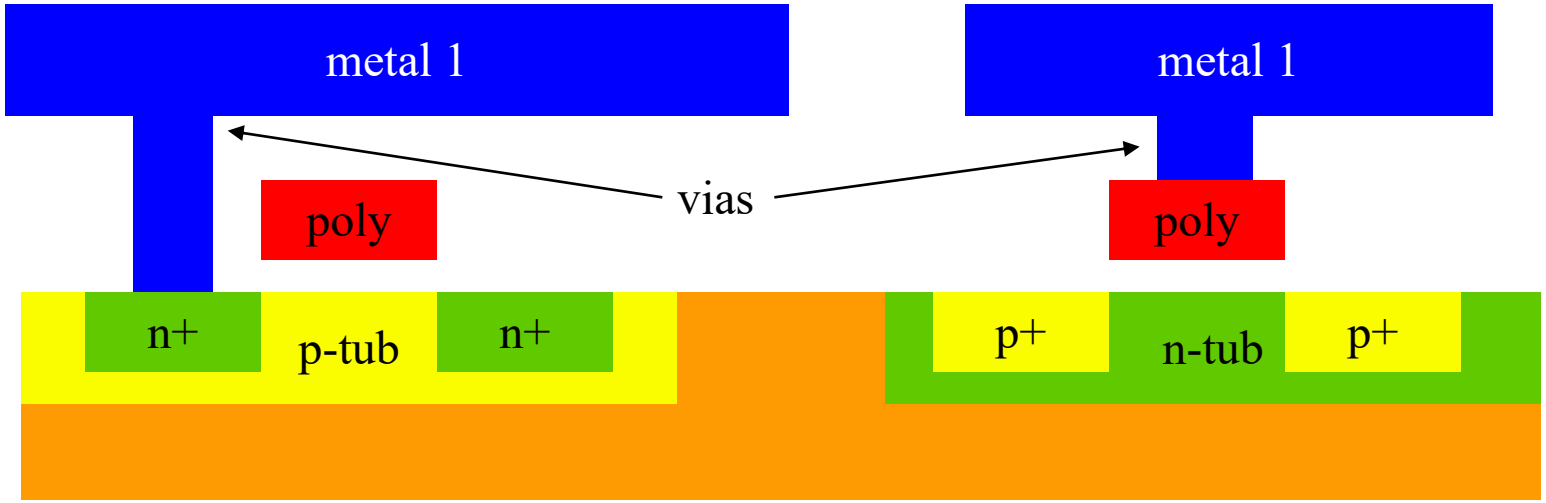
Process steps, cont'd

Add diffusions, performing self-masking:



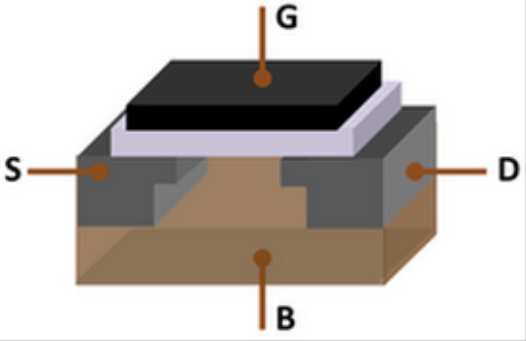
Process steps, cont'd

Start adding metal layers:

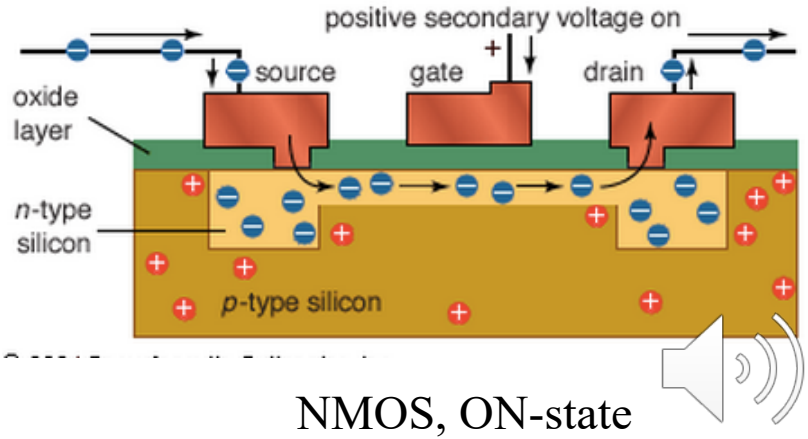


MOSFET

- **MOSFET**
  - metal-oxide-semiconductor field transistor
- **N-type MOSFET (NMOS)**
  - Carrier: electrons (negative charge)
  - Carriers flow from source to drain
  - Current direction: drain to source
- **P-type MOSFET (PMOS)**
  - Carrier: holes (positive charge)
  - Carriers flow from source to drain
  - Current direction: source to drain



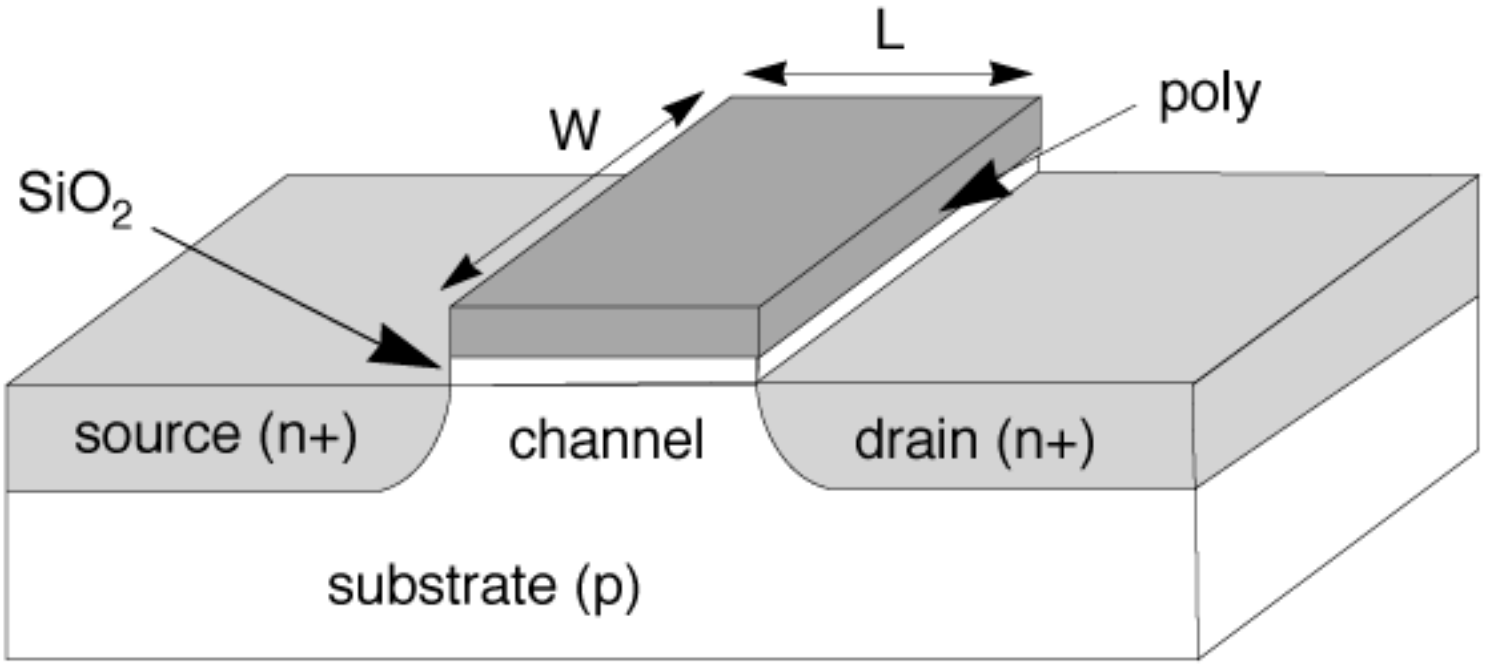
MOSFET showing gate (G), body (B), source (S) and drain (D) terminals. The gate is separated from the body by an insulating layer (white)



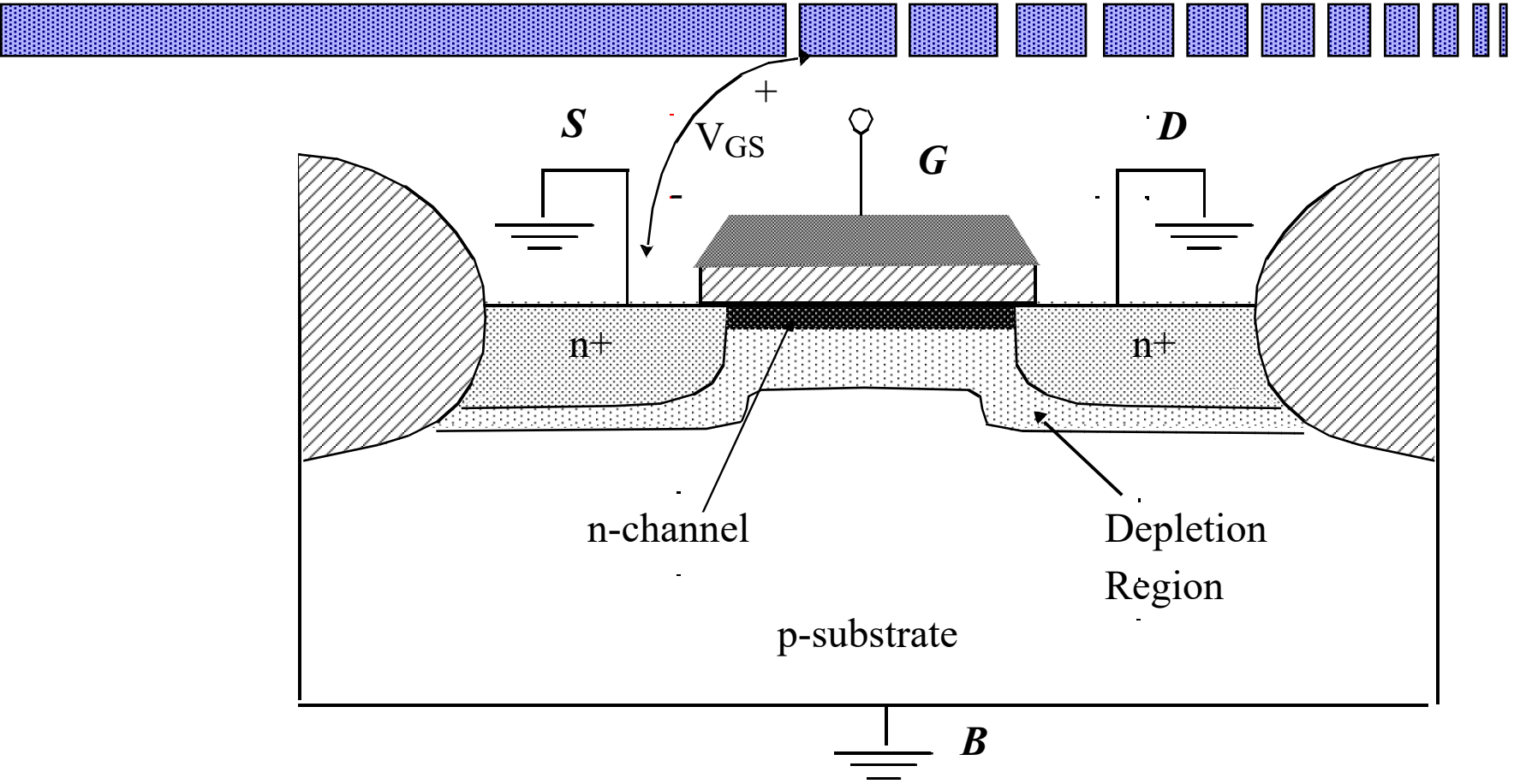
NMOS, ON-state

Transistor structure

n-type transistor:

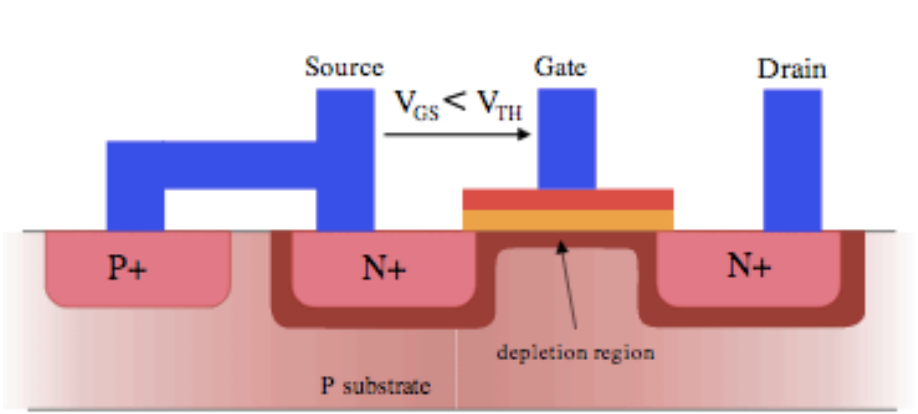


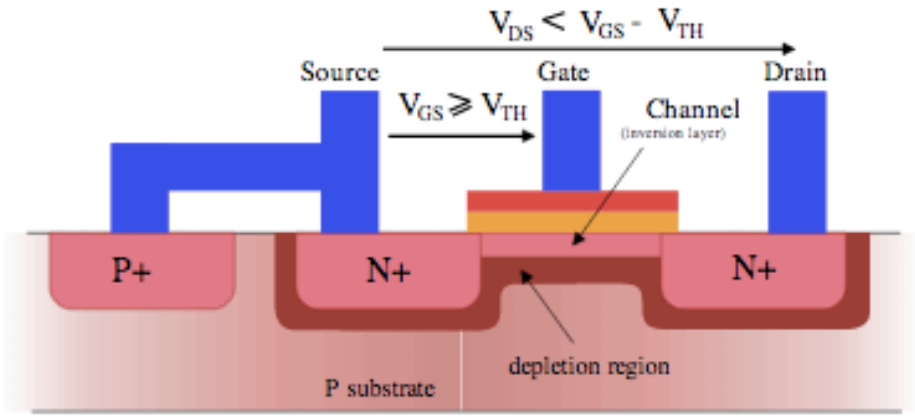
Threshold Voltage: Concept



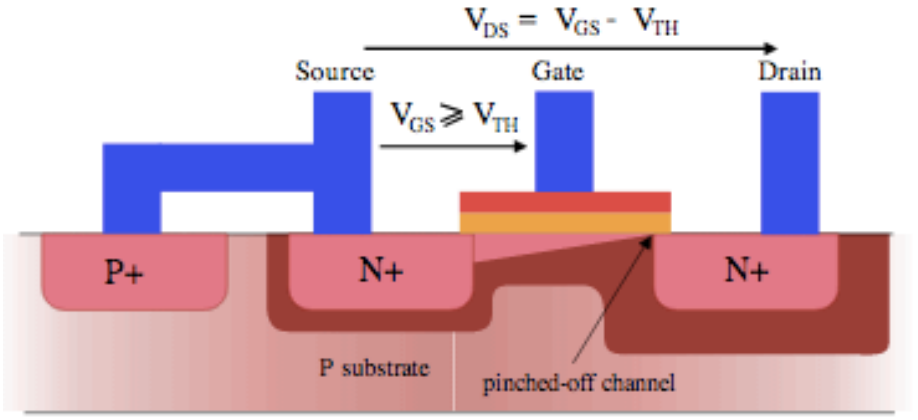
From Wikipedia

MOSFE Functioning

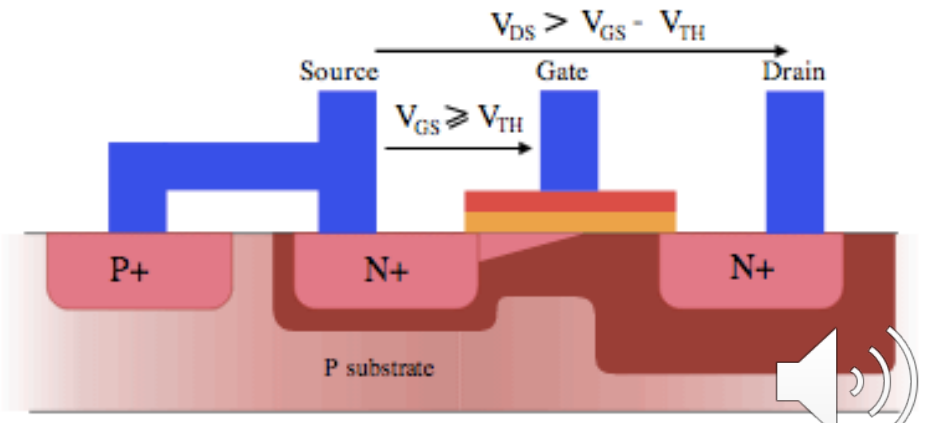




Linear operating region (ohmic mode)



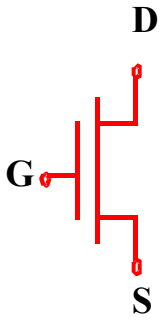
Saturation mode at point of pinch-off



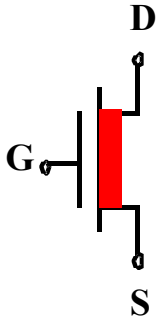
Saturation mode

NMOS

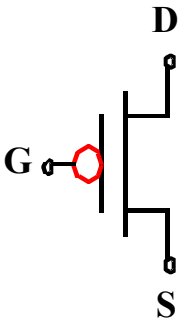
MOS Transistors - Types and Symbols



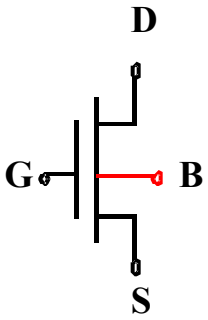
NMOS Enhancement



NMOS Depletion

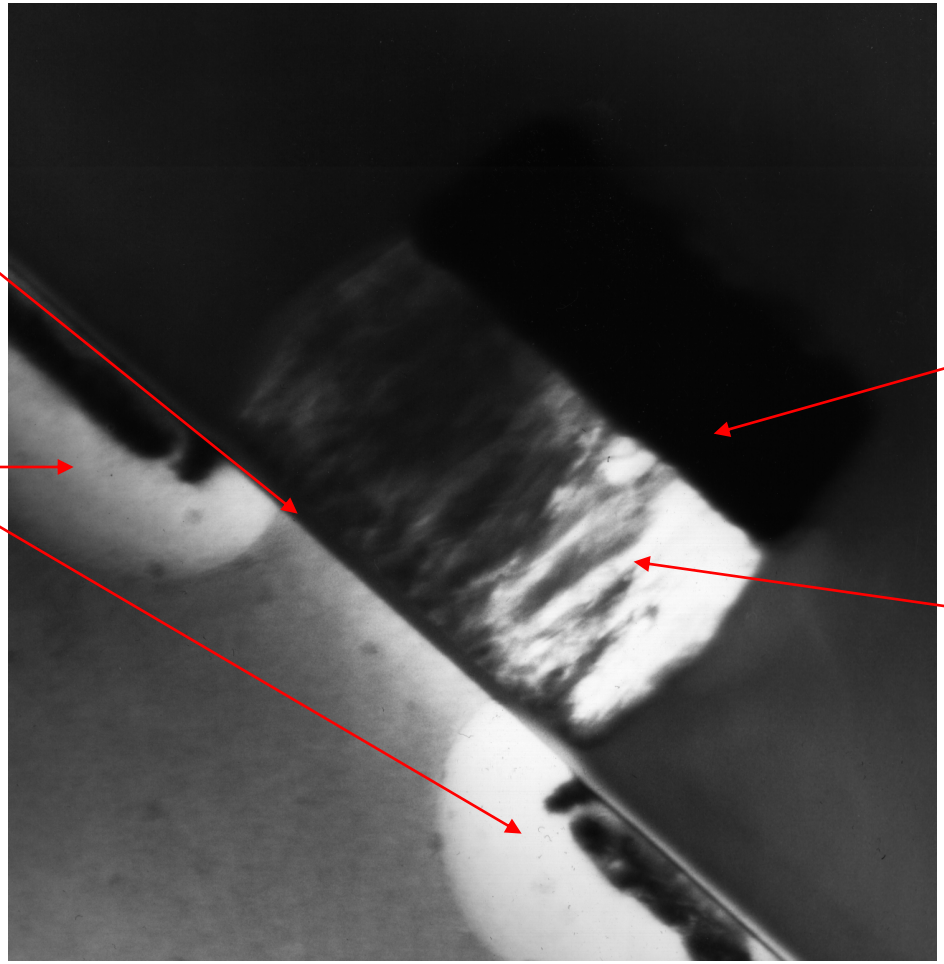


PMOS Enhancement



NMOS with Bulk Contact

0.25 micron transistor (Bell Labs)

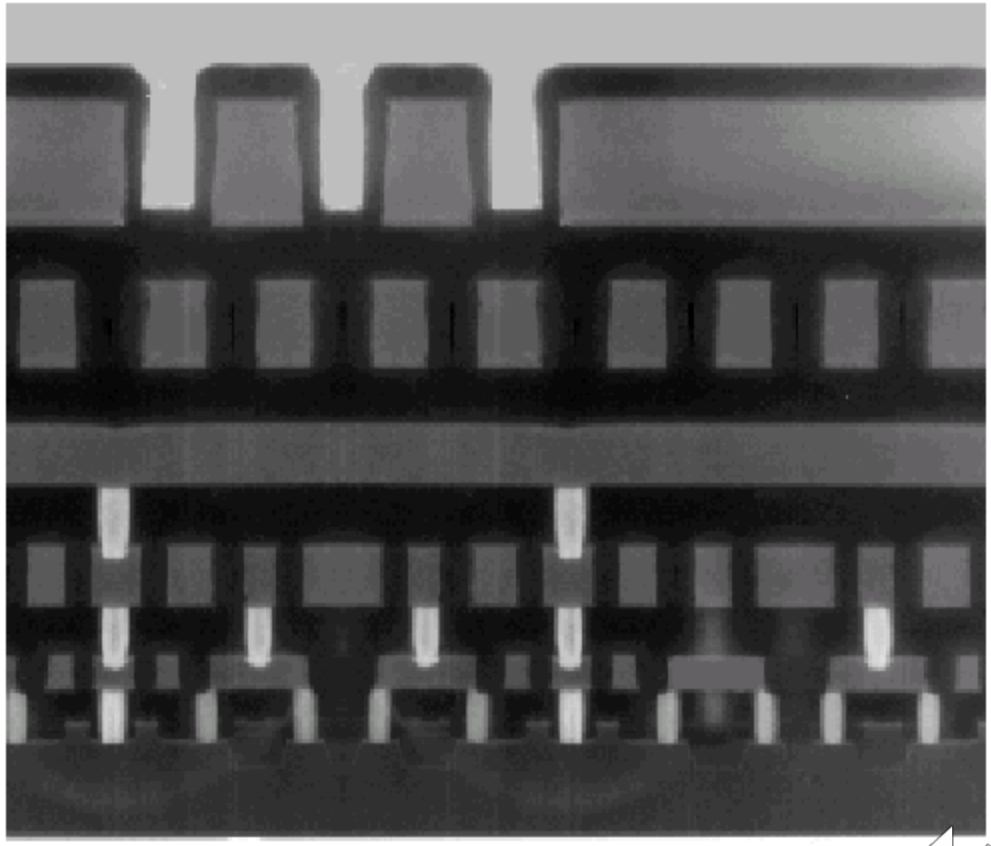


Example: Intel 0.25 micron Process

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

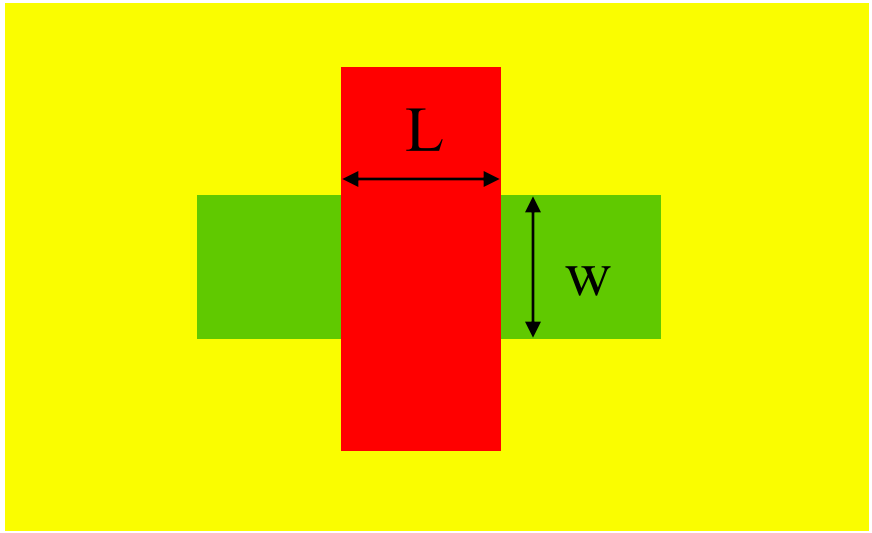
LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio



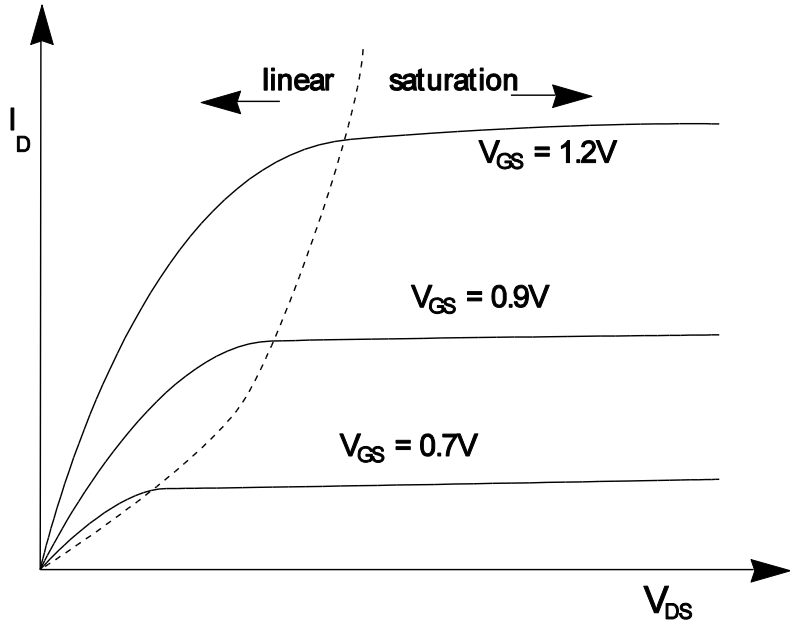
Transistor layout

n-type (tubs may vary):



Drain Current Characteristics

NMOS



- Linear region ($V_{ds} < V_{gs} - V_t$):
  - $I_d = k'(W/L)[(V_{gs} - V_t) V_{ds} - 0.5 V_{ds}^2]$
- Saturation region ($V_{ds} >= V_{gs} - V_t$):
  - $I_d = 0.5k'(W/L)(V_{gs} - V_t)^2$
  - Drain current independent of V_{ds}

PMOS: Similar to NMOS, but Vgs, Vds, Vth, Id in the opposite direction (for example, Vgs_pmos = -Vgs_nmos)

Drain current

- Linear region ($V_{ds} < V_{gs} - V_t$):
  - $I_d = k' (W/L)((V_{gs} - V_t)V_{ds} - 0.5 V_{ds}^2)$
- Saturation region ($V_{ds} >= V_{gs} - V_t$):
  - $I_d = 0.5k' (W/L)(V_{gs} - V_t)^2$

180 nm transconductances

Typical values:

- n-type:
  - $k_n' = 170\ \mu A/V^2$
  - $V_{tn} = 0.5\ V$
  - Minimum transistor W = 3λ, L=2λ
- p-type:
  - $k_p' = -30\ \mu A/V^2$
  - $V_{tp} = -0.5\ V$
  - Minimum transistor W = 3λ, L=2λ

Current through a transistor

Use 180 nm parameters. Let W/L = 3/2.
Measure at boundary between linear and saturation regions.

- $V_{gs} = 0.7V$:

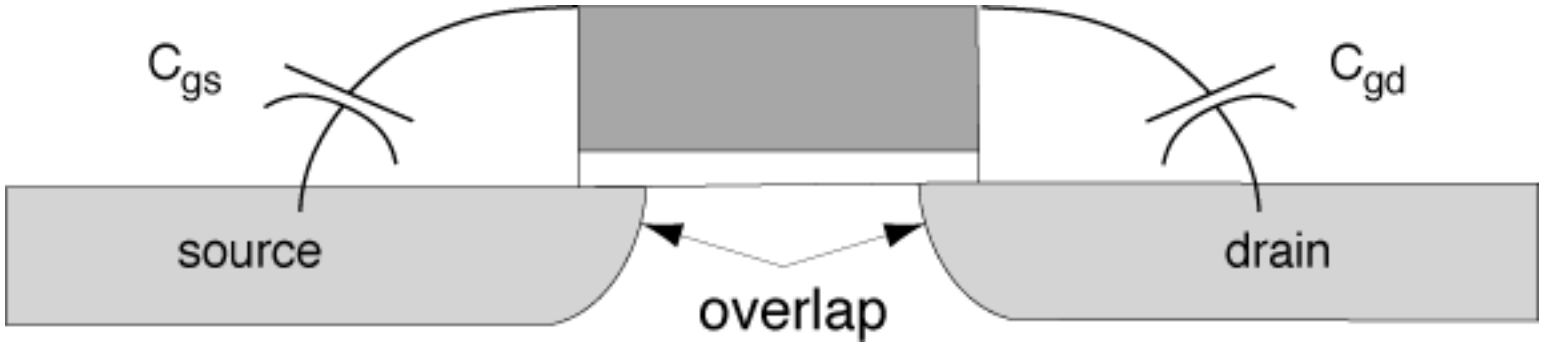
  $I_d = 0.5k'(W/L)(V_{gs}-V_t)^2 = 5.3\ \mu A$

- $V_{gs} = 1.2V$:

  $I_d = 62\ \mu A$

Basic transistor parasitics

- Gate to substrate, also gate to source/drain.
- Source/drain capacitance, resistance.



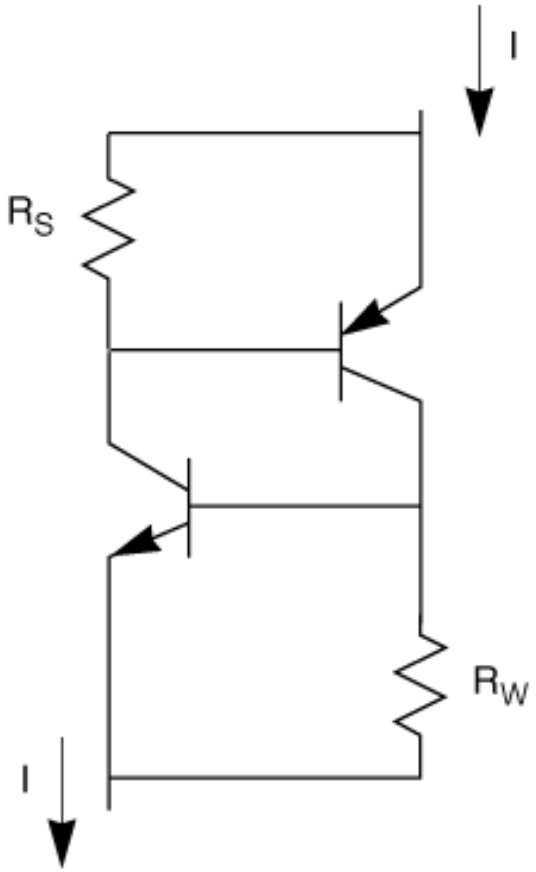
Basic transistor parasitics, cont'd

- Gate capacitance C_g. Determined by active area.
- Source/drain overlap capacitances C_{gs}, C_{gd}. Determined by source/gate and drain/gate overlaps. Independent of transistor L.
  - $C_{gs} = C_{ol} W$
- Gate/bulk overlap capacitance.

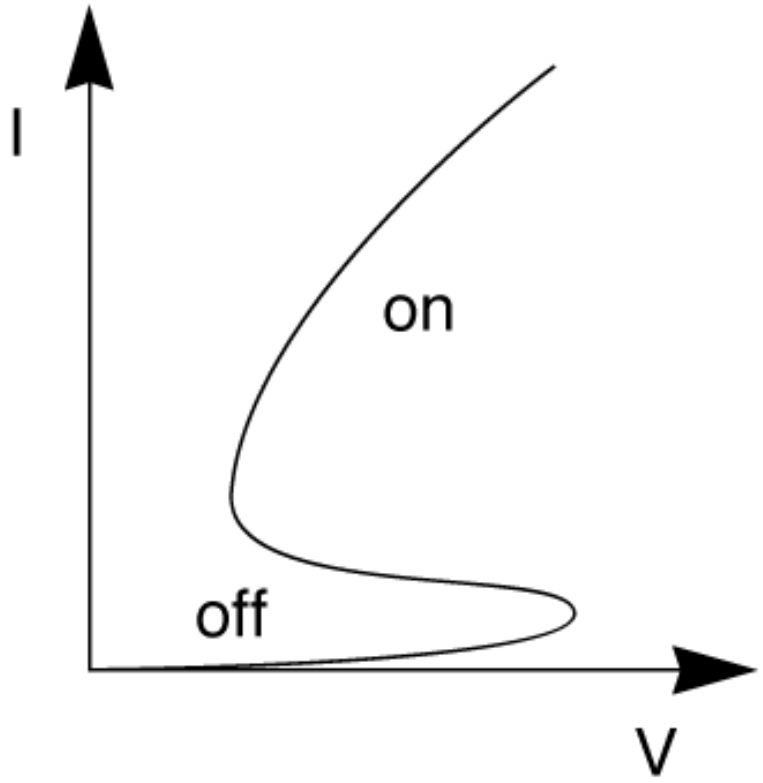
Latch-up

- CMOS ICs have parastic silicon-controlled rectifiers (SCRs).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.
- Early CMOS problem. Can be solved with proper circuit/layout structures.

Parasitic SCR

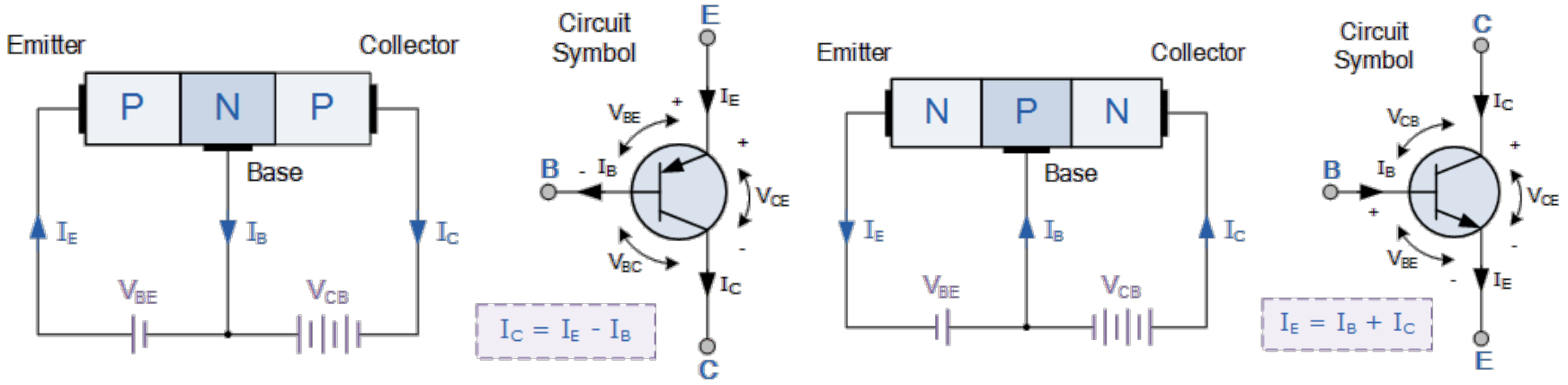


circuit

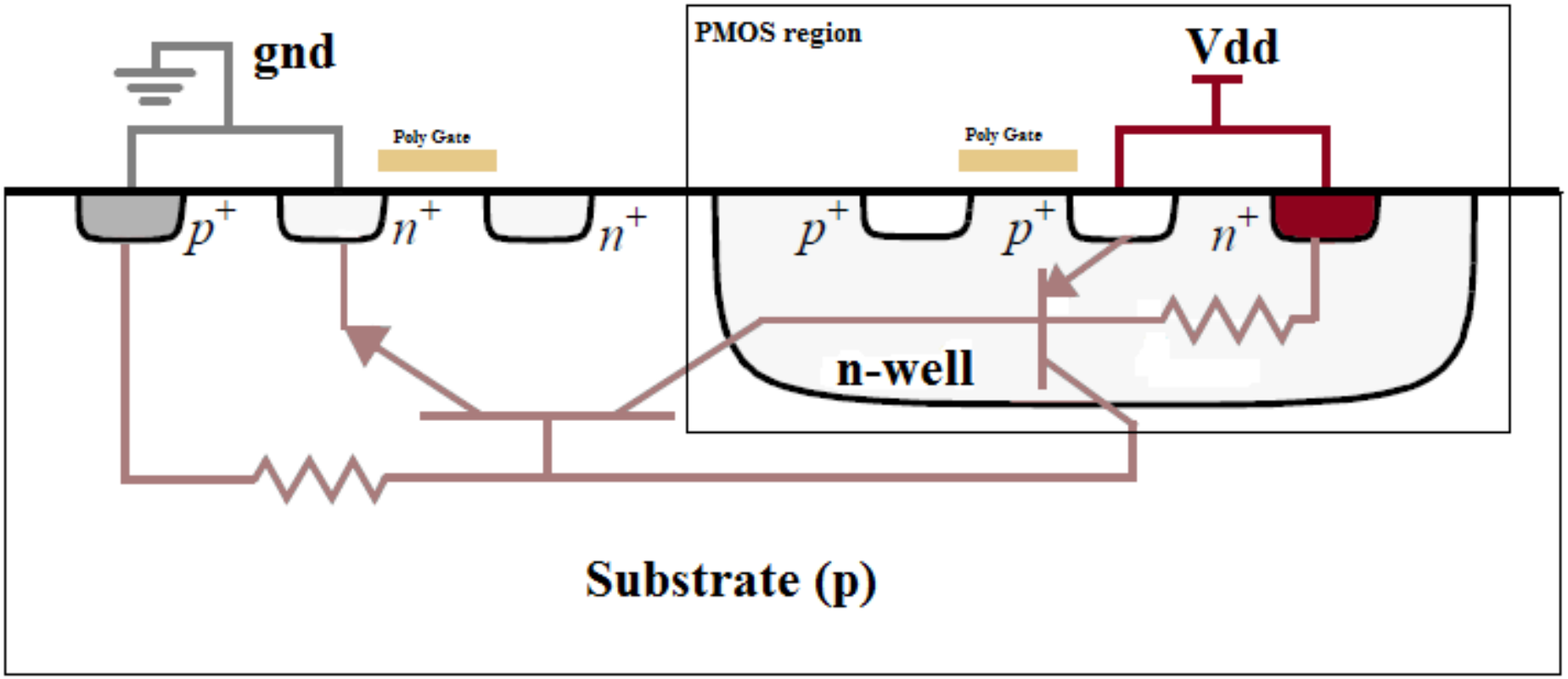


I-V behavior

PNP and NPN Bipolar transistors

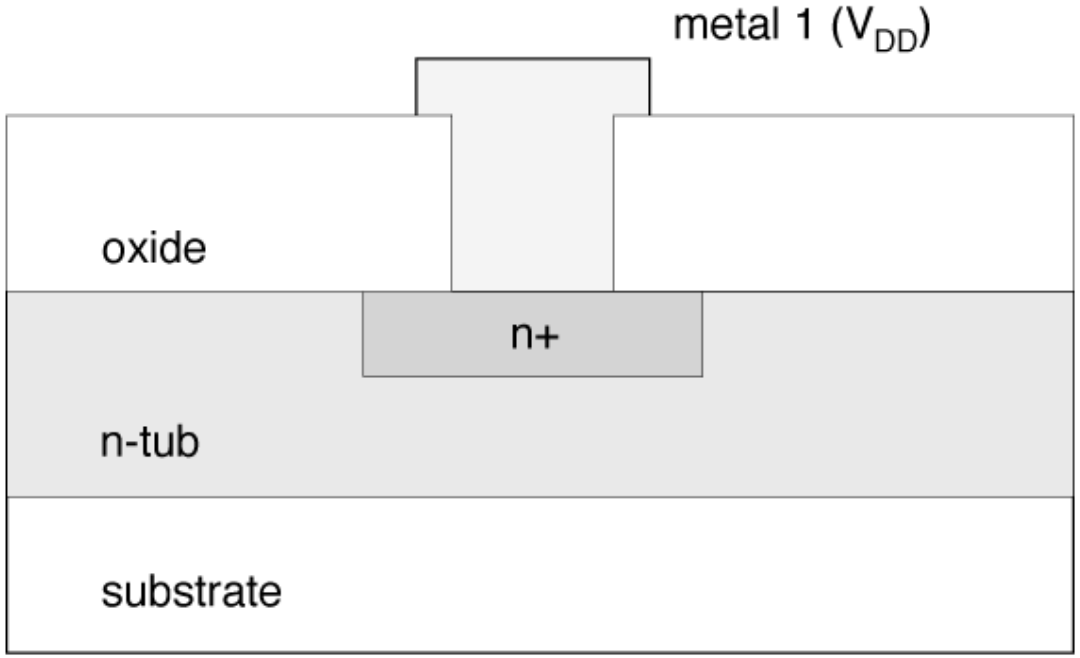


Parasitic SCR structure

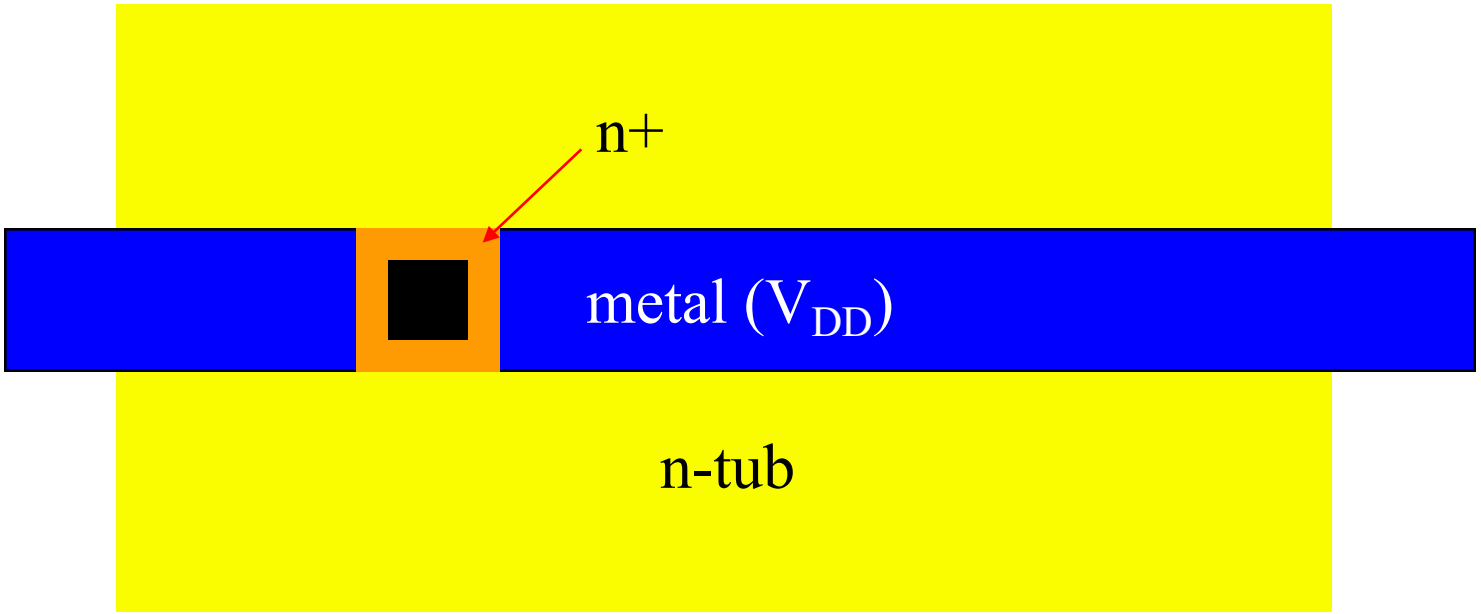


Solution to latch-up

Use tub ties to connect tub to power rail. Use enough to create low-voltage connection.



Tub tie layout



In lecture exercise

- Draw cross section of
  - (a) metal-1 to metal 2 by a via
  - (b) a poly to n-diffusion by a via
  - (c) A PMOS FET transistor and indicate source, drain and gate

In lecture exercise

- The minimum width definition
  - In this class, W = 3λ, L=2λ, so W/L = 3/2
  - NMOS, $k_n = 170\mu A/V^2$
  - PMOS, $k_p = -30\mu A/V^2$
- Plot the V_{ds} versus I_{ds} curve for a minimum PMOS transistor for V_{gs} = -0.6V, -0.9V, -1.2V (assume V_t = -0.5)
- What is the W/L is required to make drain current of a PMOS is twice of minimum NMOS (assume that both transistors have the same terminal voltages, but PMOS have opposite V_{gs}, V_{ds}, V_t of NMOS)? Assume that both transistors work in the linear region.