Cs061 example final-1 1

Data Oriented Introduction To Computing I (University of California Riverside)

Name (first last): _____ username (UCR netID): _____

CS 061-001 – Computer Org. & Assembly Language Example Final

Fill in your name/NetID on the front page, on the pages of Section II, and on the scratch page.

You may have on your desks ONLY this exam, your multiple choice answer sheet, writing implements, textbook, handwritten or printed notes, and your student ID.

You may NOT have electronic devices on your person.

The empty page at the end of the test is for scratch paper: **tear it off** and put your name on it and hand it in with your exam.

Section I (questions 1 to 25) is to be answered on your multiple choice bubble sheets;
Section II is to be answered on this exam.

When you have finished, hand in the exam, your multiple choice bubble sheet, and your scratch paper, and present your student ID.

Be sure to read each problem carefully and follow the directions.

Section I: Multiple choice

1. The von Neumann model of computing proposes (among other things) that
   a. all higher level computing languages are reducible to Machine language.
   b. the instruction set architecture of a microprocessor can be portable between machines.
   c. data and instructions can both be stored in the same memory.
   d. all computer information can be represented by a binary code.
   e. it can solve problems that all other computing models cannot

2. All control instructions in the LC-3 have one main step in common:
   a. They all use the ALU in reconstructing the required memory address
   b. They all reconstruct the required memory address in the same way
   c. They all write to the IR in the execution phase of the instruction cycle
   d. They all write to the PC in the execution phase of the instruction cycle
   e. They all write to the MDR in the execution phase of the instruction cycle

3. What data does the PSR contain?
   a. The current privilege level, the values of N, Z, and P, and the current priority level.
   b. The PC, the values of N, Z, and P, and the stack pointer
   c. the PC and all the General Purpose Registers
   d. The PC, MDR and IR
   e. the PC and the MCR (Machine Control Register)

4. What is the main difference between the JMP instruction and the JSRR instruction?
   a. The JMP does not back up the PC into R7 and the JSRR instruction does
   b. The JSRR does not back up the PC into R7 and the JMP instruction does
   c. JSRR uses the PC to calculate the effective address, and JMP uses a base register
   d. JMP uses the PC to calculate the effective address, and JSRR uses a base register
   e. There is no difference, JMP is a pseudo instruction for JSRR

5. Simplify the Boolean expression:
$a' \cdot b' \cdot c' \cdot d + a \cdot b' \cdot c' \cdot d + a' \cdot b \cdot c \cdot d' + a \cdot b \cdot c \cdot d'$
a. $b \cdot c$
b. $a \cdot b \cdot c + b \cdot c \cdot d$
c. $a \cdot b$
d. $a' \cdot b' \cdot c' \cdot d + a \cdot b' \cdot c' \cdot d + a' \cdot b \cdot c \cdot d' + a \cdot b \cdot c \cdot d'$
e. $b' \cdot c' \cdot d + b \cdot c \cdot d'$

6. Which of the following are two techniques used for I/O handling covered in this class?
a. Polling and Interrupt Driven
b. Pulling and Interruptions
c. Stacks and Queues
d. Operations and Control
e. None of these option

7. Which of the LC-3 instructions are called the data movement instructions and move data to and from registers to memory?
SELECT ALL OPTIONS THAT WOULD APPLY
a. LD, LDI, LDR
b. ST, STI, STR
c. LEA
d. TRAP
e. JSR(R)

ISA Specification
The next five questions refer to an ISA with the following specification:
- a word addressable memory;
- addressing is 24 bits (i.e. an address is a 24-bit value);
- word size is 16 bits (i.e. a standard word is a 16-bit value);
- an instruction is a single word.

8. How many memory locations can be addressed by this ISA?
a. 16 M
b. 64 M
c. 16 K
d. 64 K
e. 64 G

9. What is the total capacity of memory, in bytes?
a. 64 K Bytes
b. 128 K Bytes
c. 32 M
d. 64 K
e. 32 M Bytes

10. What is the addressability of this ISA?

a. 8 bits **c.** 28 bits **e.** None of the options
b. 16 bits **d.** 32 bits

11. What are the sizes of the PC and IR registers?

a. PC: 24 bits, IR: 16 bits **c.** PC: 8 bits, IR: 32 bits
b. PC: 16 bits, IR: 24 bits **d.** PC: 16 bits, IR: 16 bits
e. The size of both the PC and IR are indeterminable with the information given

12. What are the sizes of the MAR and MDR registers?

a. MAR: 24 bits, MDR: 16 bits **c.** MAR: 8 bits, MDR: 32 bits **e.** MAR: 16 bits, MDR: 16 bits
b. MAR: 16 bits, MDR: 24 bits **d.** MAR: 32 bits, MDR: 8 bits

13. What value in the KBSR means that new data is available for input from the keyboard?

a. KBSR = 1 **c.** KBSR[15] = 1 **e.** KBSR[14] = 1
b. KBDR[15] = 1 **d.** KBSR[14] = 0

14. What value is sent to the DR of the Register File when executing the TRAP instruction?

a. b111 **b.** b101 **c.** b011
d. The value stored in the trapvec8 part of the TRAP instruction format
e. None of the options

15. One control signal selects ZEXT(IR[7:0]) in the MARMUX. Which of the following instructions would use this control signal?

a. NOT **c.** ST, STI, & STR **e.** TRAP
b. LD, LDI, & LDR **d.** BR & JM

Instruction Formats

The next two questions refer to the following system:

A certain ISA has a 24-bit word size, uses single word (24-bit) instructions, has 32 opcodes, 64 registers, and 256 M of byte-addressable memory. One group of instructions in this ISA takes the form:

```
OPCODE | DESTINATION REGISTER | SOURCE REG. | Flag | IMMEDIATE VALUE
```

Or

```
OPCODE | DESTINATION REGISTER | SOURCE REG. 1 | Flag | SOURCE REG. 2
```

A single bit in the instruction ("Flag") is used to differentiate these two addressing modes.

Another group of instructions takes the form

```
OPCODE | SOURCE/DESTINATION REGISTER | PC OFFSET
```

Where PC Offset is the 2's complement "distance" from the current PC to the labeled location.

16. How many bits are required for addressing (i.e. what is the size, in bits, of a memory address)?

a. 32 bits
b. 30 bits
c. 28 bits
d. 31 bits
e. 16 bits

17. How will the bits in the instruction be distributed between opcode and operands? Answers are listed as bits for opcode / bits for operands

a. 4 bits / 20 bits
b. 4 bits / 28 bits
c. 5 bits / 19 bits
d. 5 bits / 27 bits
e. 6 bits / 26 bits

18. How many bits can be used to represent an immediate value as an operand?

a. 32 bits
b. 20 bits
c. 28 bits
d. 1 bit
e. 6 bits

19. How far (in memory locations) can the label be from an instruction that references the label, using the <opcode | register | pc offset> addressing mode?

a. +/- 256 K
b. +/- 128 K
c. +/- 16 k
d. +/- 32 K
e. +/- 4 K

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Section II

1. Given the data path of the LC-3, give a complete description of the JSR instruction, as outlined in the following questions

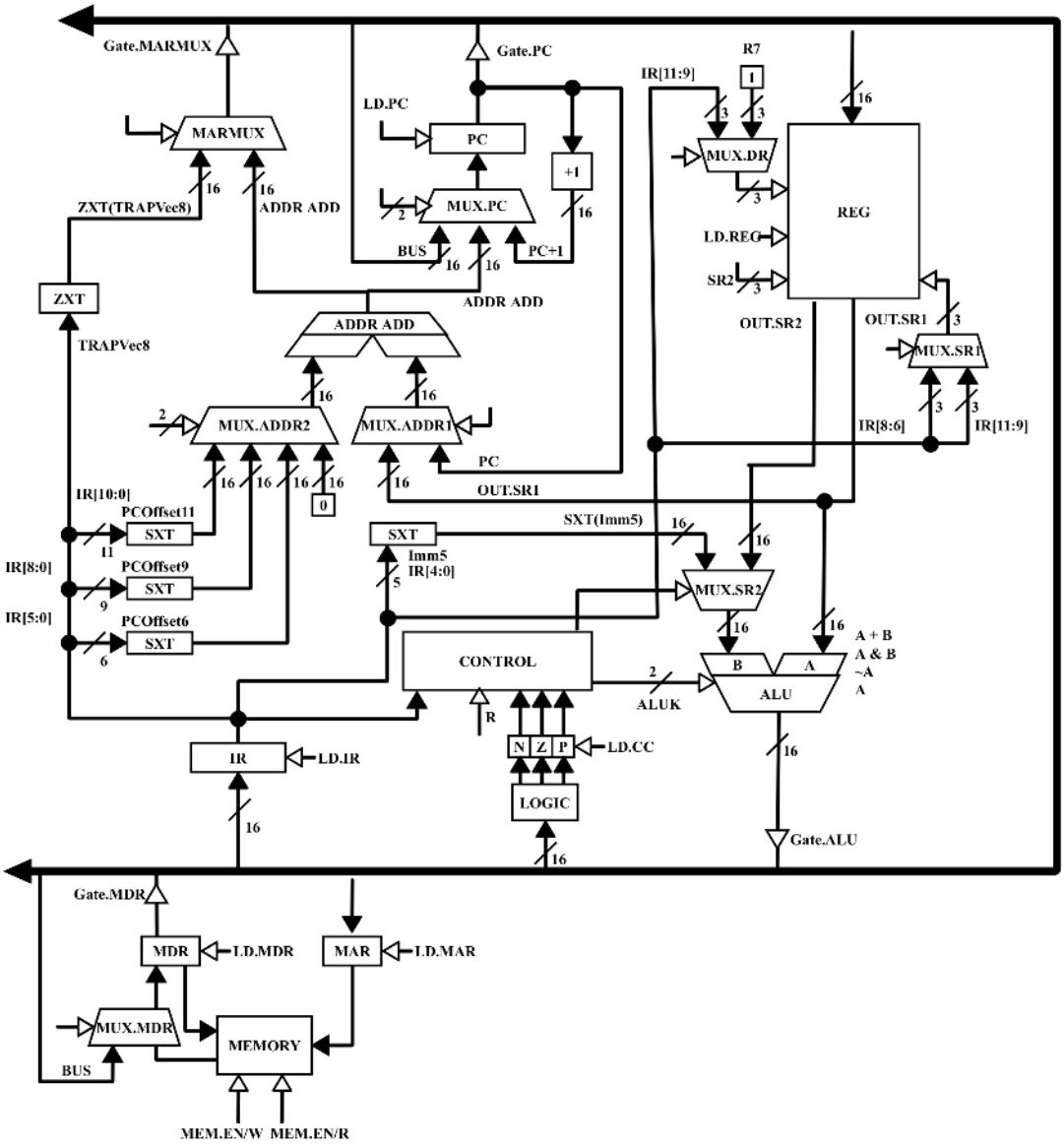
```
x3400 label1 ADD R6, R6, #-1
      ....
x3409 JSR label1
```

   a. Using the opcode table, assemble the JSR instruction to its binary representation, and give your answer in hexadecimal.

   b. Give the RT (Register Transfer) description of the JSR instruction.

   c. List, in the correct sequence, every control signal set by the FSM to implement the JSR instruction.

2. Describe the steps of the fetch step of the instruction cycle in register transfer notation



3. Use the datapath on the previous page to help you answer the next three questions

    a. The LD.PC controls when to write an address to the PC. During a BR instruction, what boolean logic is used to determine whether to assert LD.PC and overwrite the PC?

    b. What other LD control signal in the diagram is asserted whenever LD.CC is asserted?

c. Where does the FSM get the values n, z, and p to compare to N, Z, and P?

4. Use the fixed decimal point number -14.625 and answer the following questions to convert it to IEEE 754.

    a. Give -14.625 in base 2 normalized scientific notation

    b. Give the full 32-bit encoding of -14.625 into IEEE 754. Give your answer as an 8-digit hexadecimal value.

5. Two Bit Adder, this is not a full adder. This is a custom 2-bit adder circuit.

   Answer the following two questions to design a 2-bit adder circuit. The circuit has 4 input bits, two for the A operand and two for the B operand. The output is 3 bits for the boolean variable S which is equal to the sum of A + B. An example is if A: 01 and B:01 then S:010 since 1 + 1 is 2.

   a. Construct the complete truth table(s) for the circuit, showing the inputs A and B and the output bits in S.

   b. Derive and simplify the boolean expression for bit 2, the most significant bit, of the sum S.

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SCRATCH PAGE – TEAR OFF, FILL IN YOUR NAME, HAND IN WITH EXAM!