# EE/CS120A-Logic Design

## Homework 3 Solution

**Problem 1**: What is the simplest SoP expression for function Z(A, B, C) implemented by the two 2-to-1 MUXes in Figure 1?

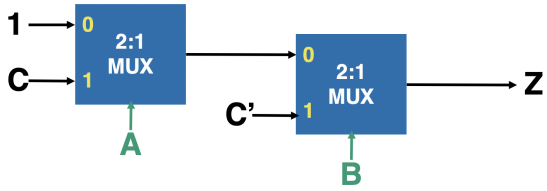



Figure 1

**Answer:**

Z = B'(A'1 + AC) + BC' = B'(A' + C) + BC' = B'A' + B'C + BC'

**Problem 2**: For the truth table in Table 1, design the circuit using one 2-to-1 MUX where $w_1$ is the control/selection signal; in other words, please finish the circuit design in Figure 2.

| $w_1$ | $w_2$ | $w_3$ | $f$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Table 1

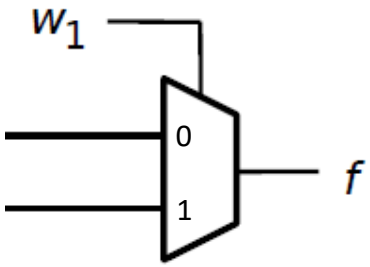
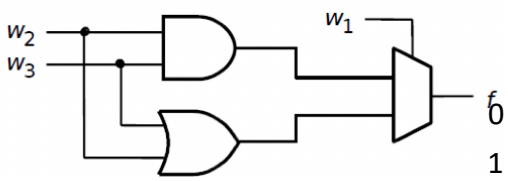



Figure 2

**Answer**:

| $w_1$ | $w_2$ | $w_3$ | $f$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

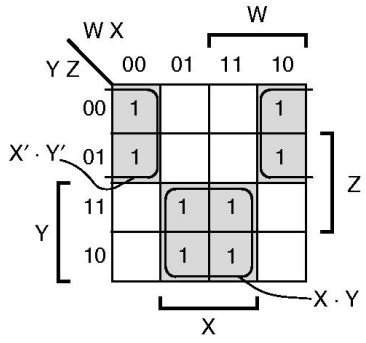
| $w_1$ | $f$ |
|---|---|
| 0 | $w_2w_3$ |
| 1 | $w_2+w_3$ |



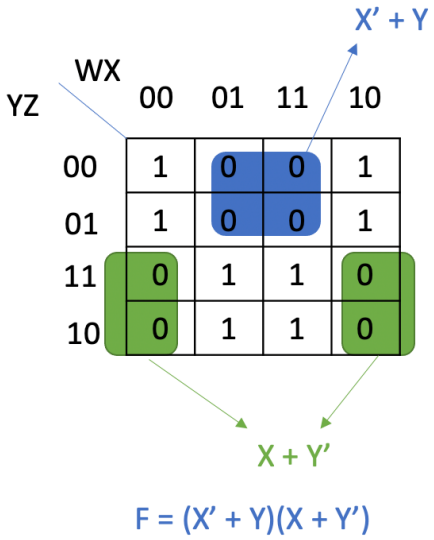

**Problem 3**: Using KMaps, find the simplest SOP and POS expressions of

$F = \Sigma_{W,X,Y,Z}(0, 1, 6, 7, 8, 9, 14, 15)$.

**Answer:**




$F = X' \cdot Y' + X \cdot Y$

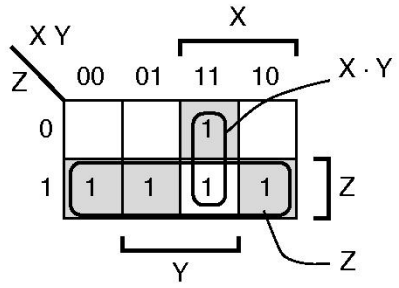


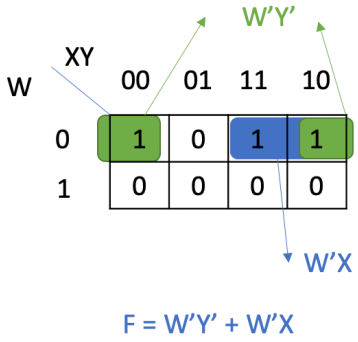

$F = (X' + Y)(X + Y')$

**Problem 4**: Using KMaps, find the simplest SOP expression of the following functions:

1) $F = \Sigma_{X,Y,Z}(1, 3, 5, 6, 7)$;
2) $F = \Pi_{W,X,Y}(1, 4, 5, 6, 7)$

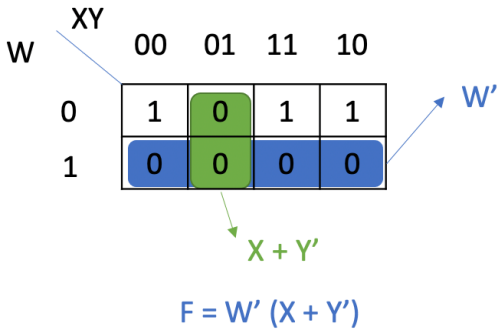
**Answer:**




**Problem 5**: Using KMaps, find the simplest POS expression of $F = \Pi_{W,X,Y}(1, 4, 5, 6, 7)$

**Answer:**




**Problem 6**: For the function f ($w_3$, $w_2$, $w_1$) = $m_1 + m_3 + m_4 + m_6$, show how the function f can be implemented using a 3-to-8 binary decoder and what is the truth table of your decoder?

**Answer:**
As f ($w_3$, $w_2$, $w_1$) = $m_1 + m_3 + m_4 + m_6$, f = 1 if $m_1 = 1$ or $m_3 = 1$ or $m_4 = 1$ or $m_6 = 1$.
If $w_3$=0, $w_2$=0, $w_1$=1, then $m_1 = 1$, thus f = $m_1 + m_3 + m_4 + m_6 = 1 + 0 + 0 + 0 = 1$.
If $w_3$=0, $w_2$=1, $w_1$=1, then $m_3 = 1$, thus f = $m_1 + m_3 + m_4 + m_6 = 0 + 1 + 0 + 0 = 1$.
If $w_3$=1, $w_2$=0, $w_1$=0, then $m_4 = 1$, thus f = $m_1 + m_3 + m_4 + m_6 = 0 + 0 + 1 + 0 = 1$.
If $w_3$=1, $w_2$=1, $w_1$=0, then $m_6 = 1$, thus f = $m_1 + m_3 + m_4 + m_6 = 0 + 0 + 0 + 1 = 1$.

This means that if $w_3$, $w_2$, $w_1$ are the three inputs of a 3-to-8 binary decoder where the Enable signal is always 1, f can be implemented using a 3-to-8 decoder and the truth table as well as the circuit design can be found below.

| Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $En$ | $w_3$ | $w_2$ | $w_1$ | $y_0$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ | $y_5$ | $y_6$ | $y_7$ |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |