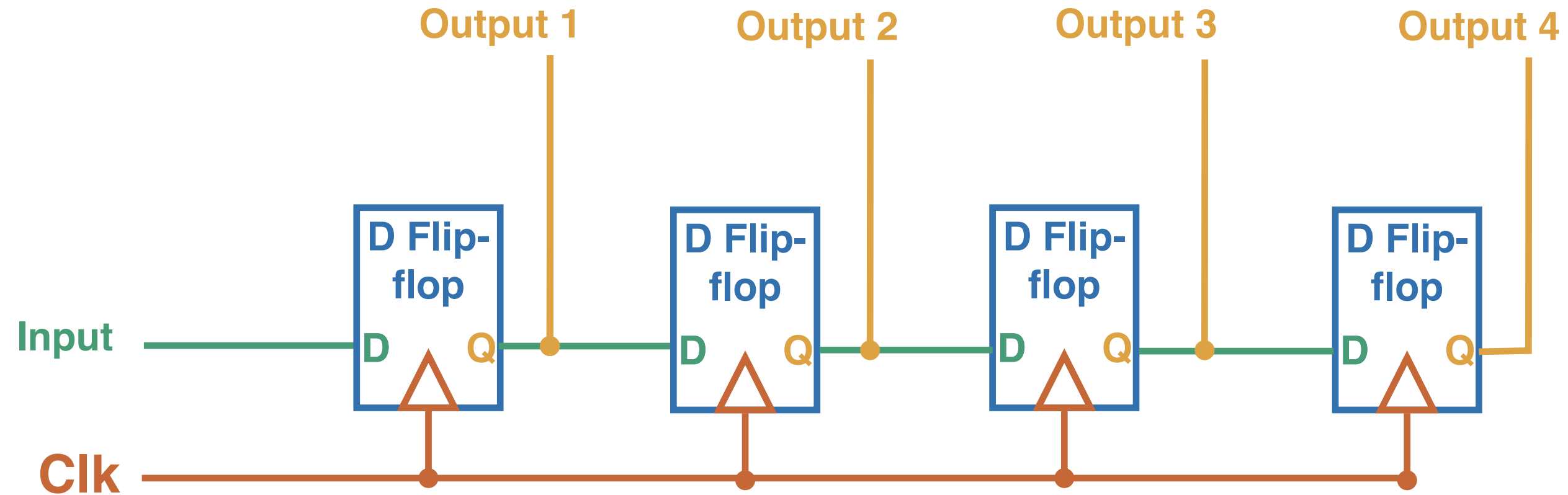
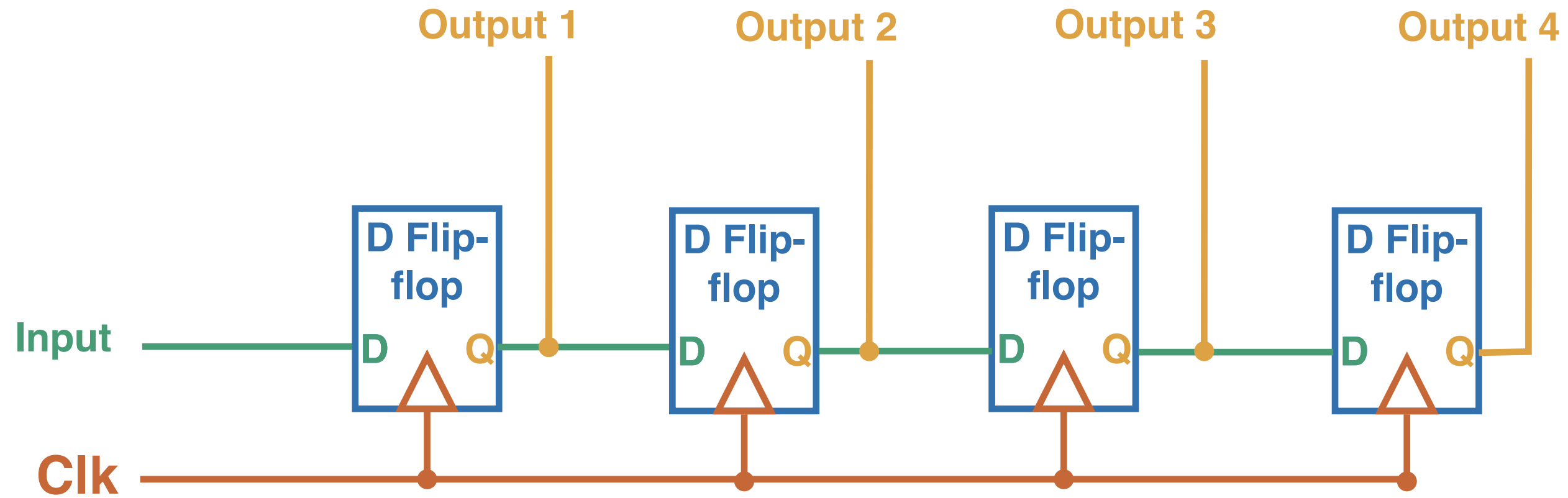


Final Exam Review

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Problem 1: Given the circuit, what are we expecting to see in outputs (Output 1, Output 2, Output 3, Output 4) in the beginning of the 4th cycle (aka after 3 clock cycles) after receiving (1, 1, 0) from the input? Assume that the initial outputs for all the D-FFs are 0.

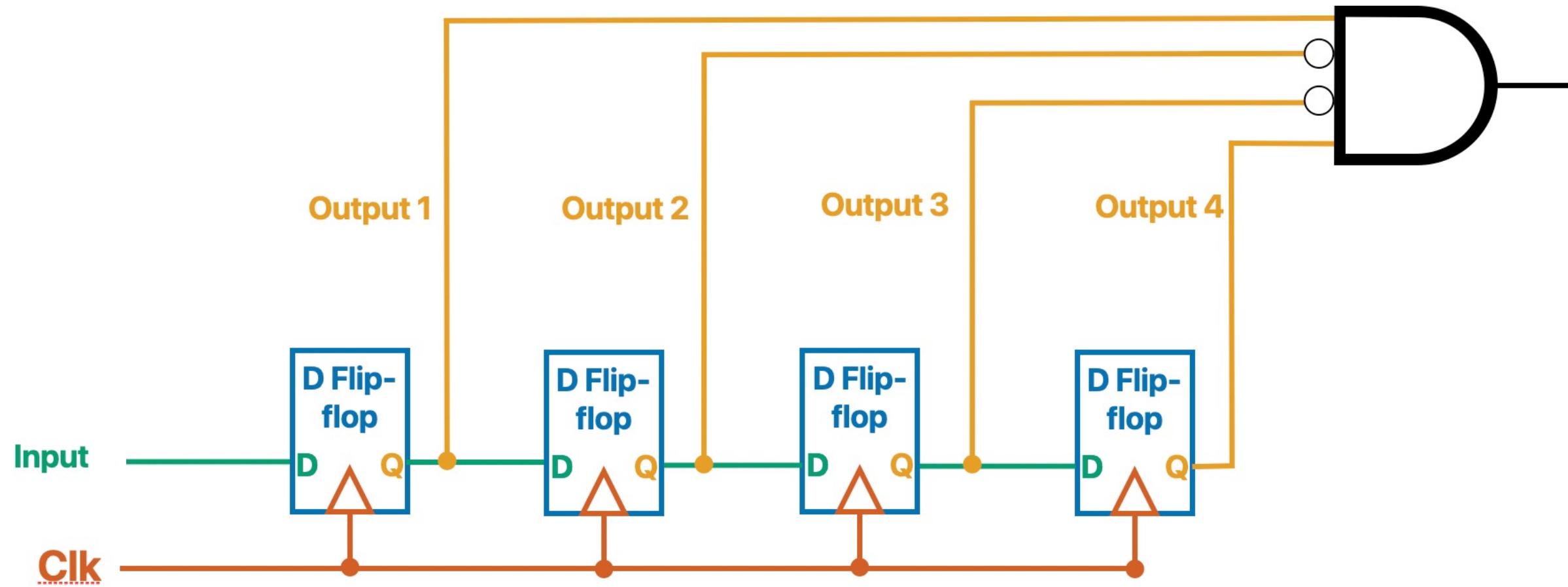




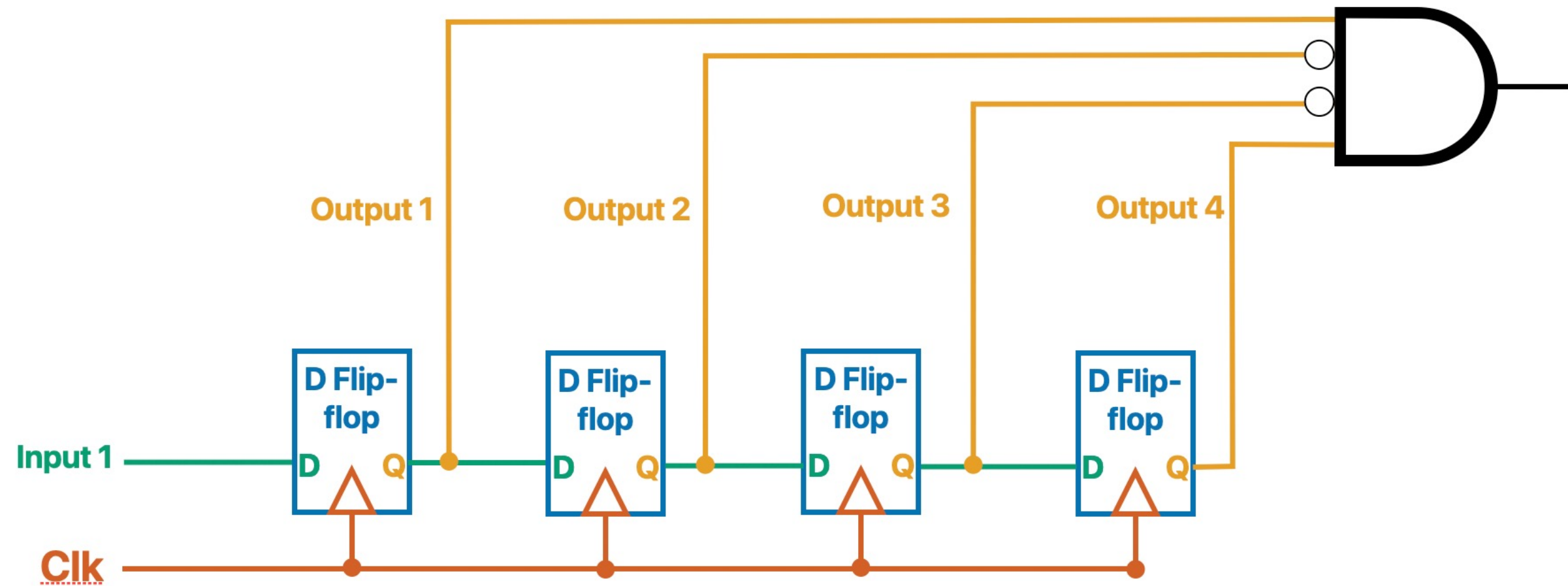
Solution:

$$(O1, O2, O3, O4) = (0, 1, 1, 0)$$

Problem 2: what sequences of input will let the circuit output “0”?



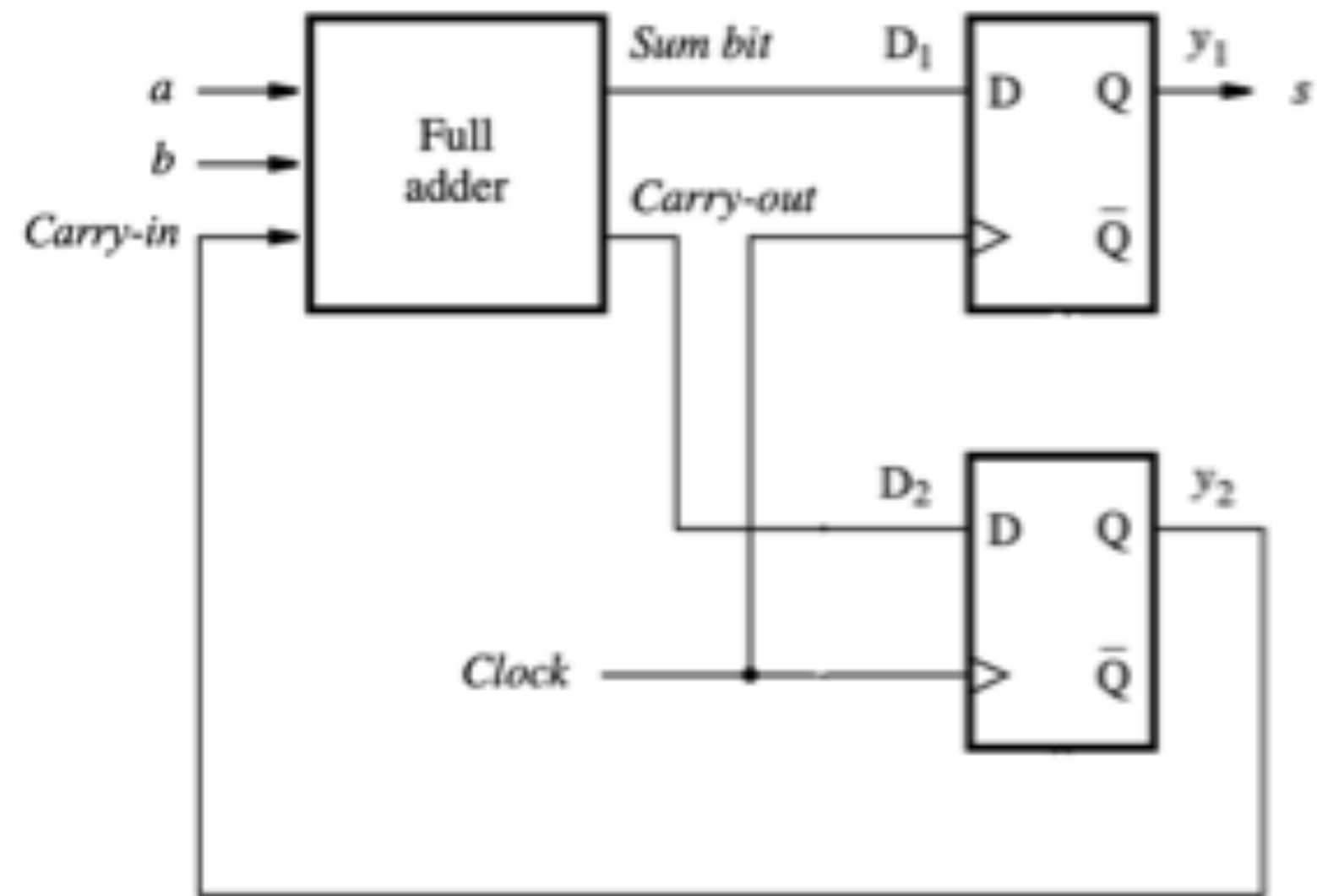
Problem 2: what sequences of input will let the circuit output “0”?



Solution:

Any sequence except (1 0 0 1)

Problem 3: Given the sequential circuit, please complete the excitation table.



Present state y_2y_1	$ab = 00 \quad 01 \quad 10 \quad 11$				Output s
	D_2D_1				
0 0					
0 1					
1 0					
1 1					

Solution:

Present state y_2y_1	$ab = 00 \quad 01 \quad 10 \quad 11$				Output s
	D_2D_1				
0 0	0 0	0 1	0 1	1 0	0
0 1	0 0	0 1	0 1	1 0	1
1 0	0 1	1 0	1 0	1 1	0
1 1	0 1	1 0	1 0	1 1	1

Problem 4: Please convert the Mealy FSM to a Moore machine by showing the Moore FSM table.

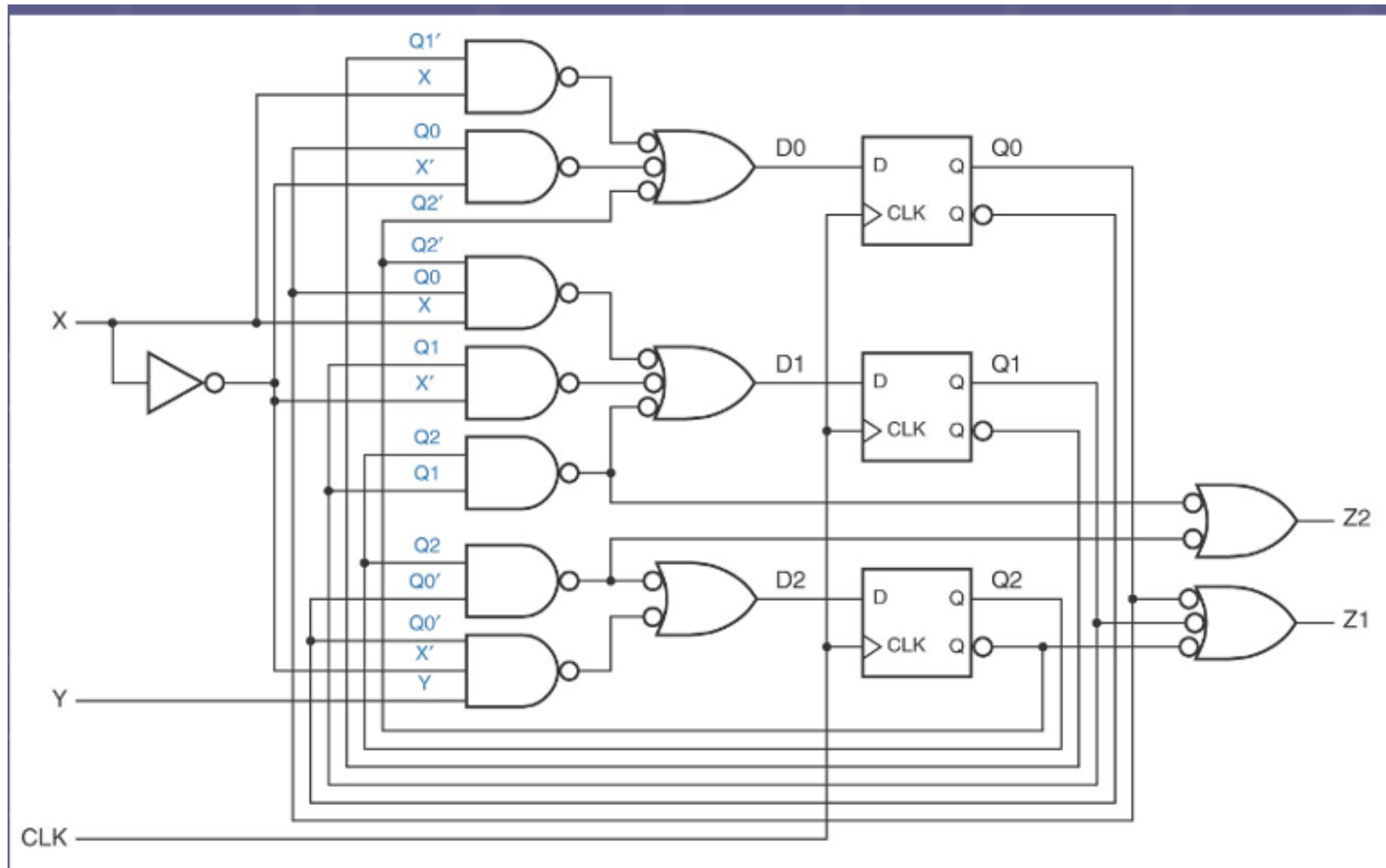
Current State	Next State, Output	
	Input	
	0	1
A	B,1	D,0
B	C,0	B,0
C	B,1	A,0
D	B,0	C,0

Solution:

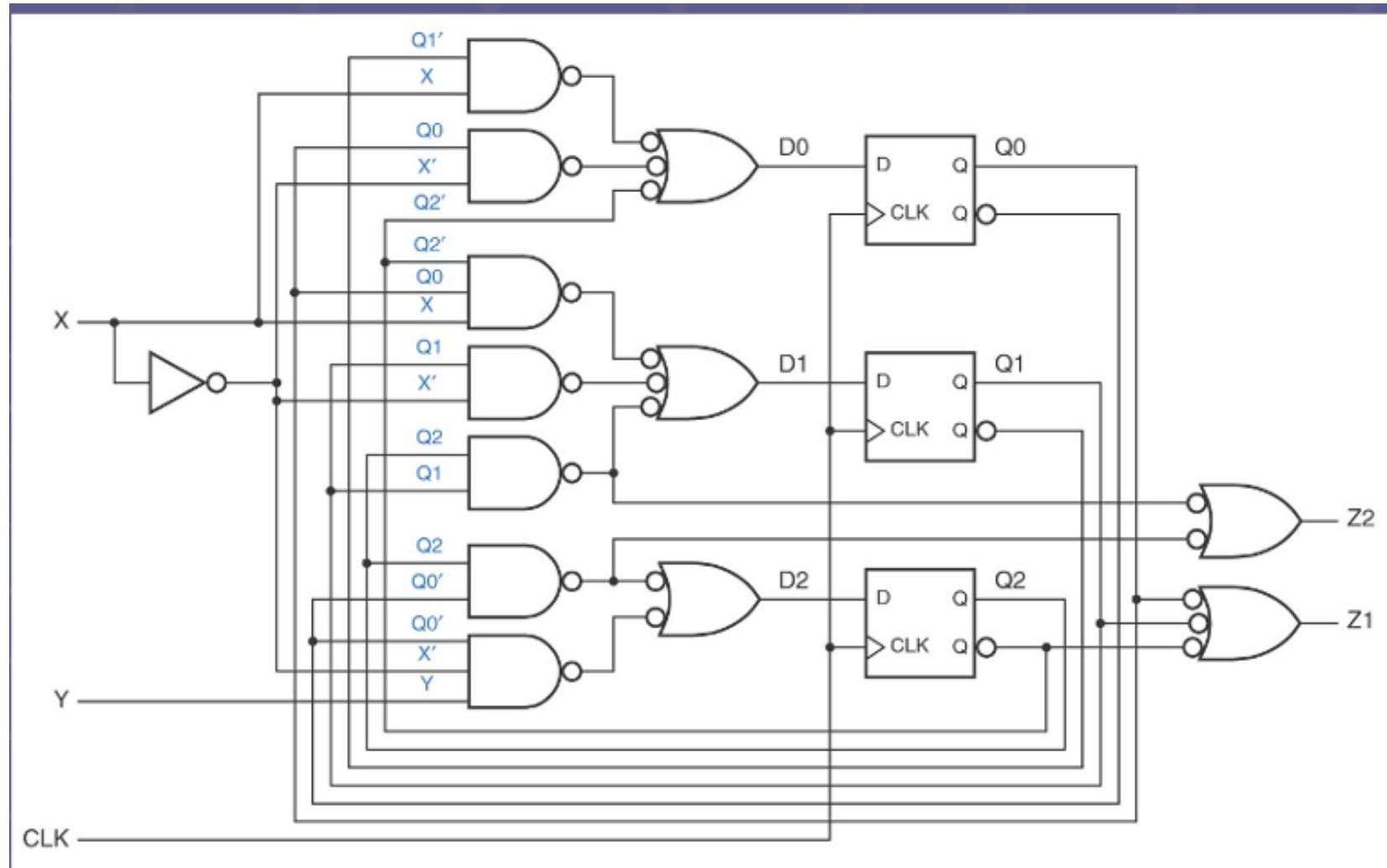
We define the new state A as (A, 0), new state B as (B, 0), new state C as (C, 0), new state D as (D, 0), and new state E as (B, 1).

Current State	Next State		Output
	Input		
	0	1	
A	E	D	0
B	C	B	0
C	E	A	0
D	B	C	0
E	C	B	1

Problem 5: What are the excitation equations, output equations, characteristic equations?



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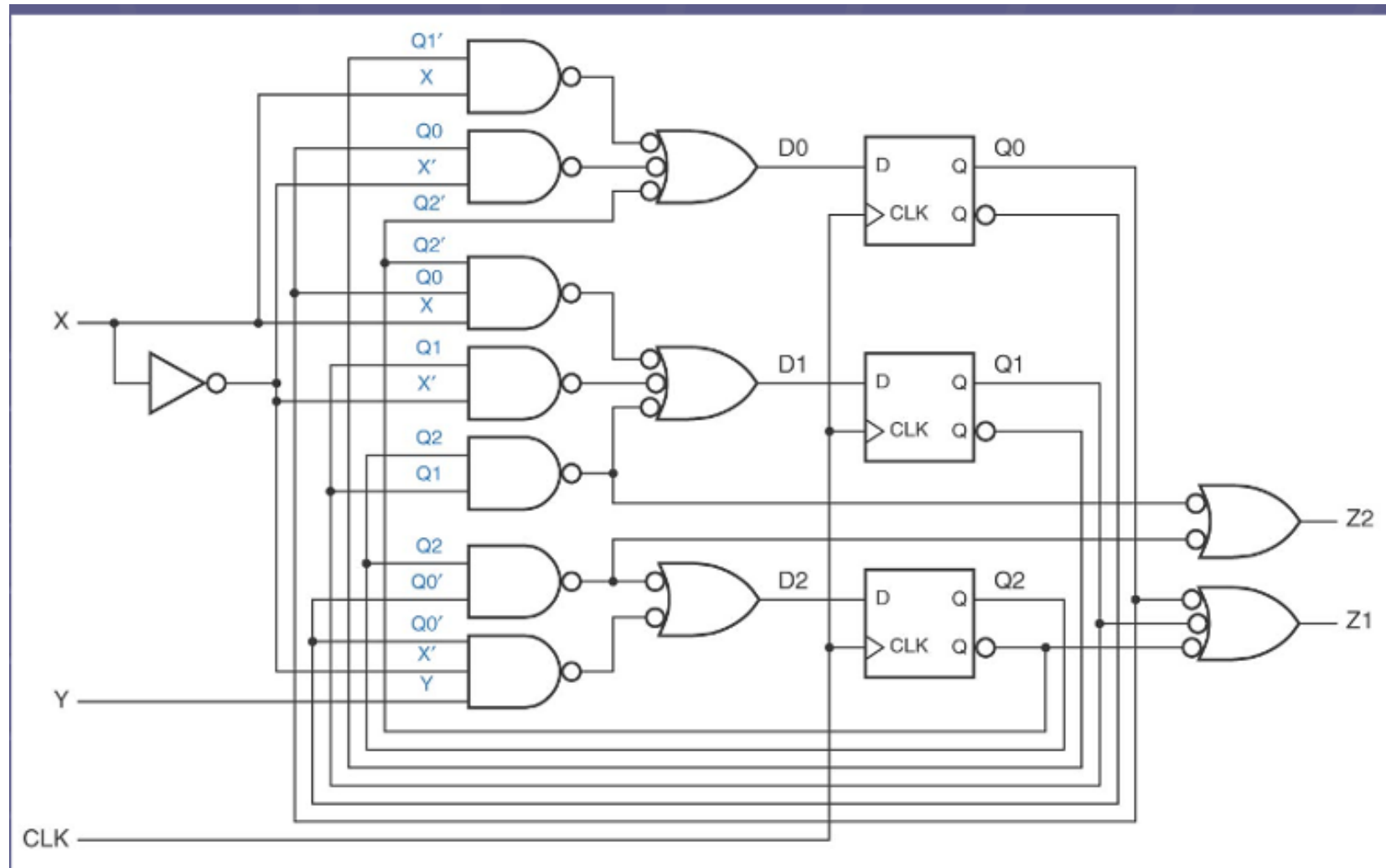


Solution:

excitation equations

$$\begin{aligned} D0 &= Q1' . X + Q0 . X' + Q2 \\ D1 &= Q2' . Q0 . X + Q1 . X' + Q2 . Q1 \\ D2 &= Q2 . Q0' + Q0' . X' . Y \end{aligned}$$

Problem 5: What are the excitation equations, output equations, characteristic equations?

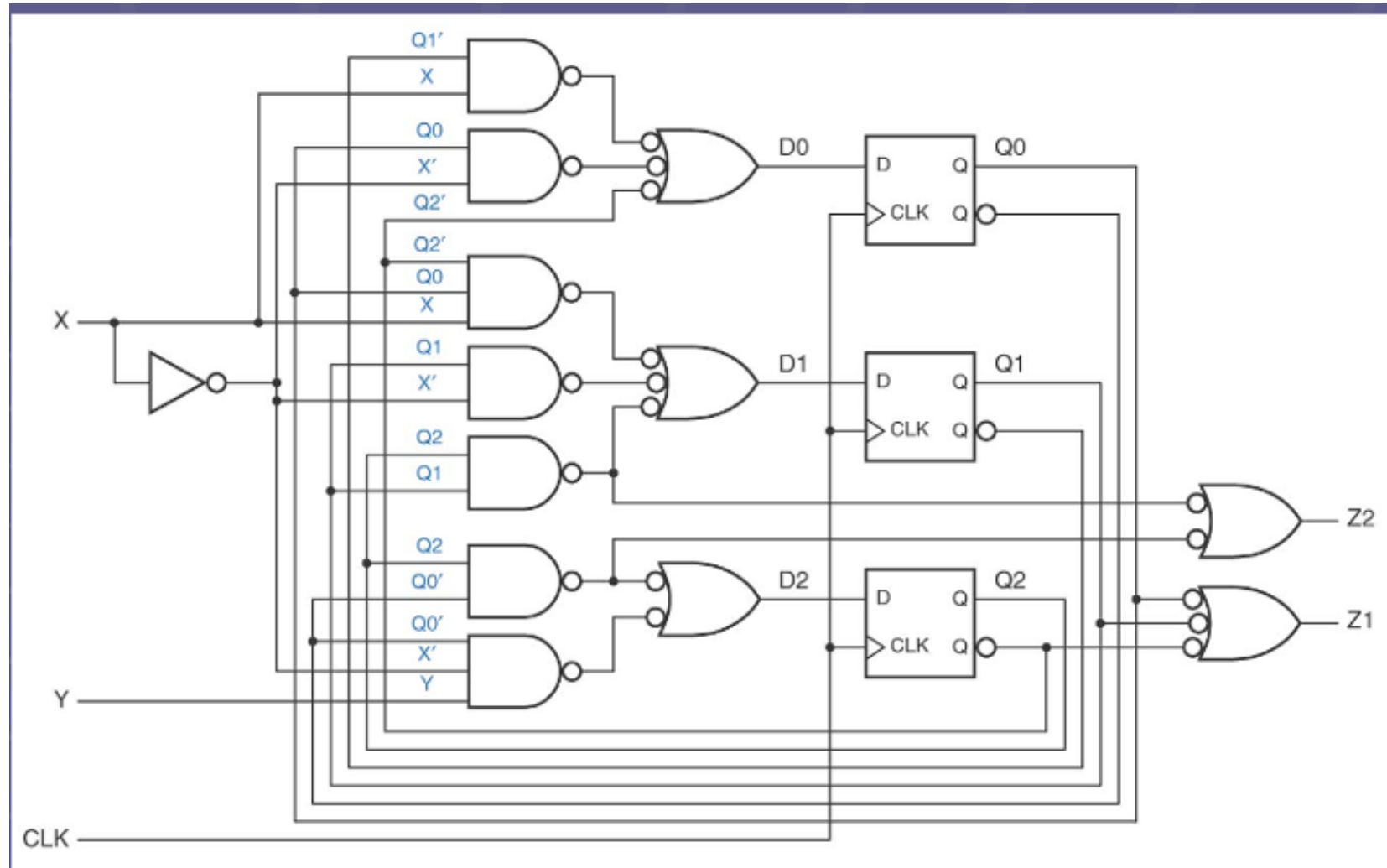


Solution:

characteristic equations

$$Q0^* = D0; Q1^* = D1; Q2^* = D2$$

Problem 5: What are the excitation equations, output equations, characteristic equations?

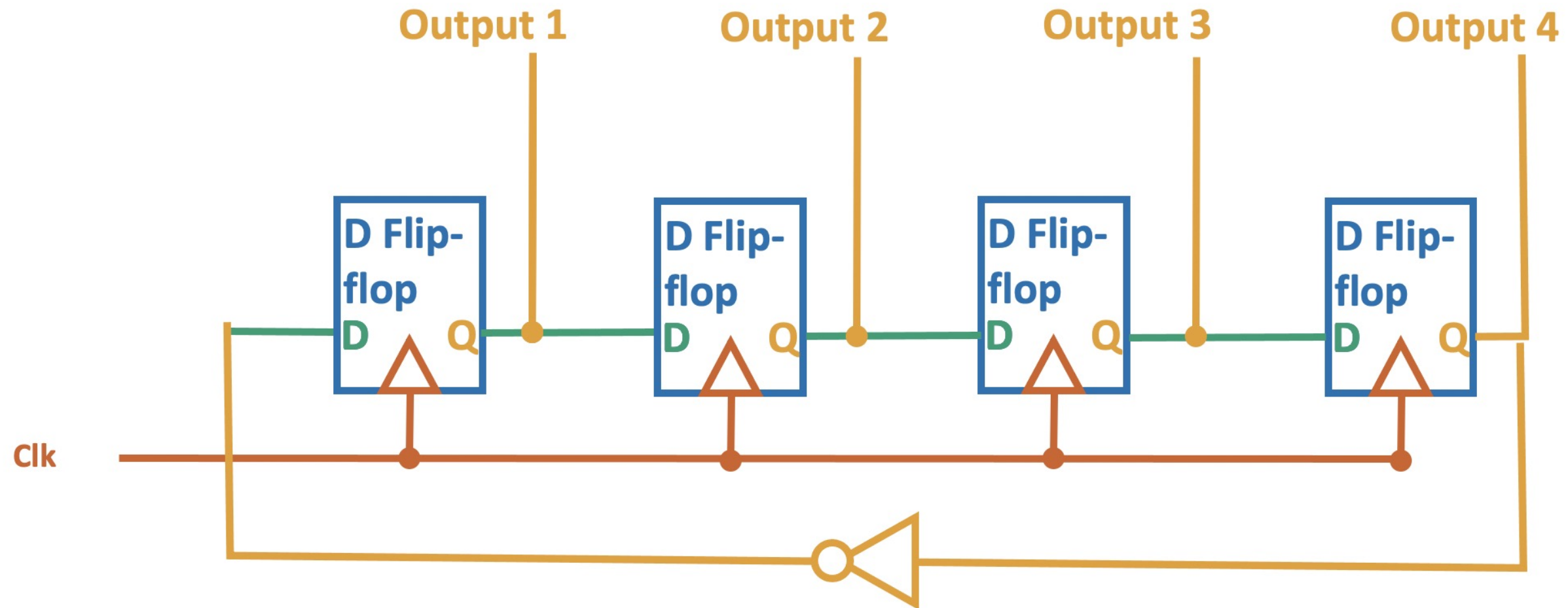


Solution:

output equations

$$Z1 = Q2 + Q1' + Q0'$$
$$Z2 = Q2 \cdot Q1 + Q2 \cdot Q0'$$

Problem 6: Assume that initially, Output1 = 0, Output 2 = 0, Output 3 = 1, Output 4 = 1. What are all the outputs after 1, 2, 3, 4, and 5 clock cycles?



Solution:

After 1 clock cycle: Output1 = 0, Output 2 = 0, Output 3 = 0, Output 4 = 1

After 2 clock cycles: Output1 = 0, Output 2 = 0, Output 3 = 0, Output 4 = 0

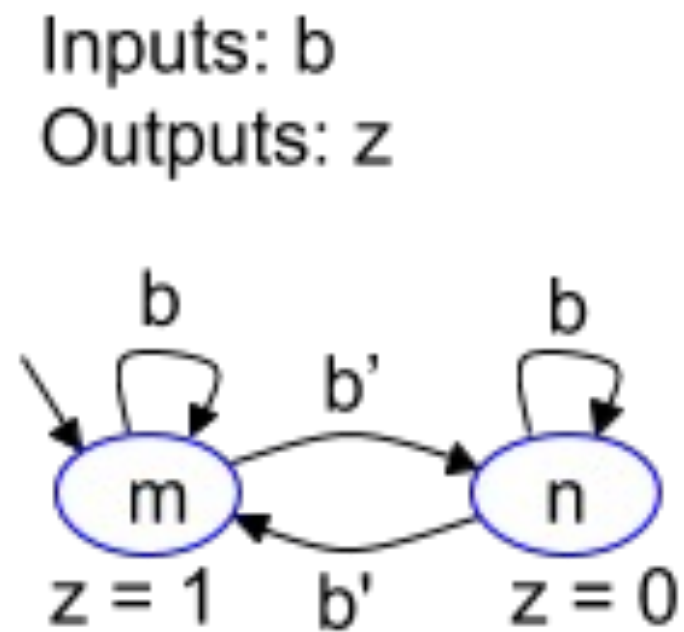
After 3 clock cycles: Output1 = 1, Output 2 = 0, Output 3 = 0, Output 4 = 0

After 4 clock cycles: Output1 = 1, Output 2 = 1, Output 3 = 0, Output 4 = 0

After 5 clock cycles: Output1 = 1, Output 2 = 1, Output 3 = 1, Output 4 = 0

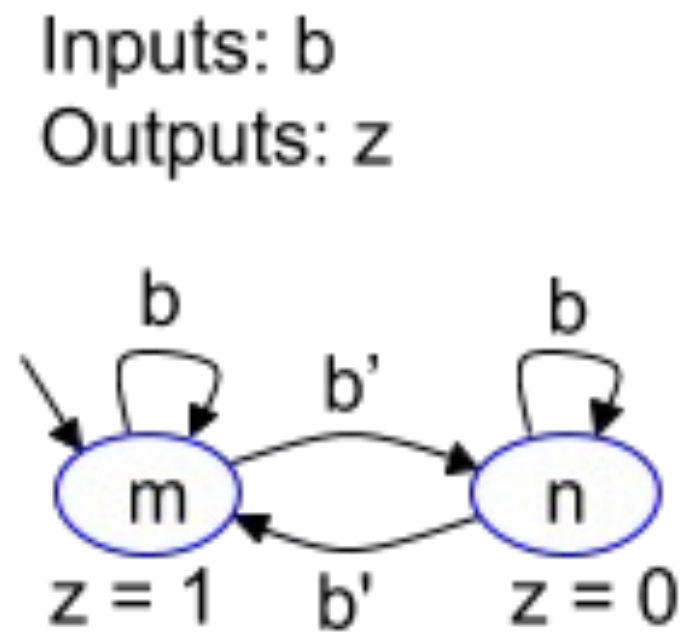
Problem 7:

The given FSM has input b , output z , and starts in state m . What is the FSM's resulting output and state if on the clock's active edge b is 0?



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The given FSM has input b , output z , and starts in state m . What is the FSM's resulting output and state if on the clock's active edge b is 0?



Solution:

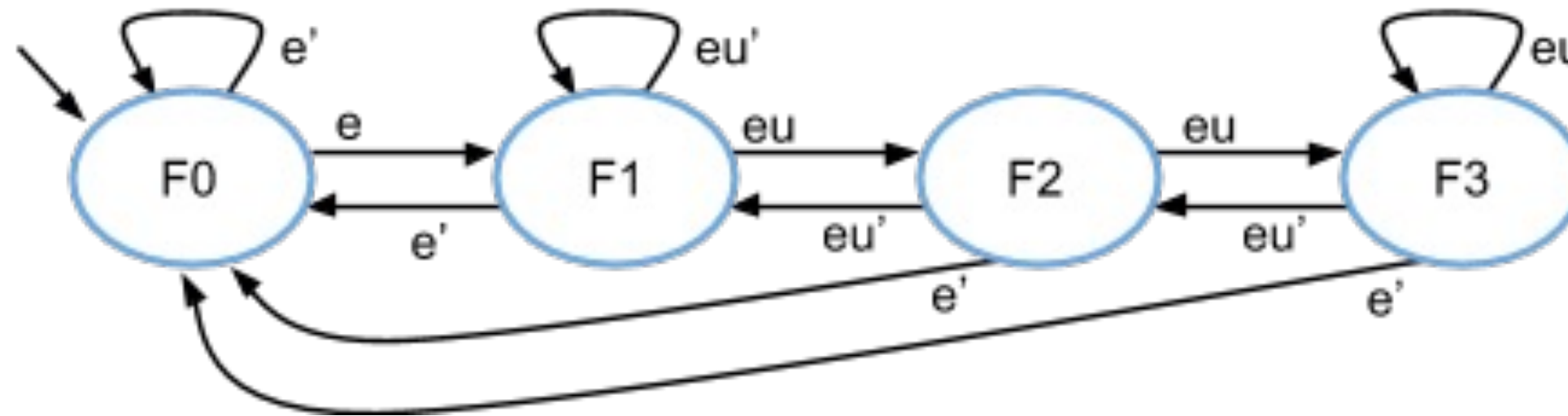
$z = 0$, state = n

Problem 8:

State F3 transitions to state _____ when enable (e) is 0.

State F1 transitions to state _____ when e is 0 and u is 1.

Inputs: e, u

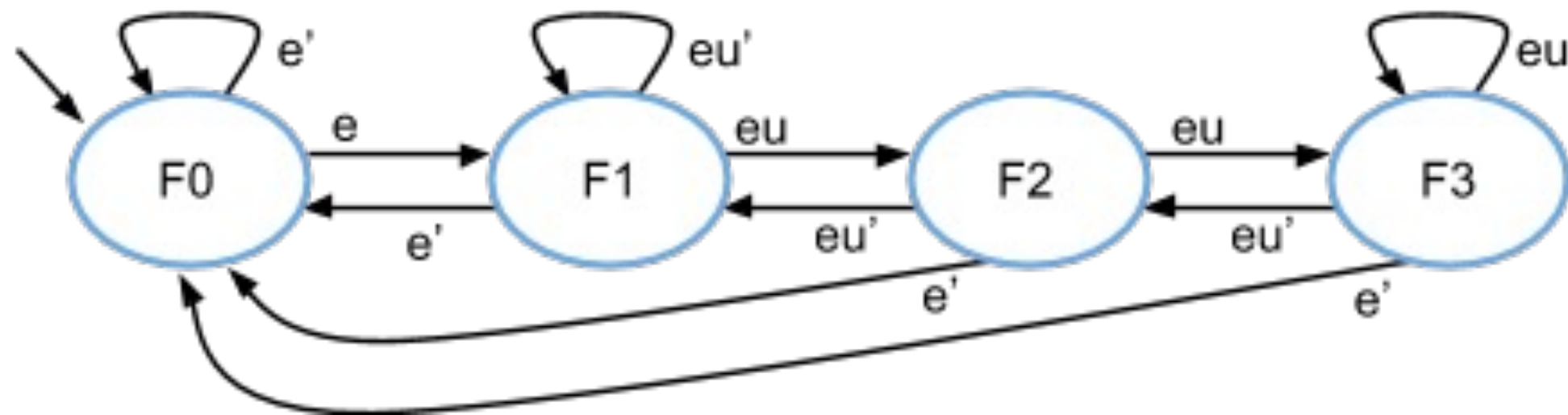


Problem 8:

State F3 transitions to state _____ when e is 0.

State F1 transitions to state _____ when e is 0 and u is 1.

Inputs: e, u



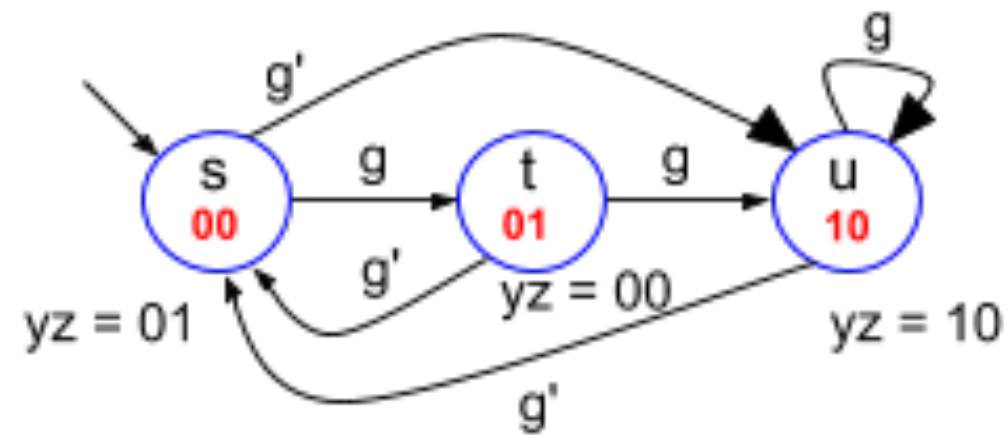
Solution: F0

F0

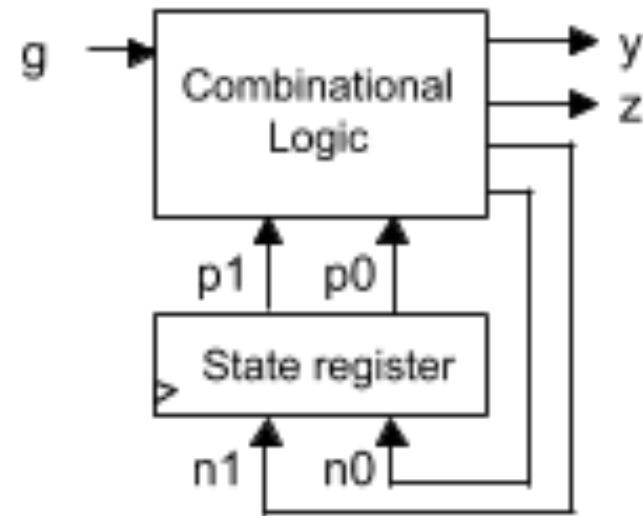
Problem 9:

Please fill up all the missing entries in the table.

Inputs: g
Outputs: y, z



*State encodings are in red



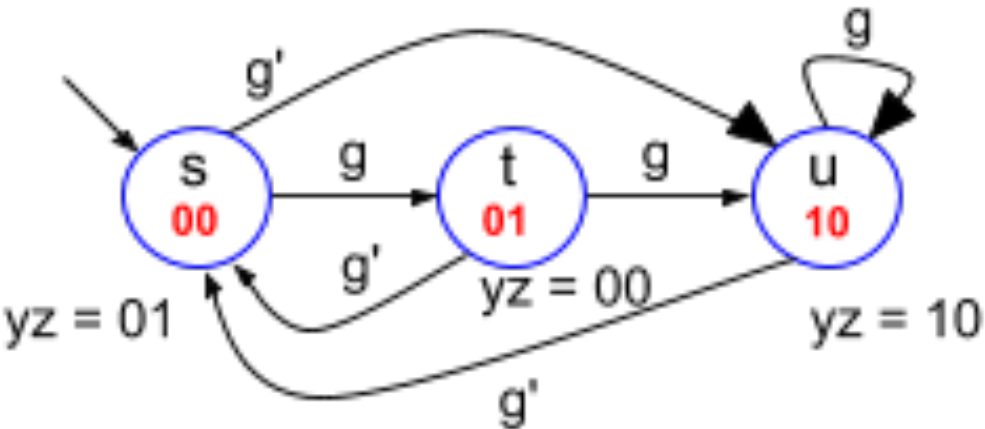
	p1	p0	g	n1	n0	y	z
s	0	0	0				
	0	0	1				
t	0	1	0				
	0	1	1				
u	1	0	0				
	1	0	1				
unused	1	1	0				
	1	1	1				

Problem 9:

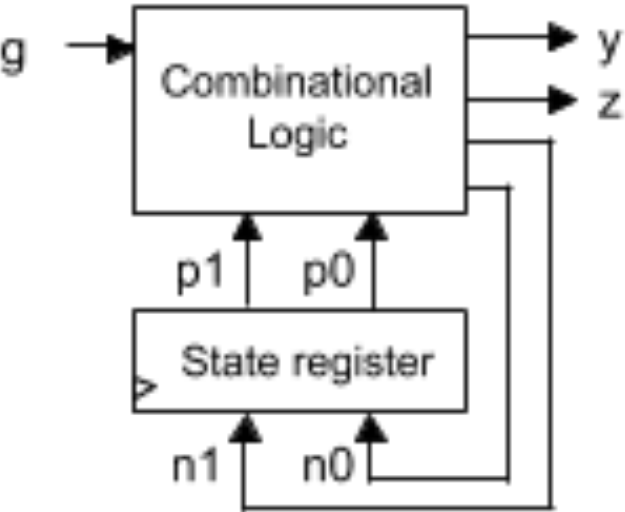
Please fill up all the missing entries in the table.

Solution:

Inputs: g
Outputs: y, z



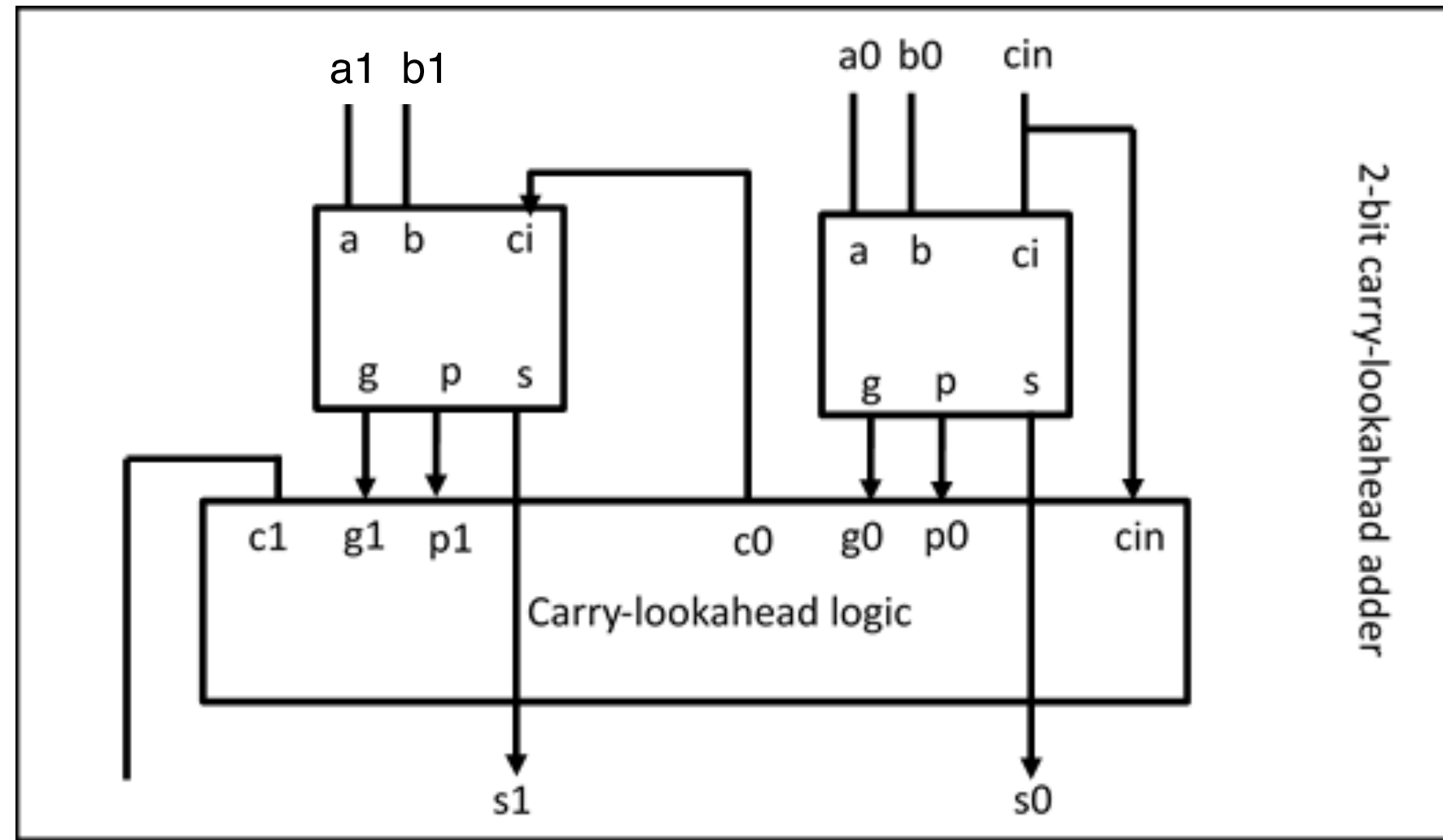
*State encodings are in red



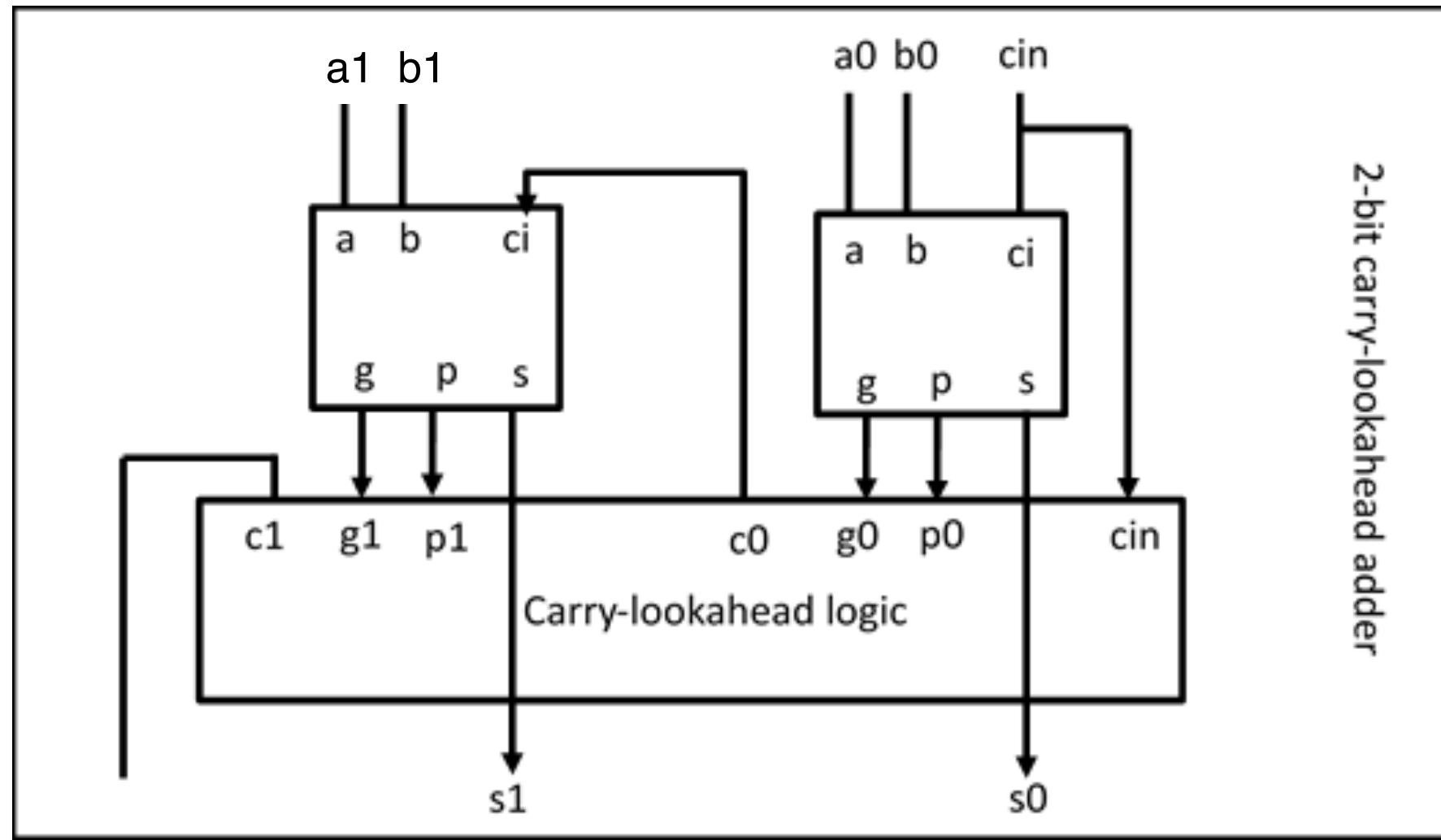
	p1	p0	g	n1	n0	y	z
s	0	0	0	1	0	0	1
	0	0	1	0	1	0	1
t	0	1	0	0	0	0	0
	0	1	1	1	0	0	0
u	1	0	0	0	0	1	0
	1	0	1	1	0	1	0
unused	1	1	0	x	x	x	x
	1	1	1	x	x	x	x

Problem 10:

Please identify all the true statement(s) about the given 2-bit carry-lookahead adder. For each true statement, what are the values of a_0 , a_1 , b_0 , b_1 , c_{in} , p_0 , p_1 , g_0 , g_1 , c_0 , c_1 , s_0 , and s_1 ? Hint: $g = ab$, $p = a \oplus b$, and the expression for each digit's carry-out is $c_o = g + p \cdot c_i$.



1. $c_0 = 0$, when $a_0 = 1$, $b_0 = 1$, and $c_{in} = 0$
2. $c_0 = 1$, when $a_0 = 1$, $b_0 = 1$, $c_{in} = 1$, $p_1 = 1$, and $b_1 = 1$
3. $c_1 = 1$, when $c_{in} = 1$, $g_0 = 1$, $p_0 = 0$, $g_1 = 0$, and $p_1 = 0$
4. $c_1 = 0$, when $c_{in} = 0$, $g_0 = 1$, $p_0 = 0$, $g_1 = 1$, and $p_1 = 0$



Solution:

Only the 2nd statement is true.

$a_0 = 1, b_0 = 1, cin = 1, p_0 = 0, g_0 = 1, c_0 = 1, s_0 = 1$

$a_1 = 0, b_1 = 1, c_1 = 1, g_1 = 0, p_1 = 1, s_1 = 0$

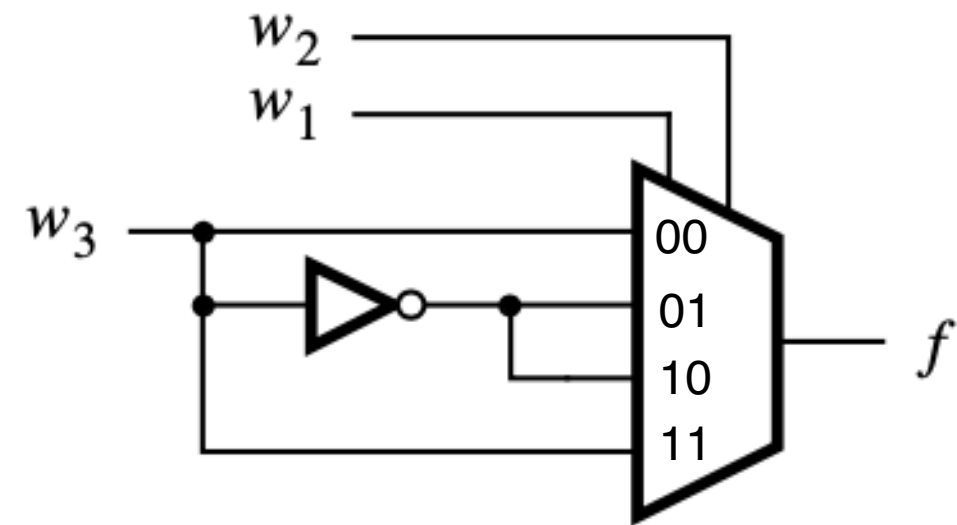
Problem 11:

Design a circuit for the following truth table using a 4-to-1 MUX and necessary gate(s).

w_1	w_2	w_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

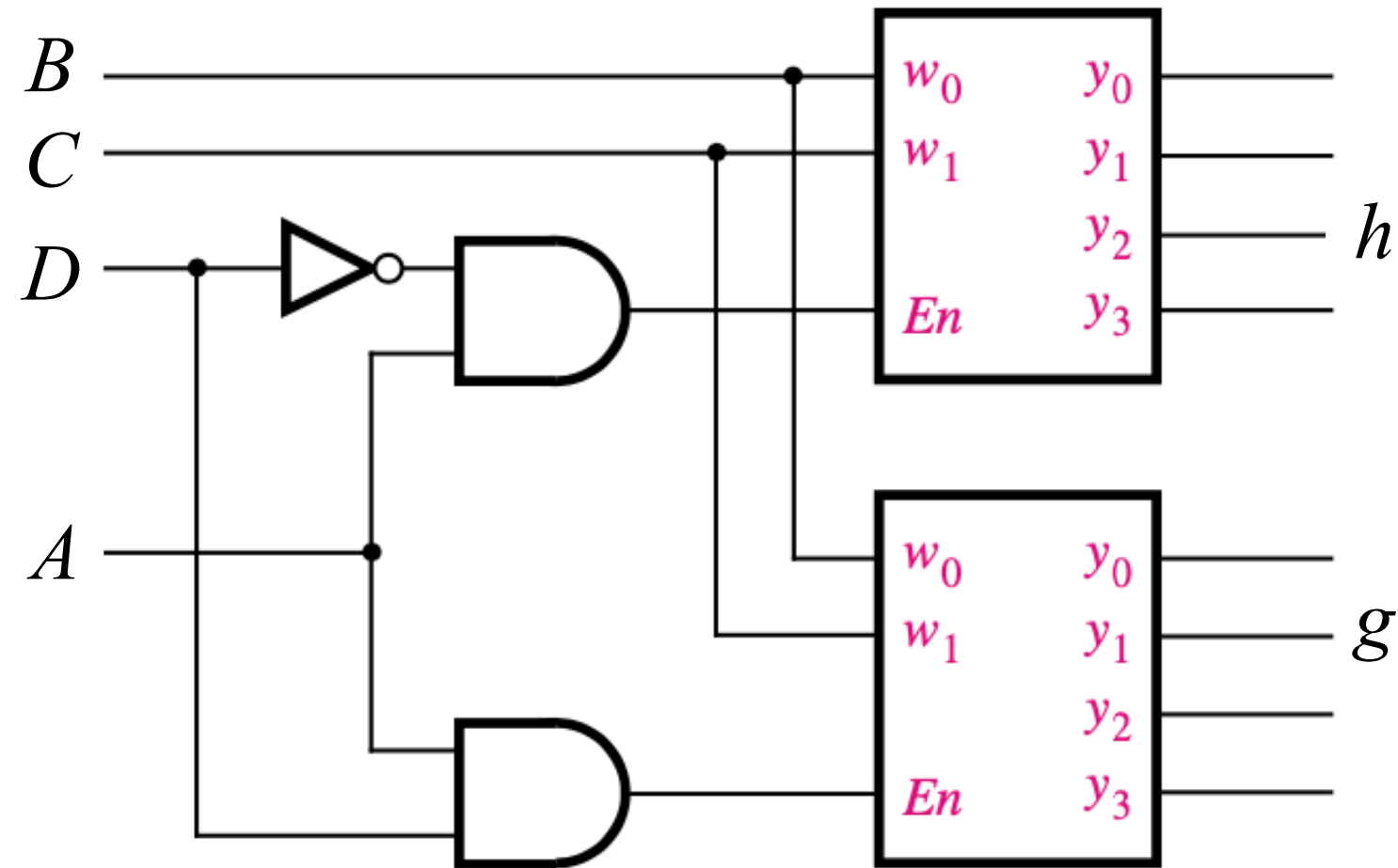
Solution:

w_1	w_2	w_3	f	
0	0	0	0	} w_3
0	0	1	1	
0	1	0	1	} \bar{w}_3
0	1	1	0	
1	0	0	1	} \bar{w}_3
1	0	1	0	
1	1	0	0	} w_3
1	1	1	1	

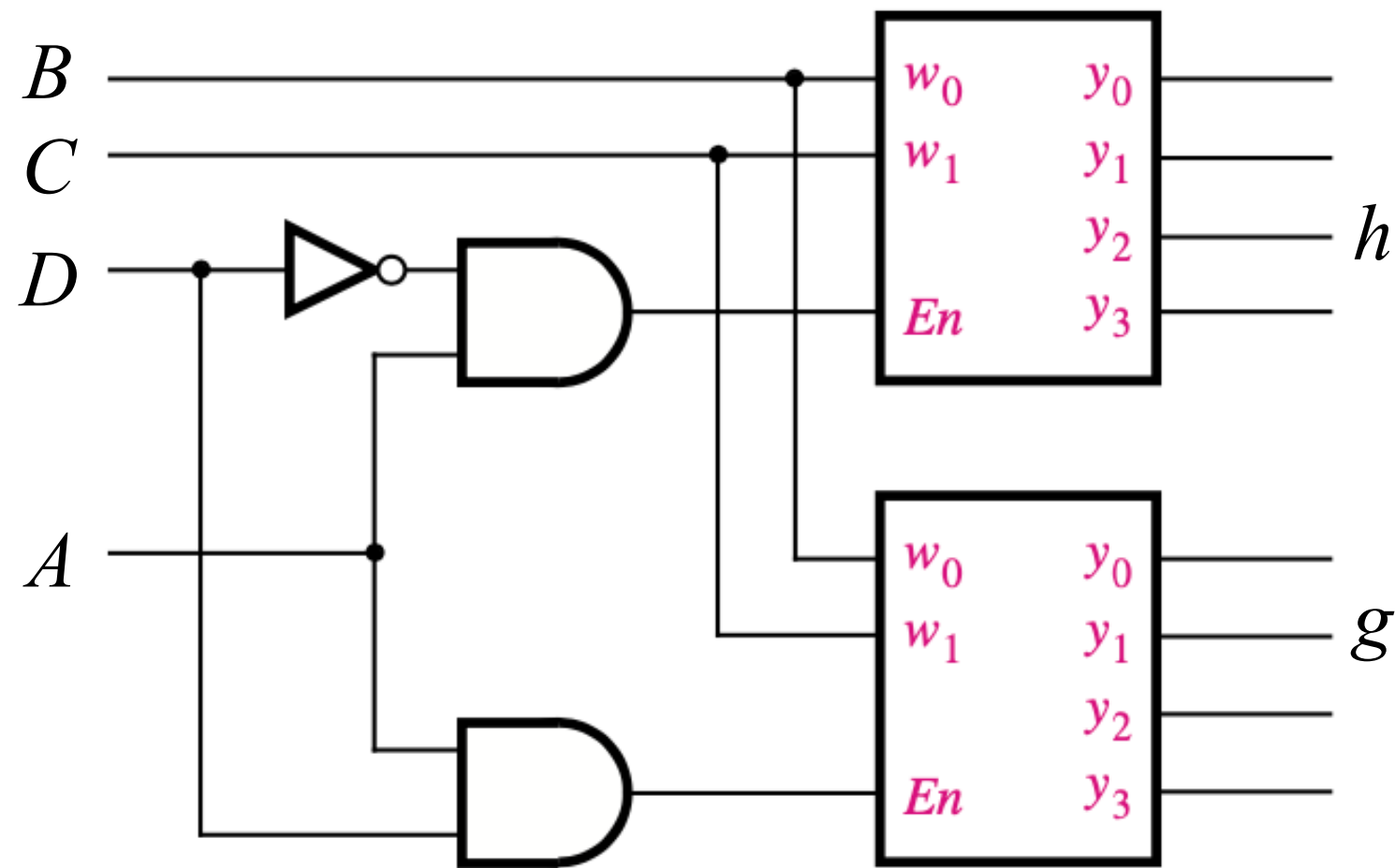


Problem 12:

What are the logic expressions for the outputs h and g ?



Solution:



$h = 1$ iff $B = 0$, $C = 1$, $D = 0$, and $A = 1$

Thus, $h = A B' C D'$

$g = 1$ iff $B = 1$, $C = 0$, $D = 1$, and $A = 1$

Thus, $g = A B C' D$

Problem 13:

Design a sequential circuit with the finite state machine shown in the Table, using D Flip-Flops. Use two state variables, Q1, Q2, with the state assignment A = 00, B = 01(aka Q1=0, Q2=1), C = 11, D = 10.

Current State	Next State, Output	
	Input	
	0	1
A	B,1	D,0
B	C,0	B,0
C	B,1	A,0
D	B,0	C,0

Solution:

Step 1: substitute the states with their assignments

Current State	Next State, Output	
	Input	
	0	1
00	01,1	10,0
01	11,0	01,0
11	01,1	00,0
10	01,0	11,0

Step 2: draw excitation table

Current state, Input	D1	D2	Output
000	0	1	1
001	1	0	0
010	1	1	0
011	0	1	0
110	0	1	1
111	0	0	0
100	0	1	0
101	1	1	0

Step 3: get the logic expressions for D1, D2, and Output

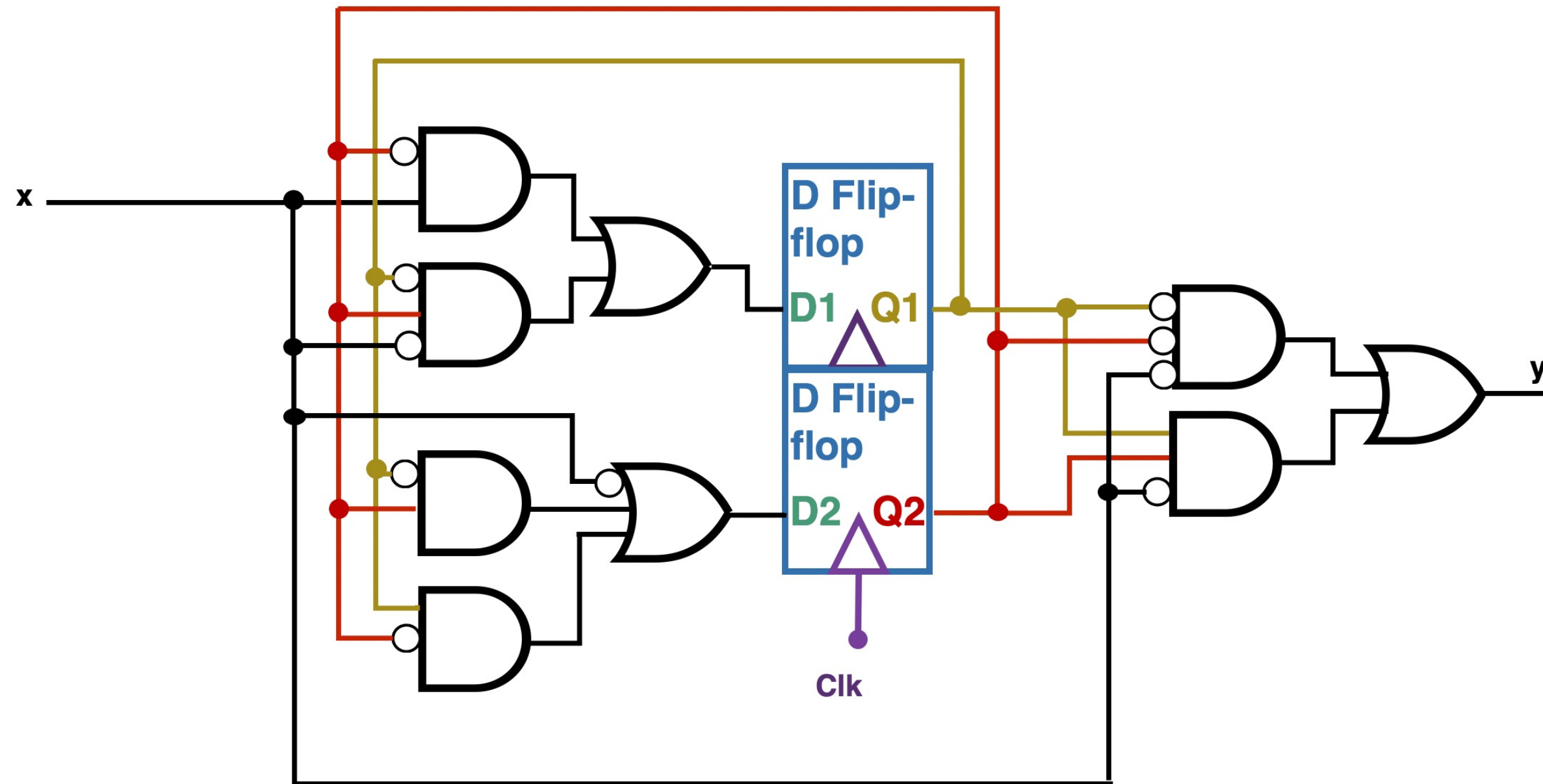
Current state is represented by Q1 and Q2, e.g., B=01 where Q1=0 and Q2=1. Let's use x and y to denote the input and output, respectively.

$$D1 = Q1' Q2' x + Q1' Q2 x' + Q1 Q2' x = Q2' x + Q1' Q2 x'$$

$$D2 = x' + Q1' Q2 + Q1 Q2'$$

$$y = Q1' Q2' x' + Q1 Q2 x'$$

Step 4: design sequential circuit



Problem 14:

Using KMaps, find the simplest SOP expression for each of the following functions.

$$1) F = \sum_{x,y,z}(1, 3, 5, 6, 7);$$

$$2) F = \sum_{w,x,y,z}(0, 1, 6, 7, 8, 9, 14, 15);$$

$$3) F = \prod_{w,x,y}(1, 4, 5, 6, 7)$$

Problem 14:

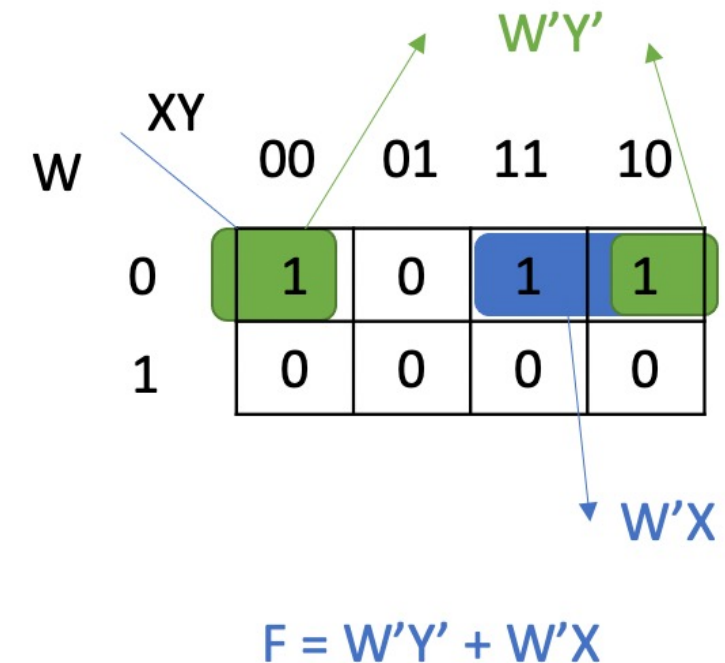
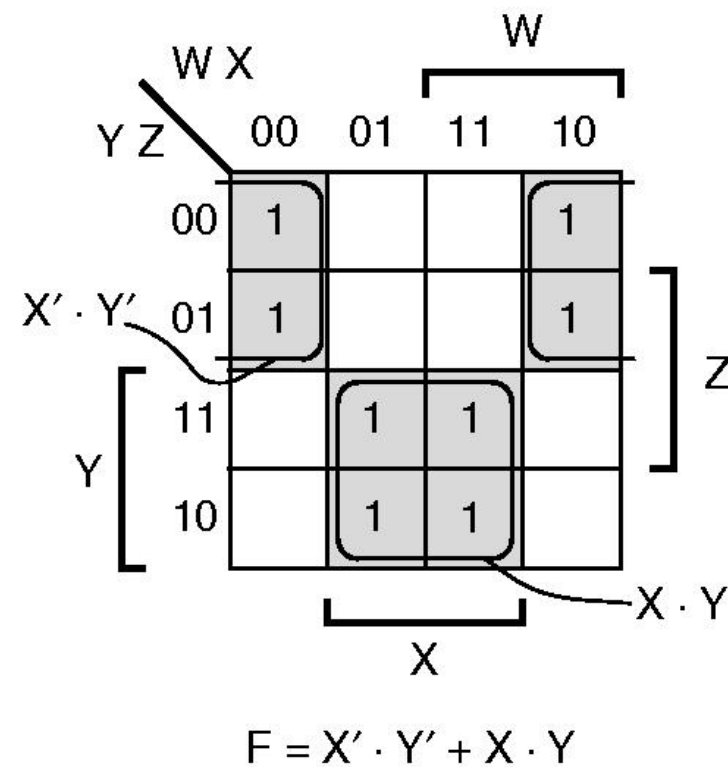
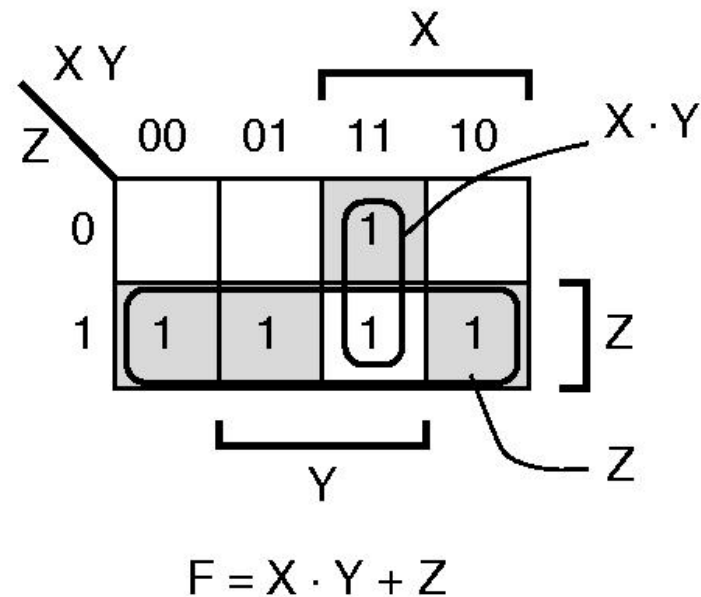
Using KMaps, find the simplest SOP expression for each of the following functions.

1) $F = \sum_{X,Y,Z}(1, 3, 5, 6, 7);$

2) $F = \sum_{W,X,Y,Z}(0, 1, 6, 7, 8, 9, 14, 15);$

3) $F = \prod_{W,X,Y}(1, 4, 5, 6, 7)$

Solution:



Problem 15:

What is the simplest SOP and POS expressions for $F = \Sigma_{A,B,C}(0, 1, 3, 4, 6) + D(2, 5)$, where “D” represents “Don’t care”; see the K-map of F below.

		A'B'	A'B	AB	AB'
		0,0	0,1	1,1	1,0
c'	0	1	X	1	1
c	1	1	1	0	X

Solution:

	A'B'	A'B	AB	AB'
c'	0	1	1	1
c	1	1	0	X

A'

The simplest SOP: $F = A' + C'$

C'

	A'B'	A'B	AB	AB'
c'	1	X	1	1
c	1	1	0	X

A' + C'

The simplest POS: $F = A' + C'$

Problem 16:

Using KMaps, find the simplest POS expression for each of the following functions.

1) $F = \Sigma_{W,X,Y,Z}(0, 1, 6, 7, 8, 9, 14, 15);$

2) $F = \Pi_{W,X,Y}(1, 4, 5, 6, 7)$

Solution:

