EECS 168 Introduction to VLSI Design Sheldon Tan

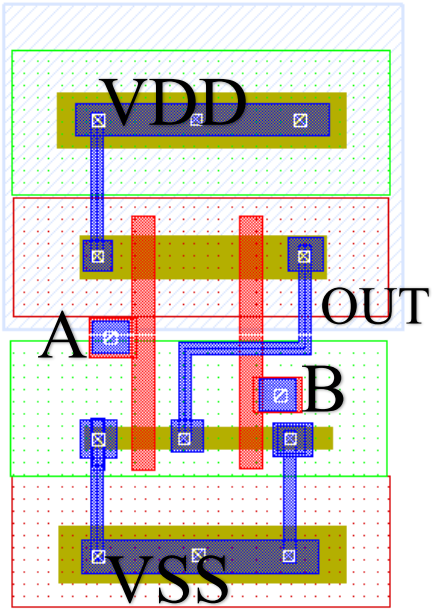
Homework 2

Please use the 180 nm process parameters shown at the end of homework for all the homework questions. For NMOS as $R_n = 6.47K\Omega$, for PMOS as $R_p = 29.6K\Omega$, and $C_l = 0.89f\ F$)

1. Design the static complementary gates (CMOS gates) for the following logic expressions using pull-up/pull-down networks. Use a truth table to show logical equivalence for converted expressions. Assume inverted variables are available, i.e., you do not have to add inverters for complementary variables. (10pt)
   a) a+b
   b) ab
   c) (a+b)c
   d) (ab)' + (cd)

2. Write the defining logic expressions and draw the transistor level schematic for each complex gates below: (10pt)
   a) AOI32
   b) AOI312
   c) OAI22
   d) OAI323

3. Draw the circuit level schematic from the follow layout design. Write the logic expression of the extracted logic. The inputs are indicated by 'A' and 'B' and the output by the "OUT" label. (10pt)



4. Size the transistors in each of those gates so that its pullup and pulldown times are approximate equal. Assume effective resistances for NMOS as $R_n = 6.47K\Omega$, for PMOS as $R_p = 29.6K\Omega$. The loading capacitance for the network is C_L. Please show all the steps. Please consider the following two cases: (15pt)
   (1) In the worst case
   (2) In the best case

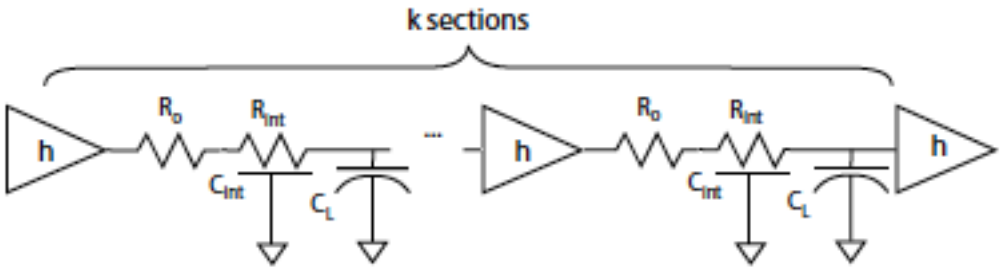
   a) f = a'b'c' + d'
   b) f = a'b' + c'd'
   c) f = a'b + bc

5. Compute the value of R_{eff} required to model the behavior of an inverter that reaches 50% of its output value at 20ps with load C_L equal to $3C_1$, $4C_1$, and $5C_1$. What effect does load capacitance have on the effective resistance ($C_1 = 0.89*10^{-15}$)? (10pt)

6. Compute transition times for a four-input NAND gate with 8/2 pulldown (the W/L = 8/2 for n-type transistors) and 8/2 pullup that drives an identically-sized NOR four-input gate (the NAND gate only drives one input of the NOR gate): (10pt)
   a) Rise time
   b) Fall time

7. Compute rise time for a two-input NAND gate with 8/2 pull-down and 8/2 pullup that drives these wires (assume that the wire impedance is modeled as s single lump): (15pt)
   a) Poly wire with width 3λ, length 300λ.
   b) Metal 1 wire of width with 4λ, length 600λ.
   c) Metal 2 wire of width with 4λ, length 1200λ.

8. For a metal 1 wire with R_{int} =500 Ω C_{int}=200fF, which is driven by a minimum-size buffer, which has equivalent resistance R_0 =6.47k Ω and input capacitance C_0=1.78fF. The wire then drives another minimum-size buffer as shown below. (20pt)



(a) If no additional buffer is inserted, then what is 50% delay?

(b) If one buffer is inserted and the wire is evenly divided into 2 sections (k=2) and all buffer inserted are minimum-size buffers (h=1) , what is 50% delay?

(c) If one buffer is inserted and the wire is evenly divided into 2 sections (k=2) and all buffer inserted are two times of minimum-size buffers (h=2), what is 50% delay?

(d) What is optimal number of buffers, buffer size, and minimum 50% delay?

n-type transconductance	k'_n	$170\mu A/V^2$
p-type transconductance	k'_p	$-30\mu A/V^2$
n-type threshold voltage	V_{tn}	0.5V
p-type threshold voltage	V_{tp}	-0.5V
n-diffusion bottomwall capacitance	$C_{ndiff,bot}$	$940aF/\mu m^2$
n-diffusion sidewall capacitance	$C_{ndiff,side}$	$200aF/\mu m$
p-diffusion bottomwall capacitance	$C_{pdiff,bot}$	$1000aF/\mu m^2$
p-diffusion sidewall capacitance	$C_{pdiff,side}$	$200aF/\mu m$
n-type source/drain resistivity	R_{ndiff}	$7\Omega/\square$
p-type source/drain resistivity	R_{pdiff}	$7\Omega/\square$
poly-substrate plate capacitance	$C_{poly,plate}$	$63aF/\mu m^2$
poly-substrate fringe capacitance	$C_{poly,fringe}$	$63aF/\mu m$
poly resistivity	R_{poly}	$8\Omega/\square$
metal 1-substrate plate capacitance	$C_{metal1,plate}$	$36aF/\mu m^2$
metal 1-substrate fringe capacitance	$C_{metal1,fringe}$	$54aF/\mu m$
metal 2-substrate capacitance	$C_{metal2,plate}$	$36aF/\mu m^2$
metal 2-substrate fringe capacitance	$C_{metal2,fringe}$	$51aF/\mu m$
metal 3-substrate capacitance	$C_{metal3,plate}$	$37aF/\mu m^2$
metal 3-substrate fringe capacitance	$C_{metal3,fringe}$	$54aF/\mu m$
metal 1 resistivity	R_{metal1}	$0.08\Omega/\square$
metal 2 resistivity	R_{metal2}	$0.08\Omega/\square$
metal 3 resistivity	R_{metal3}	$0.03\Omega/\square$
metal current limit	$I_{m,max}$	$1mA/\mu m$

Typical 180 nm process parameters