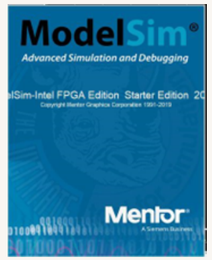
RIPPLE CARRY ADDER (64-bit)

COMPUTER-AIDED DIGITAL DESIGN



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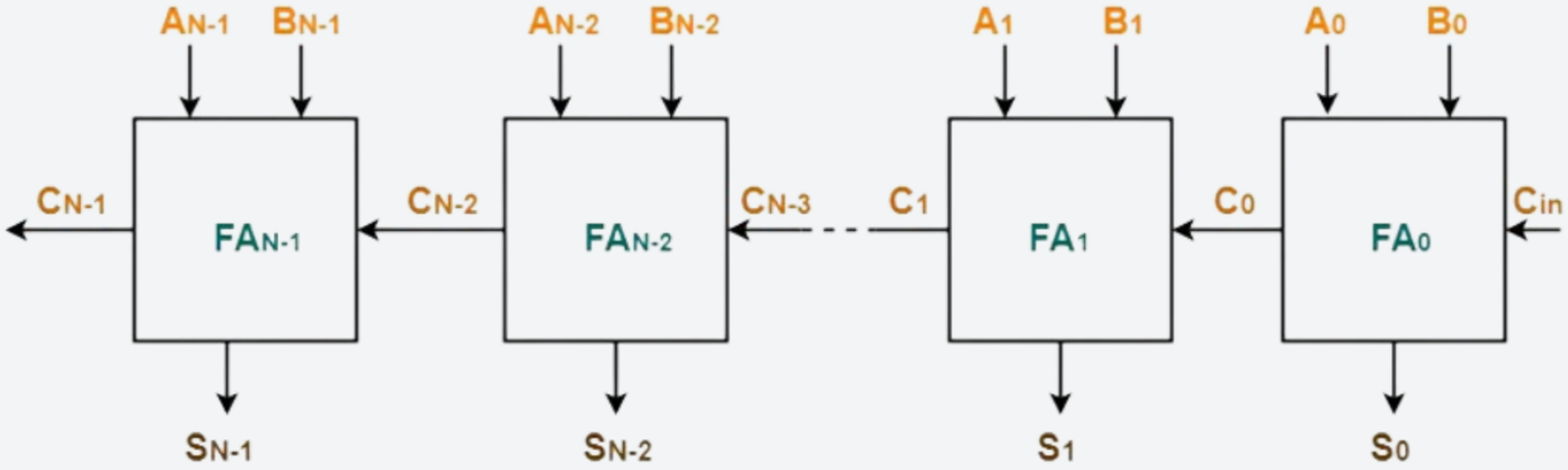


N-bit Ripple Carry Adder

The "ripple" part comes from the fact that the carry ripples through each bit from right to left, just like ripples

A Ripple carry adder is a set of simple binary adders lined up in a row.
The carry-out from each bit's addition passes to the carry-in of the next bit

Slow for large binary numbers because each bit's addition depends on the previous one.

RCA-64bit

↓

16 4-bit FULL ADDERS

↓

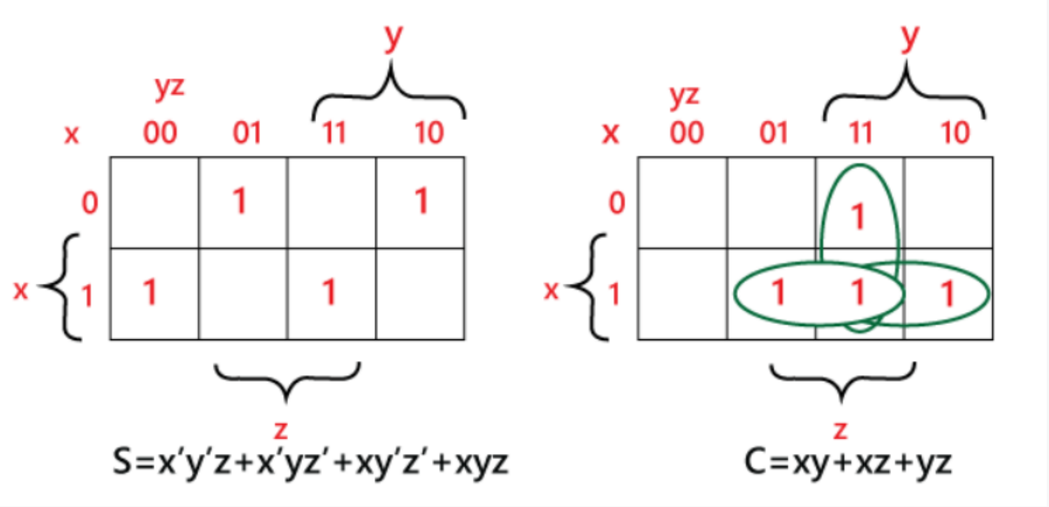
4 1-bit FULL ADDERS

↓

sum & carry

1-BIT FULL ADDER

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

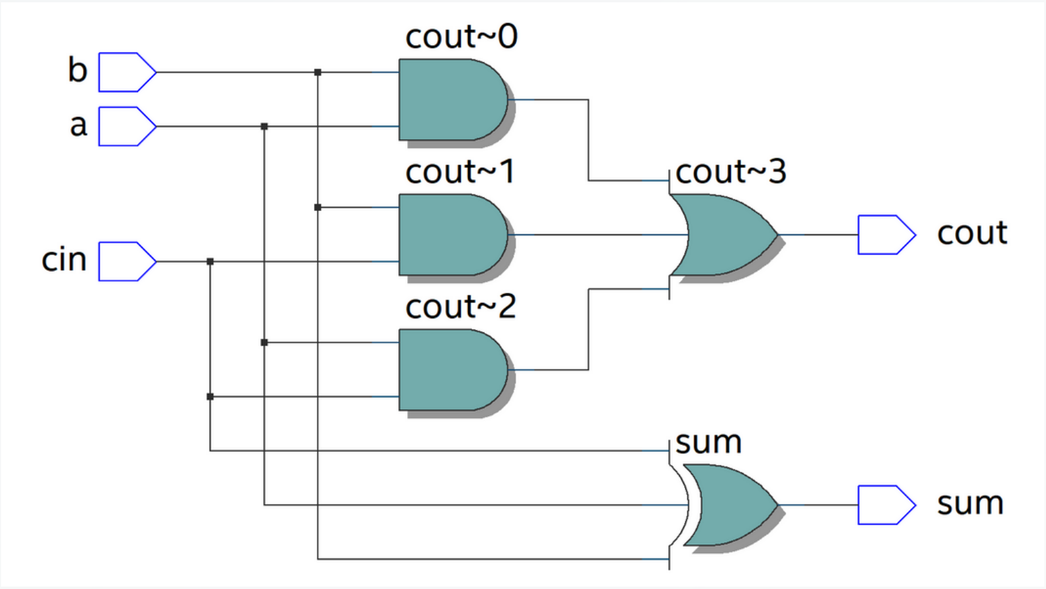


Sum = x' y' z+x' yz+xy' z'+xyz

Carry = xy+xz+yz

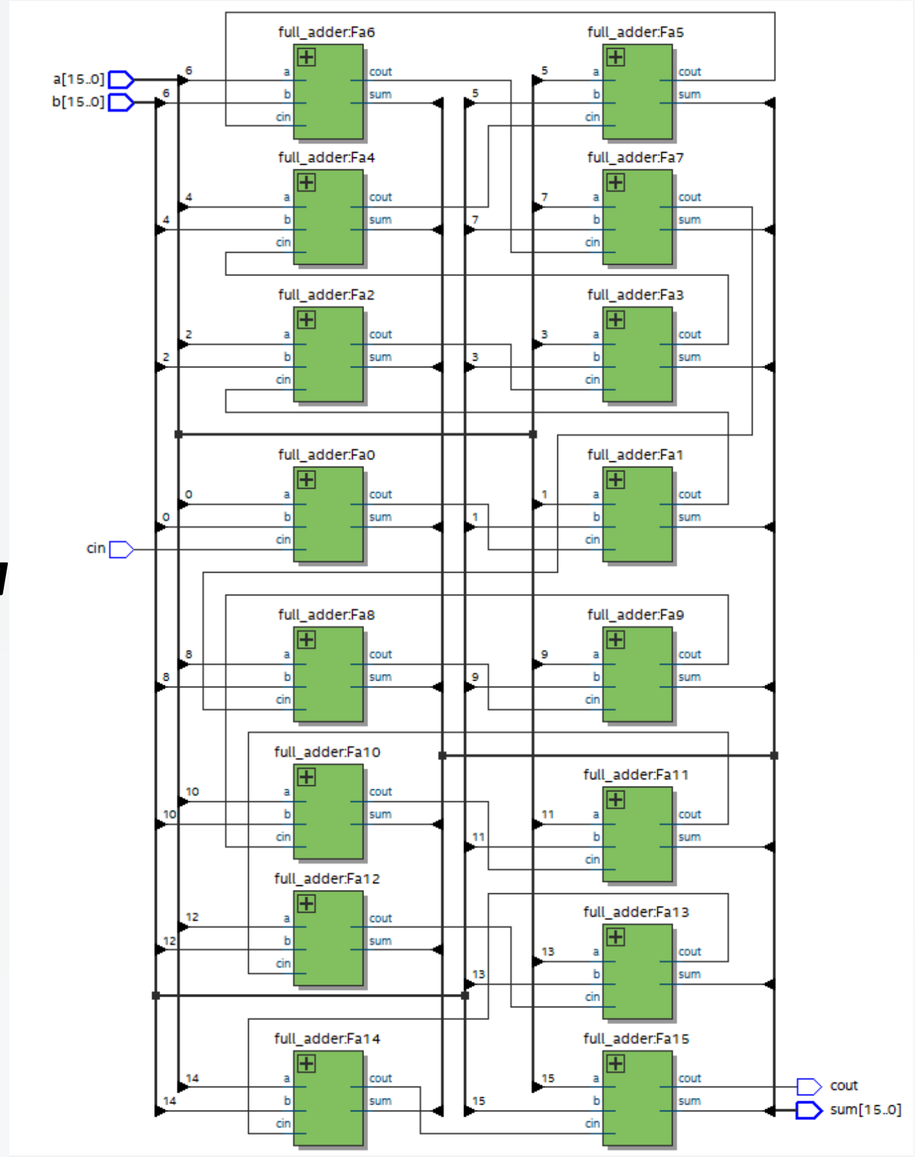
```
1   // full_adder.sv
2   module full_adder(
3       input logic a, b, cin,
4       output logic sum, cout
5   );
6
7       assign sum = a ^ b ^ cin;
8       assign cout = (a & b) | (b & cin) | (a & cin);
9
10  endmodule
11
```

RTL VIEW



1-BIT FULL ADDER
system verilog HDL

RTL VIEW

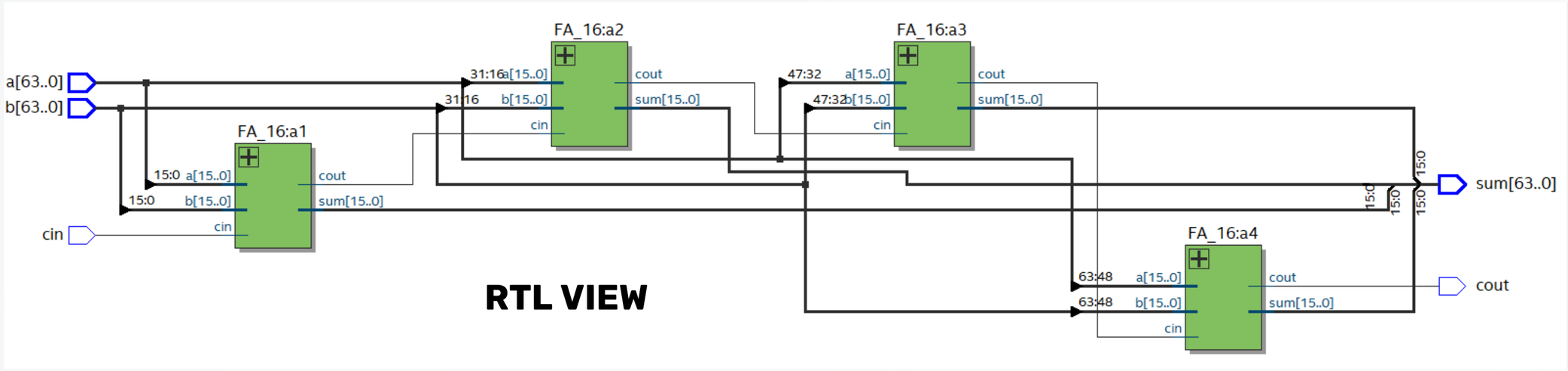



```
1  module FA_16(
2     input logic [15:0] a, b,
3     input logic cin,
4     output logic [15:0] sum,
5     output logic cout);
6
7     wire [14:0]c;
8
9     full_adder Fa0 (a[0],b[0],cin,sum[0],c[0]);
10    full_adder Fa1 (a[1],b[1],c[0],sum[1],c[1]);
11    full_adder Fa2 (a[2],b[2],c[1],sum[2],c[2]);
12    full_adder Fa3 (a[3],b[3],c[2],sum[3],c[3]);
13    full_adder Fa4 (a[4],b[4],c[3],sum[4],c[4]);
14    full_adder Fa5 (a[5],b[5],c[4],sum[5],c[5]);
15    full_adder Fa6 (a[6],b[6],c[5],sum[6],c[6]);
16    full_adder Fa7 (a[7],b[7],c[6],sum[7],c[7]);
17    full_adder Fa8 (a[8],b[8],c[7],sum[8],c[8]);
18    full_adder Fa9 (a[9],b[9],c[8],sum[9],c[9]);
19    full_adder Fa10 (a[10],b[10],c[9],sum[10],c[10]);
20    full_adder Fa11 (a[11],b[11],c[10],sum[11],c[11]);
21    full_adder Fa12 (a[12],b[12],c[11],sum[12],c[12]);
22    full_adder Fa13 (a[13],b[13],c[12],sum[13],c[13]);
23    full_adder Fa14 (a[14],b[14],c[13],sum[14],c[14]);
24    full_adder Fa15 (a[15],b[15],c[14],sum[15],cout);
25
26 endmodule
27
```

16-BIT FULL ADDER
system verilog HDL

64-BIT RIPPLE CARRY ADDER
system verilog HDL

```
1   module RCA_64(
2       input logic [63:0] a, b,
3       input logic cin,
4       output logic [63:0] sum,
5       output logic cout);
6
7       wire [2:0] c;
8
9        FA_16 a1(a[15:0],b[15:0],cin,sum[15:0],c[0]);
10
11       FA_16 a2(a[31:16],b[31:16],c[0],sum[31:16],c[1]);
12
13       FA_16 a3(a[47:32],b[47:32],c[1],sum[47:32],c[2]);
14
15       FA_16 a4(a[63:48],b[63:48],c[2],sum[63:48],cout);
16
17  endmodule
18
```



RTL VIEW

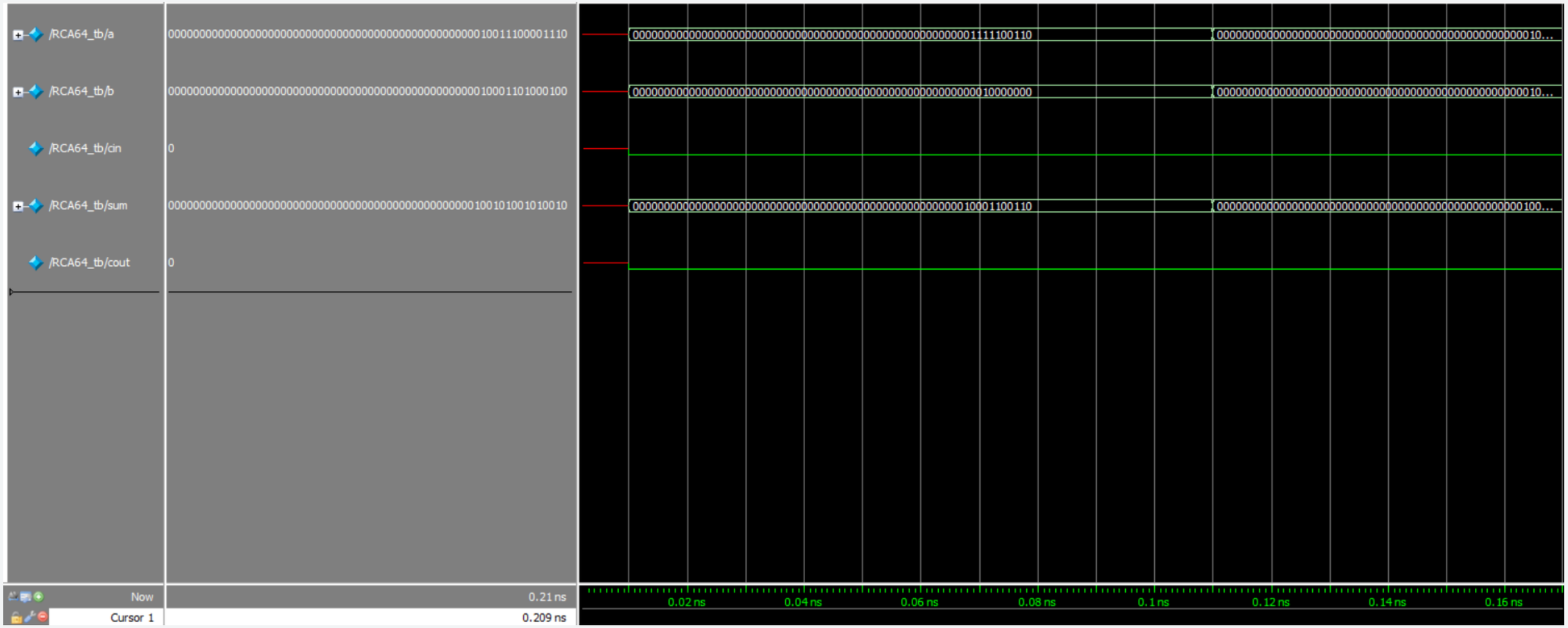
```
1  module RCA64_tb;
2  logic [63:0] sum;//output
3  logic cout;//output
4  logic [63:0] a,b;//input
5  logic cin;//input
6
7  RCA_64 T1(
8  .a(a),
9  .b(b),
10 .cin(cin),
11 .sum(sum),
12 .cout(cout));
13
14 initial begin
15
16 a=0; b=0; cin=0;
17 #10 a=64'd998; b=64'd128;cin=64'd0;
18 #100 a=64'd9998; b=64'd9028;cin=64'd0;
19 #50;
20
21 end
22 endmodule
23
```

TESTBENCH

a=64'd998
b=64'd128

a=64'd9998
b=64'd9028

SIMULATION



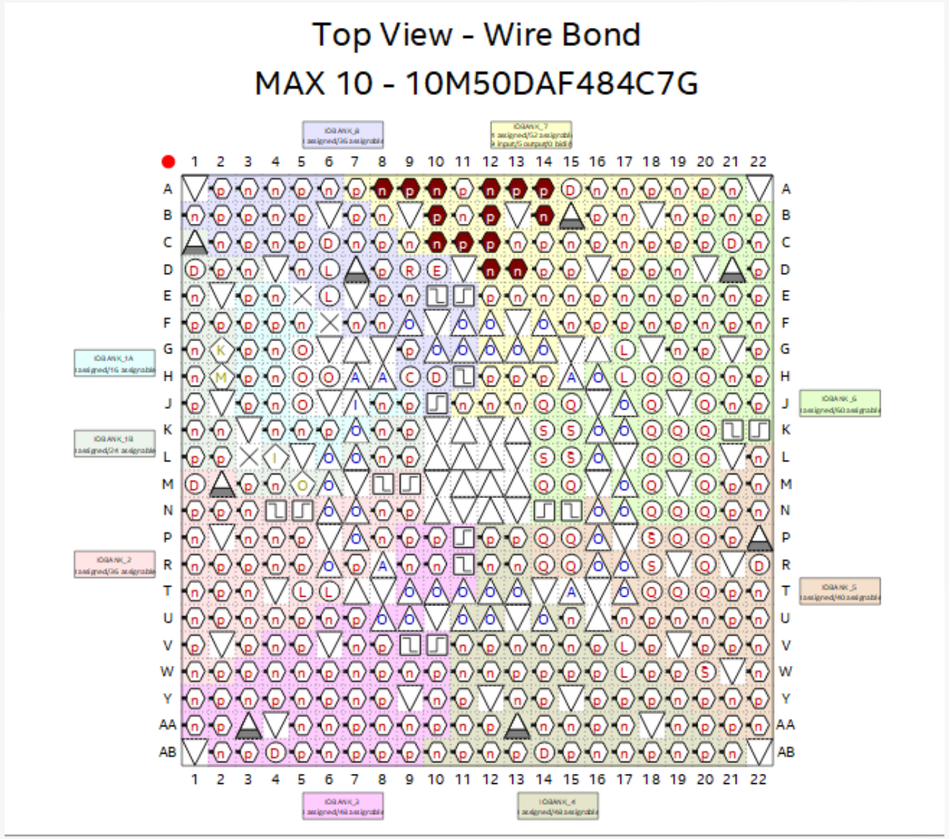
ADDITION OF TWO DECIMAL NUMBERS
a=64'd998; b=64'd128; a=64'd9998; b=64'd9028;

SUM=1126
Cout=0

SUM=25094
Cout=0

PIN PLANNER

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	urrent Streng	Slew Rate
a[3]	Input	PIN_C12	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
a[2]	Input	PIN_D12	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
a[1]	Input	PIN_C11	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
a[0]	Input	PIN_C10	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
b[3]	Input	PIN_A14	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
b[2]	Input	PIN_A13	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
b[1]	Input	PIN_B12	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
b[0]	Input	PIN_A12	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
cin	Input	PIN_B14	7	B7_N0	2.5 V ...fault)	12mA ...ault)	
cout	Output	PIN_D13	7	B7_N0	2.5 V ...fault)	12mA ...ault)	2 (default)
sum[3]	Output	PIN_B10	7	B7_N0	2.5 V ...fault)	12mA ...ault)	2 (default)
sum[2]	Output	PIN_A10	7	B7_N0	2.5 V ...fault)	12mA ...ault)	2 (default)
sum[1]	Output	PIN_A9	7	B7_N0	2.5 V ...fault)	12mA ...ault)	2 (default)
sum[0]	Output	PIN_A8	7	B7_N0	2.5 V ...fault)	12mA ...ault)	2 (default)



THANK YOU

S.KAUSHIK