R15 & R14

Subject Code: R15A22CS04

ANURAG GROUP OF INSTITUTIONS

(Autonomous)

School of Engineering

II- B. Tech- II-Semester End Examinations, April / May - 2018

Subject: Computer Organization

(Common to CSE & IT)

Time: 3 Hours **Max.Marks: 75**

Section—A (Short Answer type questions)

- **Answer All questions** **(25 Marks)**

Q1. What are the different phases of instruction cycle?

Q2. Define an addressing mode? List out different addressing modes?

Q3. Explain pipelining concept.

Q4. How to generate a twenty bit physical address? Explain with an example.

Q5. Give the reason why RAM is volatile?

Q6. Define cache hit ratio?

Q7. Define Handshaking mechanism?

Q8. Explain interrupt initiated I/O.

Q9. Illustrate different characteristics of multiprocessor architectures?

Q10. How do you achieve parallel processing?

Section – B (Essay Type Questions)

- **Answer all the questions, each question carries equal marks (5x10=50Marks)**

Q11. Discuss about types of instruction formats and instruction cycle?

Q12. Illustrate different types of addressing modes?

Q13. Explain the INTEL 8086 CPU architecture with suitable example?

Q14. Write and discuss about Pin Diagram of 8086 Multiprocessor and its configuration details?

Q15. Draw and Explain different mapping techniques of cache memory?

Q16. Discuss and Write in detail about Micro programmed control mechanism with neat diagram including control memory and address sequencing?

Q17. A) Explain about modes of data transfer?

Q18. Draw and explain block diagram of typical DMA controller and DMA transfer?

Q19. List the various interconnection structures and explain them in detail?

Q20. Describe Flynn's Classification with examples?