

Figure: Main memory

Address space

To access a word in memory requires an identifier. Although programmers use a name to identify a word (or a collection of words), at the hardware level each word is identified by an address.

The total number of uniquely identifiable locations in memory is called the **address space**.

For example, a memory with 64 kilobytes and a word size of 1 byte has an address space that ranges from 0 to 65,535.

Example: a byte-addressable 32-bit computer can address $2^{32} = 4,294,967,296$ bytes of memory, or 4 [gibibytes](#) (GiB)

Table **Memory units**

<i>Unit</i>	<i>Exact Number of Bytes</i>	<i>Approximation</i>
kilobyte	2^{10} (1024) bytes	10^3 bytes
megabyte	2^{20} (1,048,576) bytes	10^6 bytes
gigabyte	2^{30} (1,073,741,824) bytes	10^9 bytes
terabyte	2^{40} bytes	10^{12} bytes

Memory addresses are defined using unsigned binary integers

Example 1

A computer has 32 MB (megabytes) of memory. How many bits are needed to address any single byte in memory?

Solution

The memory address space is $32 \text{ MB} = 2^{25} (2^5 \times 2^{20})$.

This means that we need $\log_2 2^{25} = 25 \text{ bits}$, to address each byte.

Example 2

A computer has 128 MB of memory. Each word in this computer is eight bytes. How many bits are needed to address any single word in memory?

Solution: The memory address space is 128 MB, which means 2^{27} . However, each word is eight (2^3) bytes, which means that we have 2^{24} words.

This means that we need $\log_2 2^{24}$, or 24 bits , to address each word.

A SIMPLE COMPUTER

To explain the architecture of computers as well as their instruction processing, we introduce a simple (unrealistic) computer, as shown in next Figure.

Our simple computer has three components: CPU, main memory and an input/output subsystem.

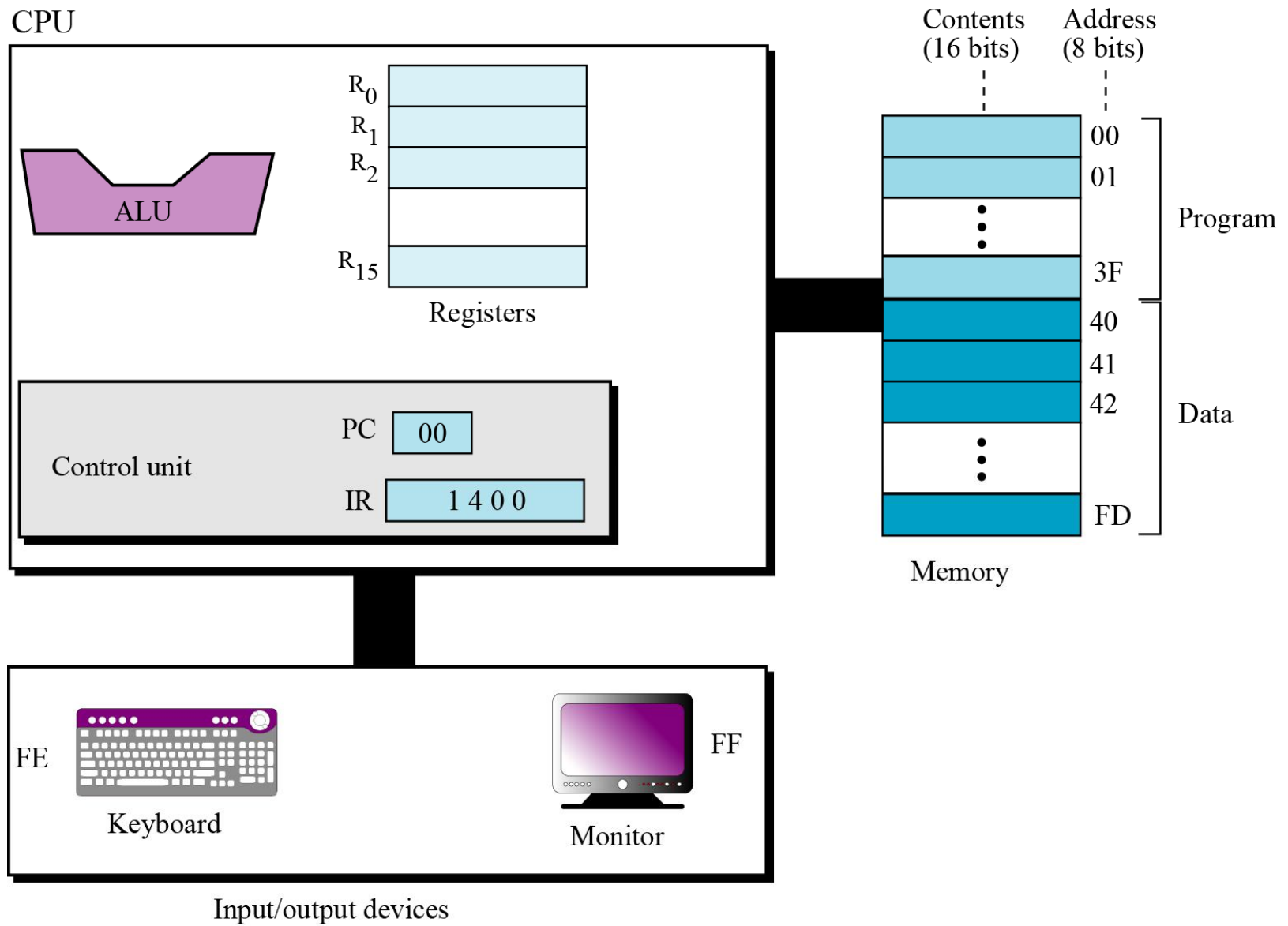


Figure: The components of a simple computer

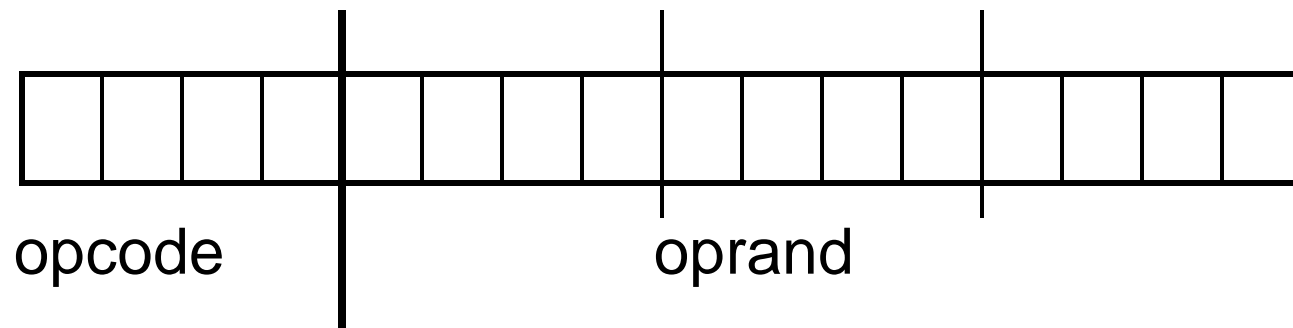
Instruction set

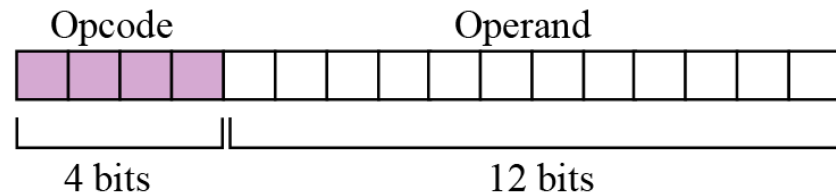
Each computer instruction consists of two parts: the **operation code (opcode)** and the **operand (s)**.

The opcode specifies the type of operation to be performed on the operand (s).

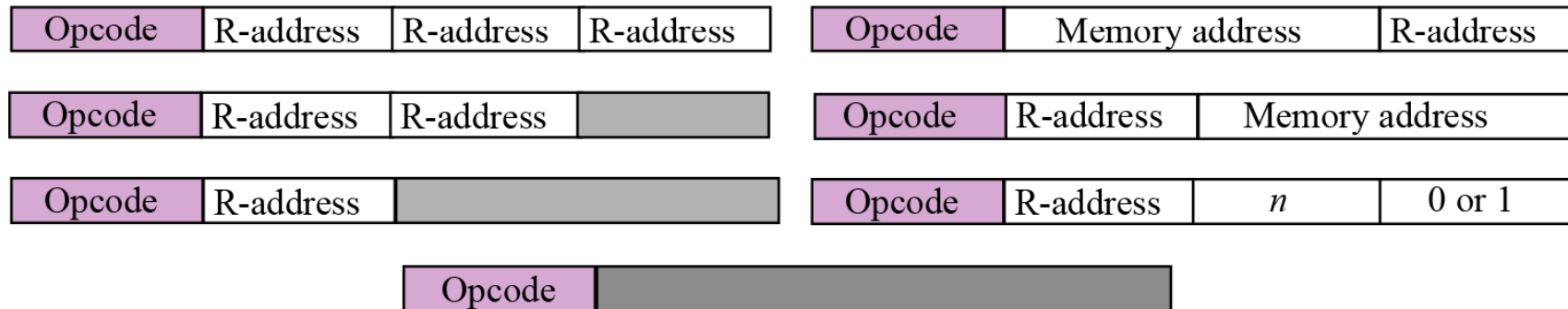
Each instruction consists of sixteen bits divided into four 4-bit fields.

The leftmost field contains the opcode and the other three fields contains the operand or address of operand (s), as shown in next Figure.





a. Instruction format



b. Instruction types

Figure: Format and different instruction types

R-address: address of a register

Memory address: Main memory address

Processing the instructions

Our simple computer, like most computers, uses machine cycles.

A cycle is made of three phases: **fetch**, **decode** and **execute**.

During the fetch phase, the instruction whose address is in PC is obtained from the memory and loaded into the IR. The PC is then incremented to point to the next instruction.

During the decode phase, the instruction in IR is decoded and the required operands are fetched from the register or from memory.

During the execute phase, the instruction is executed and the results are placed in the appropriate memory location or the register.

Once the third phase is completed, the control unit starts the cycle again, but now the PC is pointing to the next instruction. The process continues until the CPU reaches a HALT instruction.

Table List of instructions for the simple computer

Instruction	Code	Operands				Action
	d ₁	d ₂	d ₃	d ₄		
HALT	0				Stops the execution of the program	
LOAD	1	R _D	M _S		R _D ← M _S	
STORE	2	M _D		R _S	M _D ← R _S	
ADDI	3	R _D	R _{S1}	R _{S2}	R _D ← R _{S1} + R _{S2}	
ADDF	4	R _D	R _{S1}	R _{S2}	R _D ← R _{S1} + R _{S2}	
MOVE	5	R _D	R _S		R _D ← R _S	
NOT	6	R _D	R _S		R _D ← $\overline{R_S}$	
AND	7	R _D	R _{S1}	R _{S2}	R _D ← R _{S1} AND R _{S2}	
OR	8	R _D	R _{S1}	R _{S2}	R _D ← R _{S1} OR R _{S2}	
XOR	9	R _D	R _{S1}	R _{S2}	R _D ← R _{S1} XOR R _{S2}	
INC	A	R			R ← R + 1	
DEC	B	R			R ← R – 1	
ROTATE	C	R	n	0 or 1	Rot _n R	
JUMP	D	R	n		IF R ₀ ≠ R then PC = n, otherwise continue	

Key: R_S, R_{S1}, R_{S2}: Hexadecimal address of source registers
R_D: Hexadecimal address of destination register
M_S: Hexadecimal address of source memory location
M_D: Hexadecimal address of destination memory location
n: hexadecimal number
d₁, d₂, d₃, d₄: First, second, third, and fourth hexadecimal digits

An example

Let us show how our simple computer can add two integers A and B and create the result as C . We assume that integers are in two's complement format. Mathematically, we show this operation as:

$$C = A + B$$

We assume that the first two integers are stored in memory locations $(40)_{16}$ and $(41)_{16}$ and the result should be stored in memory location $(42)_{16}$.

To do the simple addition needs five instructions, as shown next:

1. Load the contents of M_{40} into register R_0 ($R_0 \leftarrow M_{40}$).
2. Load the contents of M_{41} into register R_1 ($R_1 \leftarrow M_{41}$).
3. Add the contents of R_0 and R_1 and place the result in R_2 ($R_2 \leftarrow R_0 + R_1$).
4. Store the contents R_2 in M_{42} ($M_{42} \leftarrow R_2$).
5. Halt.

In the language of our simple computer, these five instructions are encoded as:

<i>Code</i>	<i>Interpretation</i>			
$(1040)_{16}$	1: LOAD	0: R_0	40: M_{40}	
$(1141)_{16}$	1: LOAD	1: R_1	41: M_{41}	
$(3201)_{16}$	3: ADDI	2: R_2	0: R_0	1: R_1
$(2422)_{16}$	2: STORE	42: M_{42}		2: R_2
$(0000)_{16}$	0: HALT			

Storing program and data

We can store the five-line program in memory starting from location $(00)_{16}$ to $(04)_{16}$.

We already know that the data needs to be stored in memory locations $(40)_{16}$, $(41)_{16}$, and $(42)_{16}$.

Cycles

Our computer uses one cycle per instruction. If we have a small program with five instructions, we need five cycles. We also know that each cycle is normally made up of three steps: fetch, decode, execute.

Assume for the moment that we need to add $161 + 254 = 415$. The numbers are shown in memory in hexadecimal is, $(00A1)_{16}$, $(00FE)_{16}$, and $(019F)_{16}$.

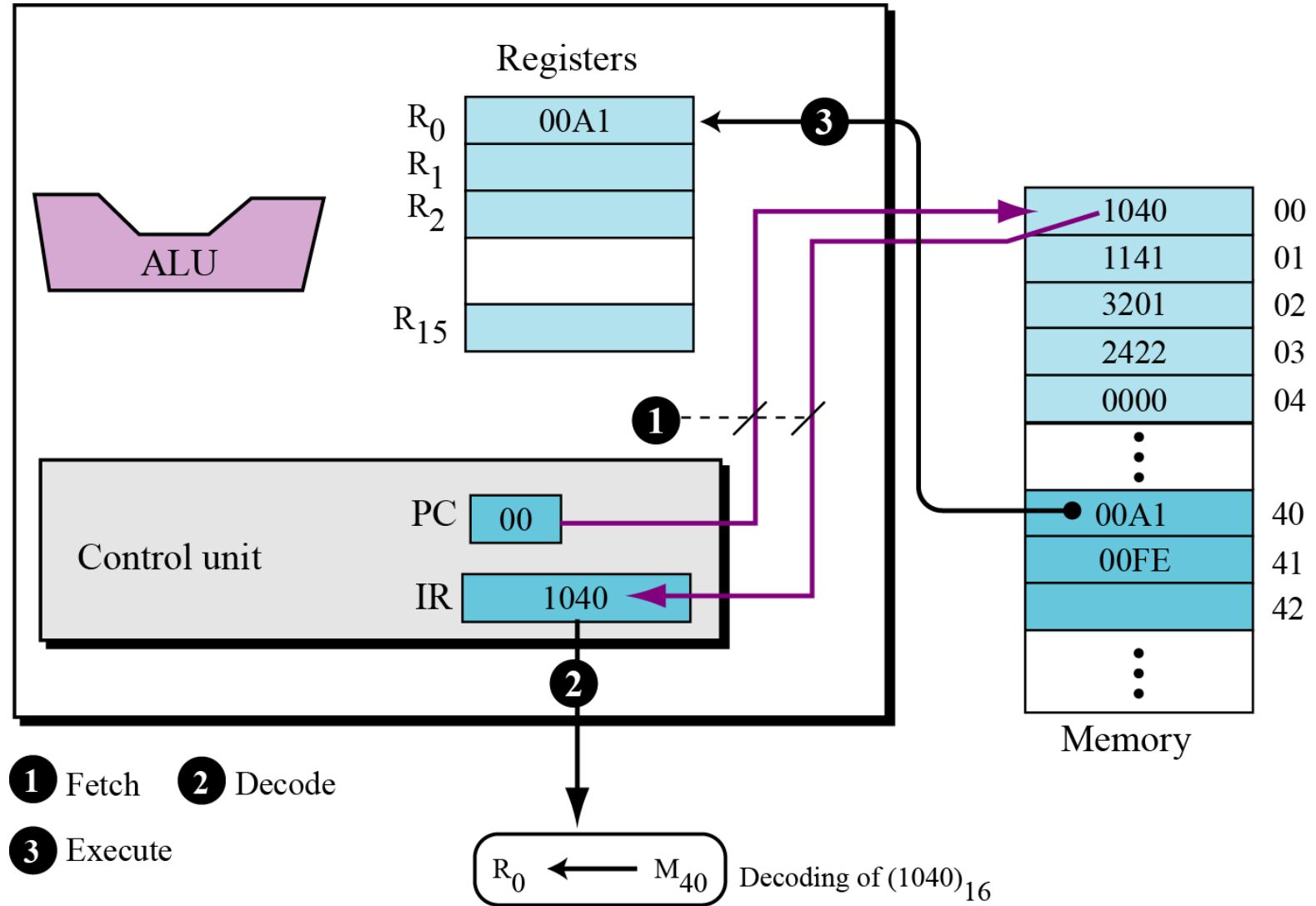


Figure Status of cycle 1

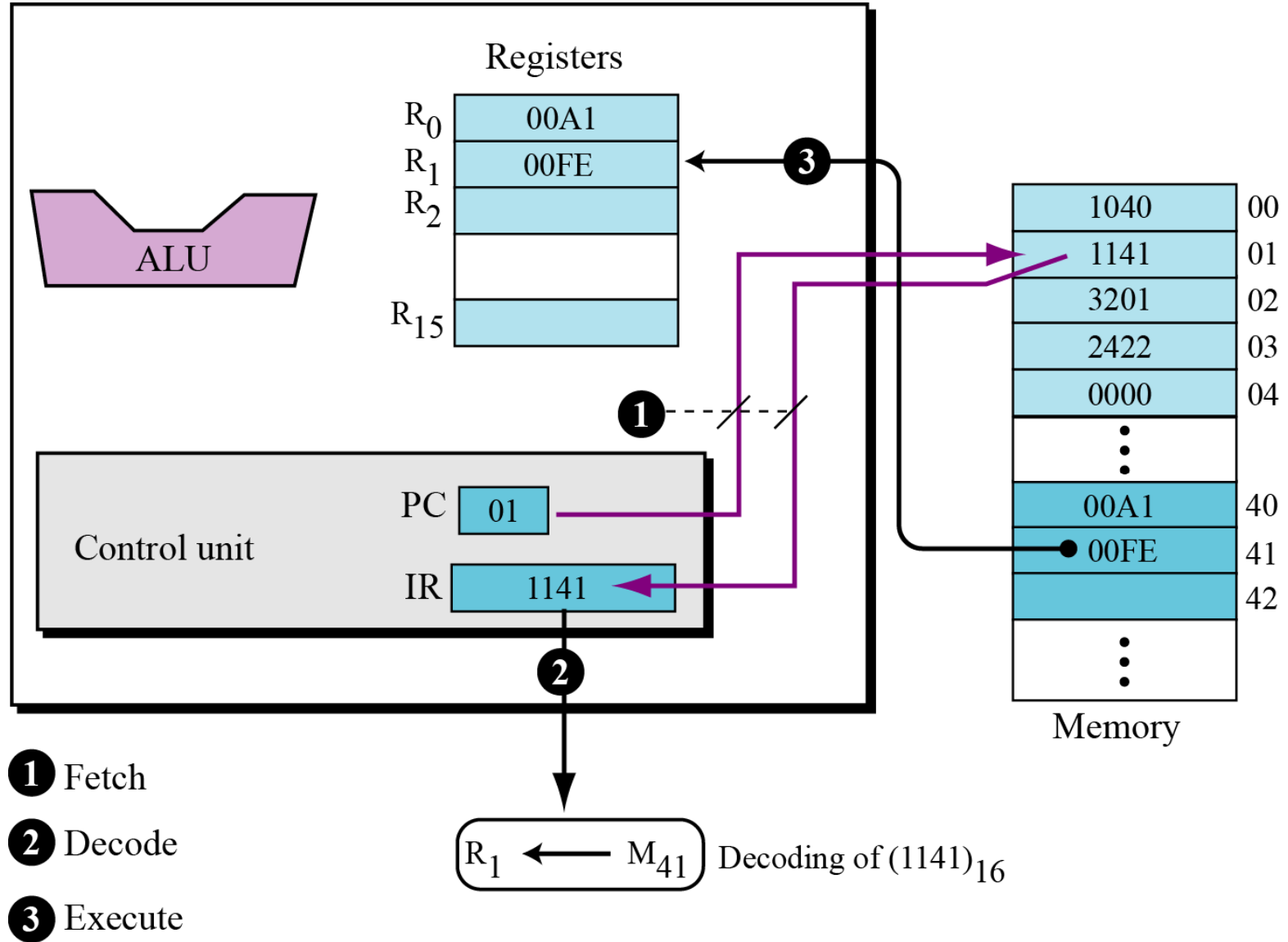


Figure Status of cycle 2

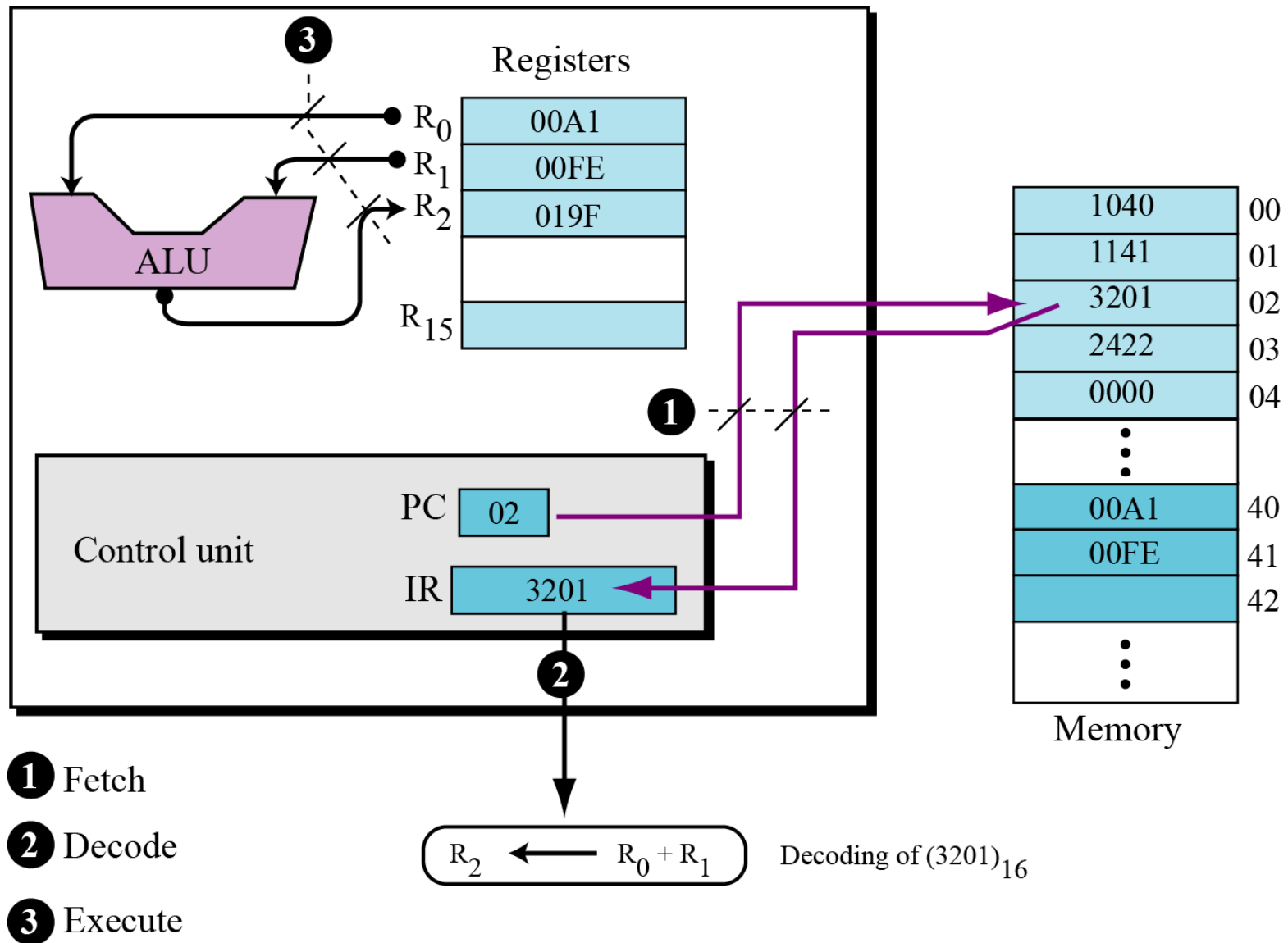


Figure: Status of cycle 3

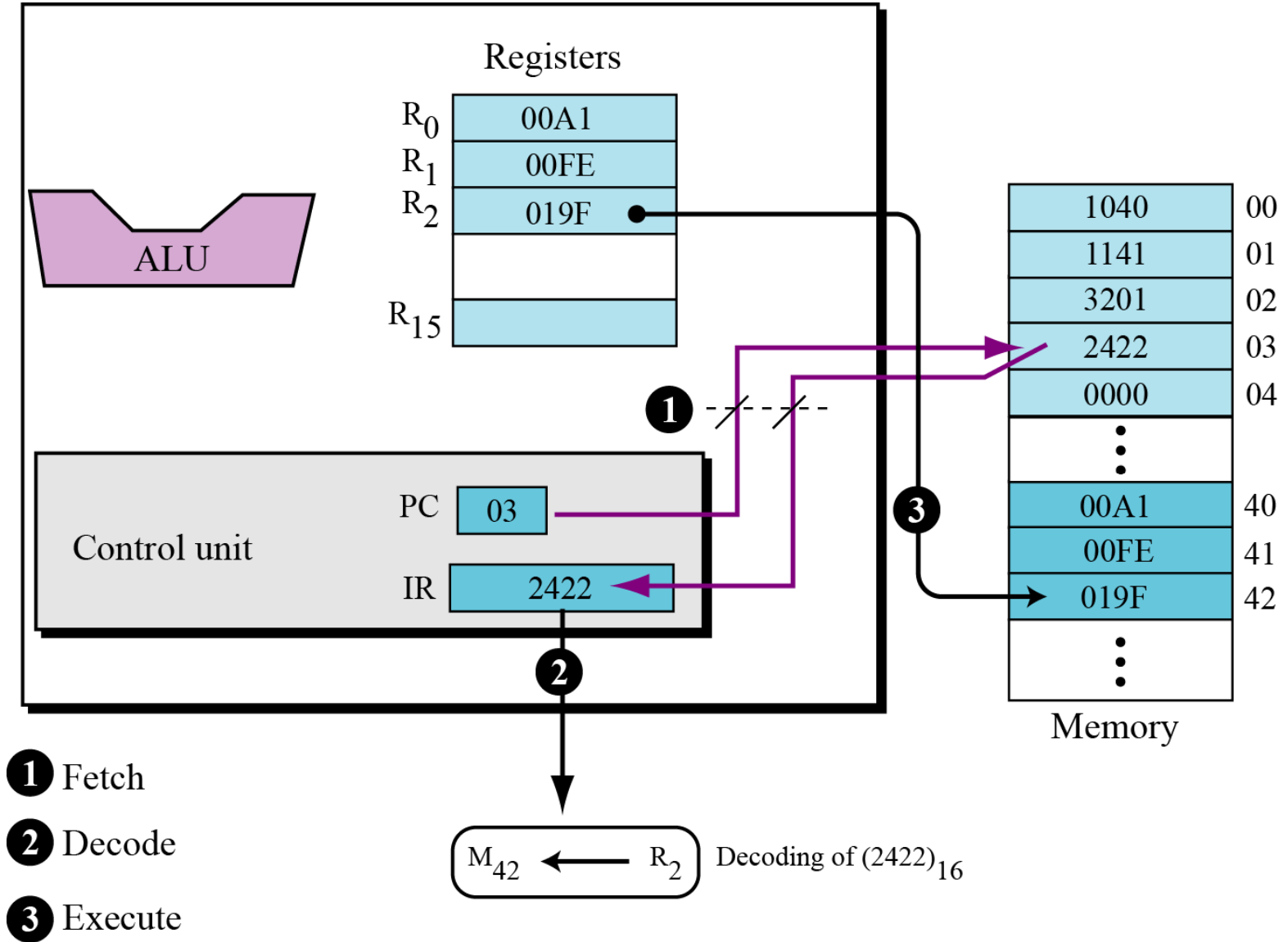


Figure: Status of cycle 4

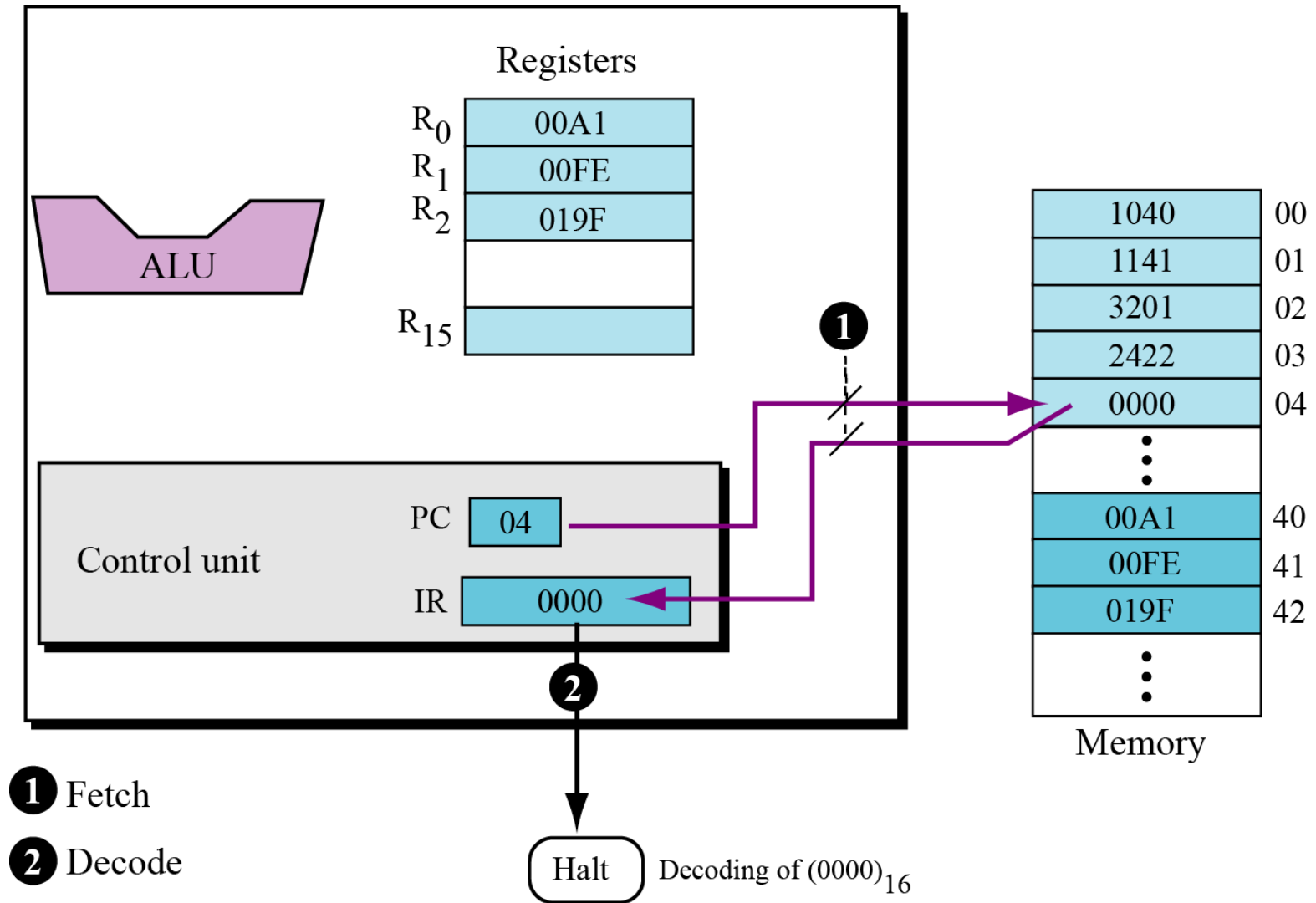


Figure: Status of cycle 5

Prerequisites

- Algorithm complexity: **Big Oh** notation
- Java/c++

PROGRAM EXECUTION

Today, **general-purpose computers** use a set of instructions called a **program** to process data.

A computer executes the program to create output data from input data.

Machine cycle

The CPU uses repeating **machine cycles** to execute instructions in the program, one by one, from beginning to end. A simplified cycle can consist of three phases: **fetch**, **decode** and **execute**

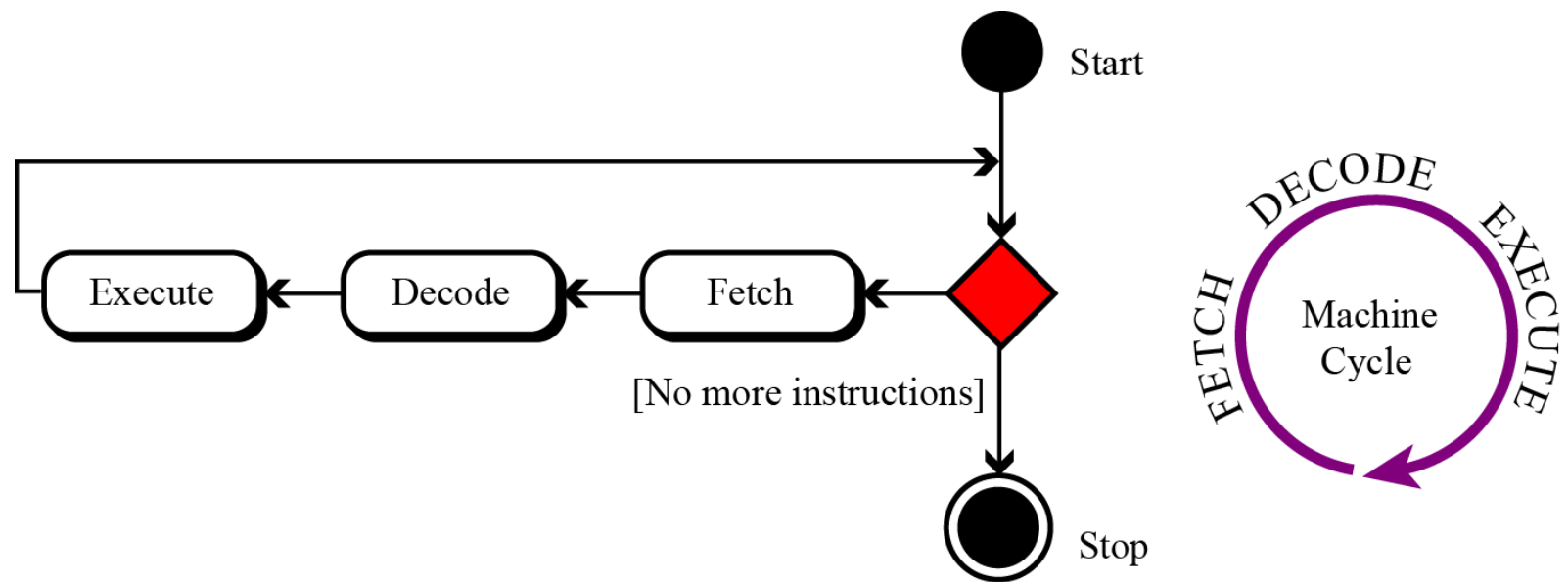


Figure: The steps of a cycle

Complexity

In general, we are not so much interested in the time and space complexity for small inputs

For example, while the difference in time complexity between linear and binary search is meaningless for a sequence with $n = 10$, but it is significant for $n = 2^{30}$

Complexity

For example, let us assume two algorithms A and B that solve the same class of problems.

The time complexity of A is **$5,000n$** , the one for B is **1.1^n** for an input with n elements.

For $n = 10$, A requires 50,000 steps, but B only 3, so B seems to be superior to A.

For $n = 1000$, however, A requires 5,000,000 steps, while B requires $2.5 \cdot 10^{41}$ steps.

Complexity

- **Comparison:** time complexity of algorithms A and B

Input Size	Algorithm A	Algorithm B
n	$5,000n$	1.1^n
10	50,000	3
100	500,000	13,781
1,000	5,000,000	2.5×10^{41}
1,000,000	5×10^9	4.8×10^{41392}