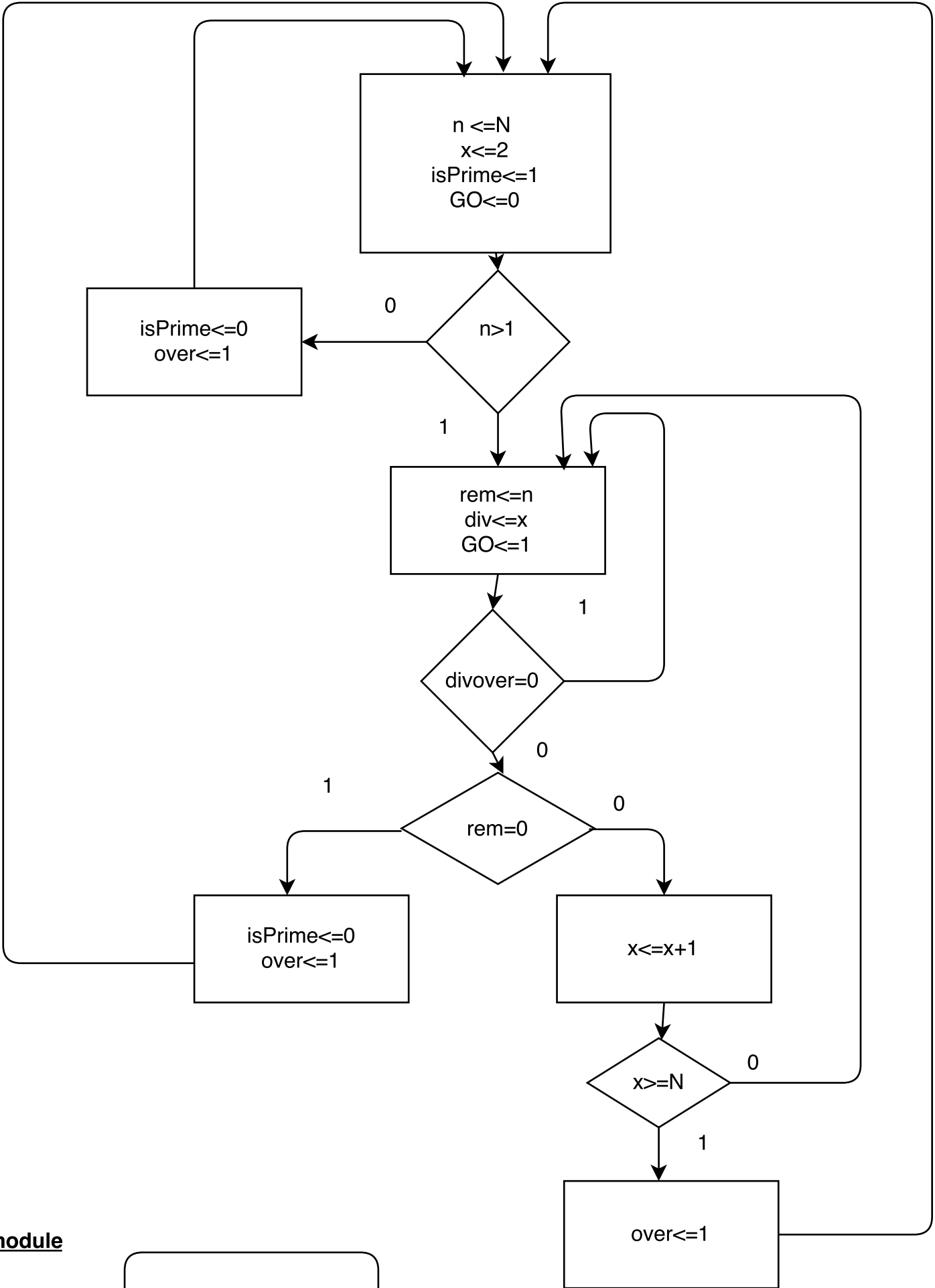


isPrime module

Input ports: N

Output ports: isPrime



Divide module

Input ports: n,x

Output ports rem,divover

