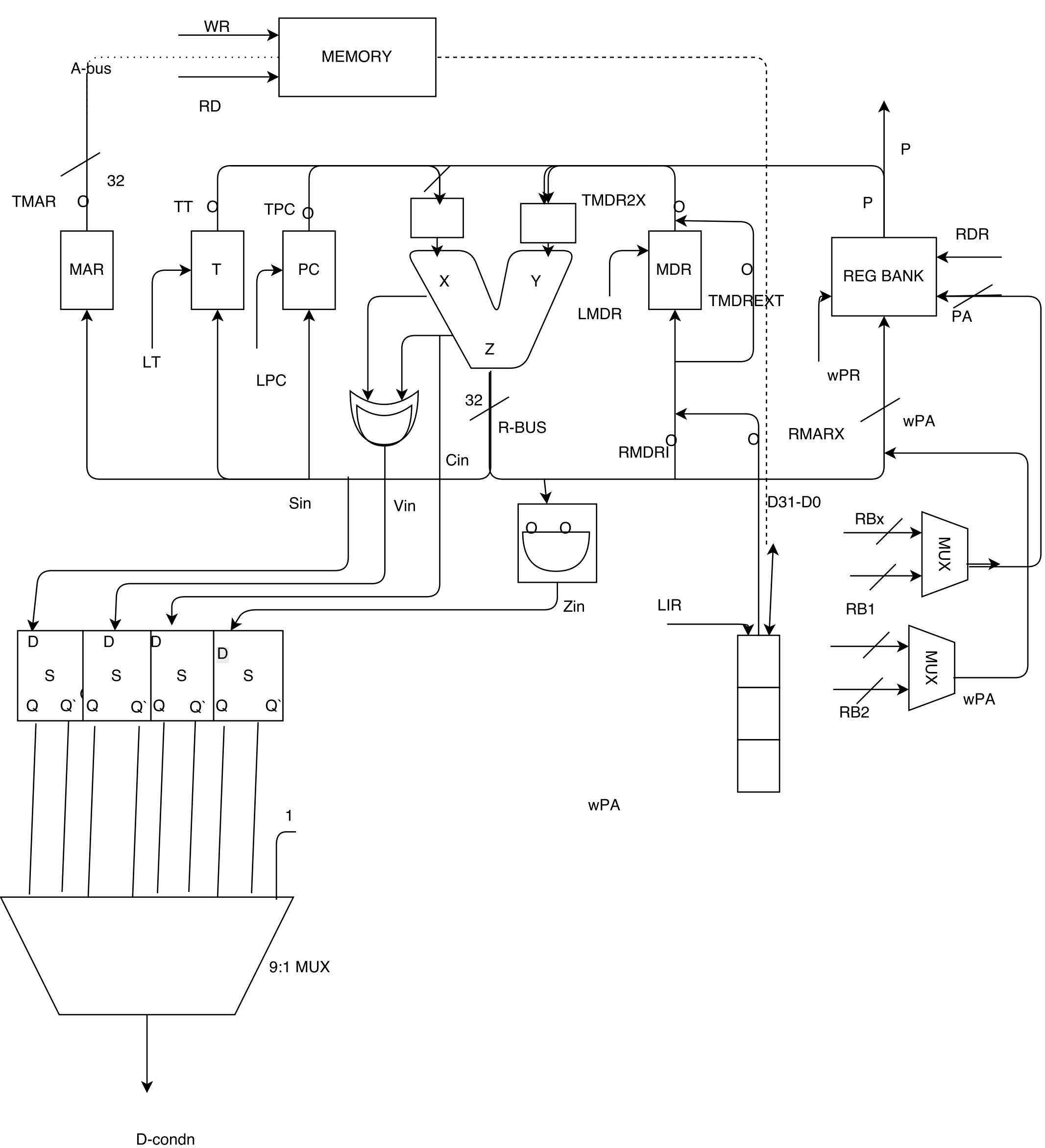


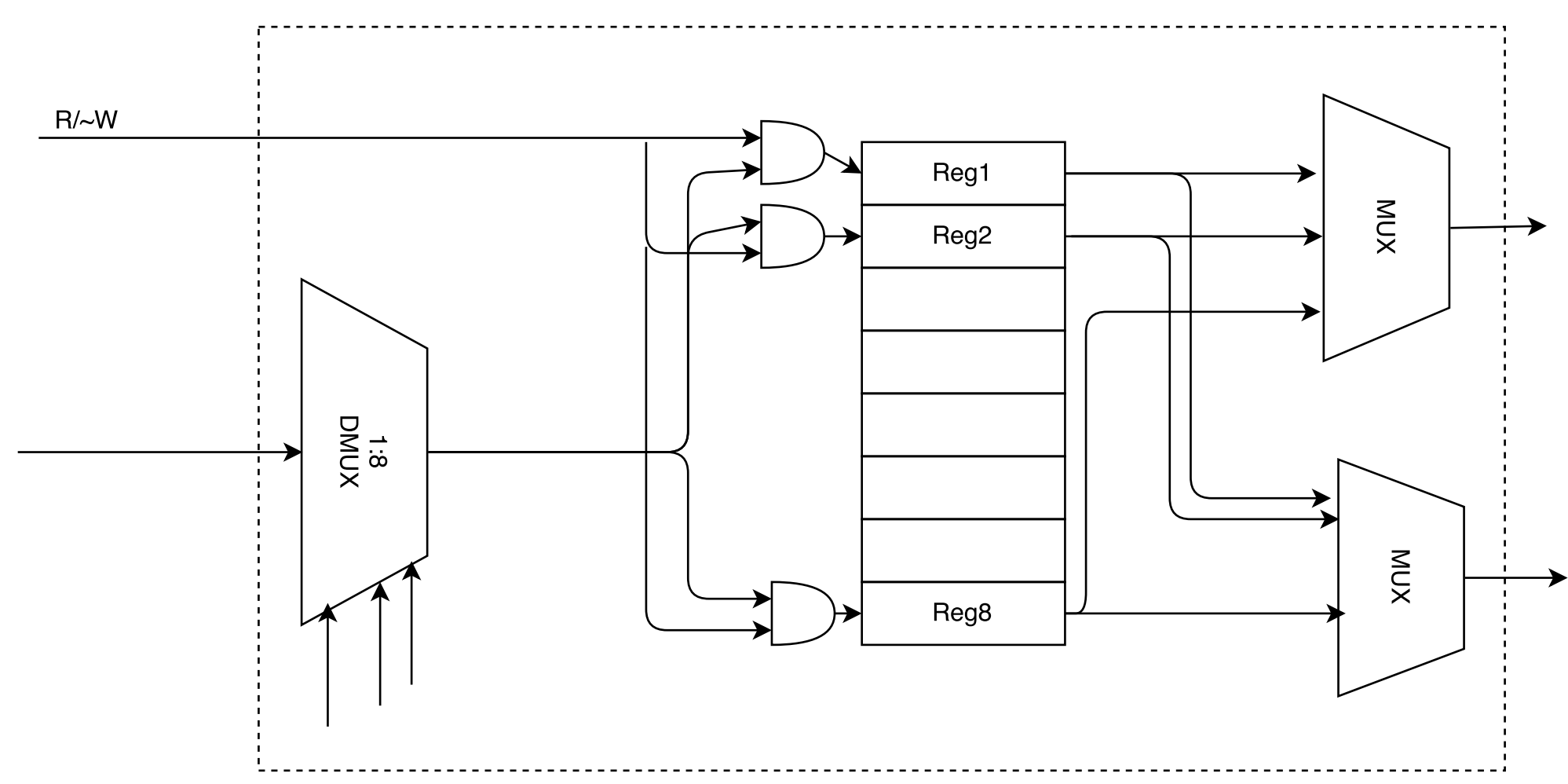
DATAPATH FOR CPU DESIGN

14CS30011 Kaustubh Hiware
14CS30027 Rameshwar Bhaskaran

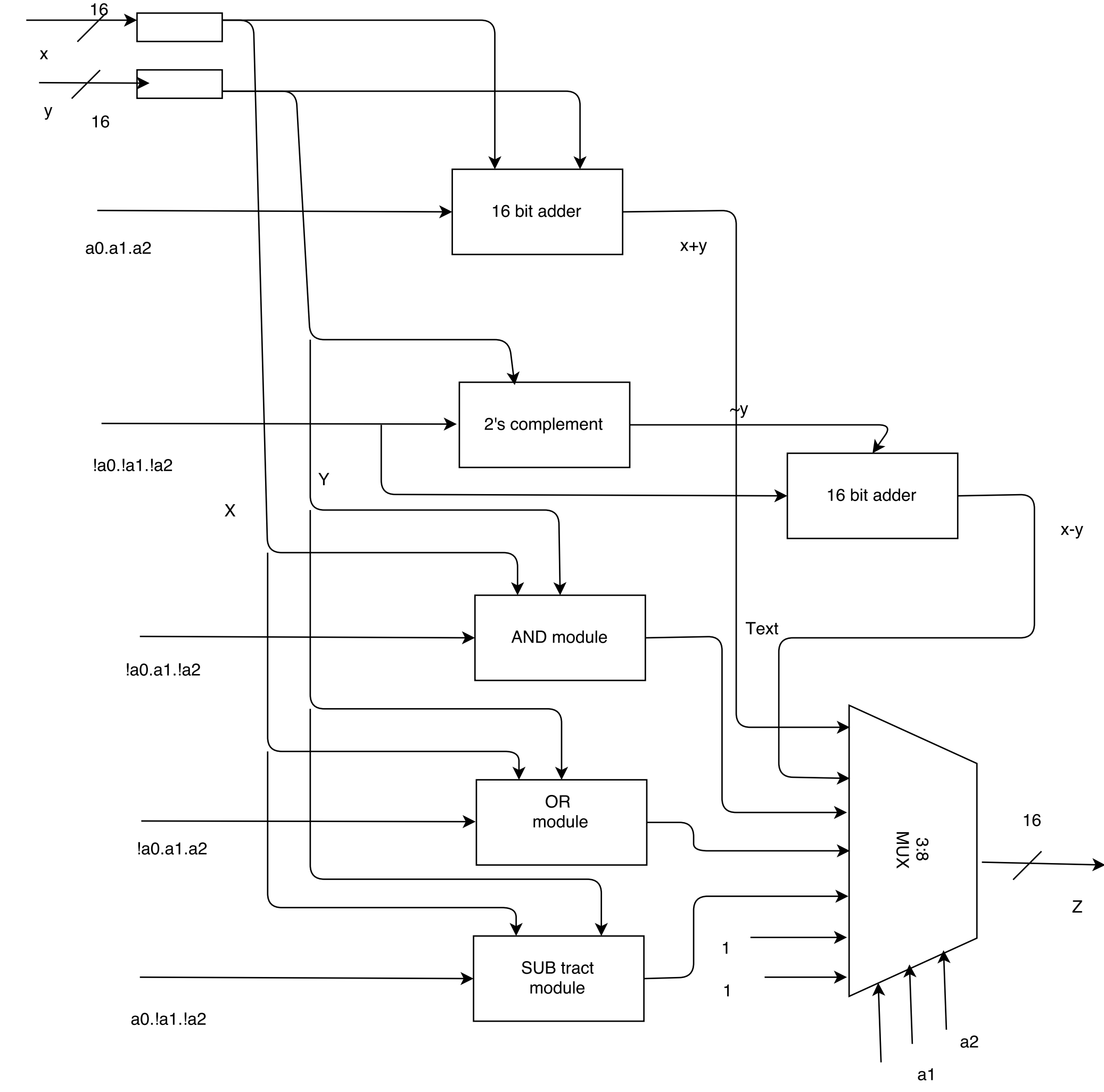
Group 17



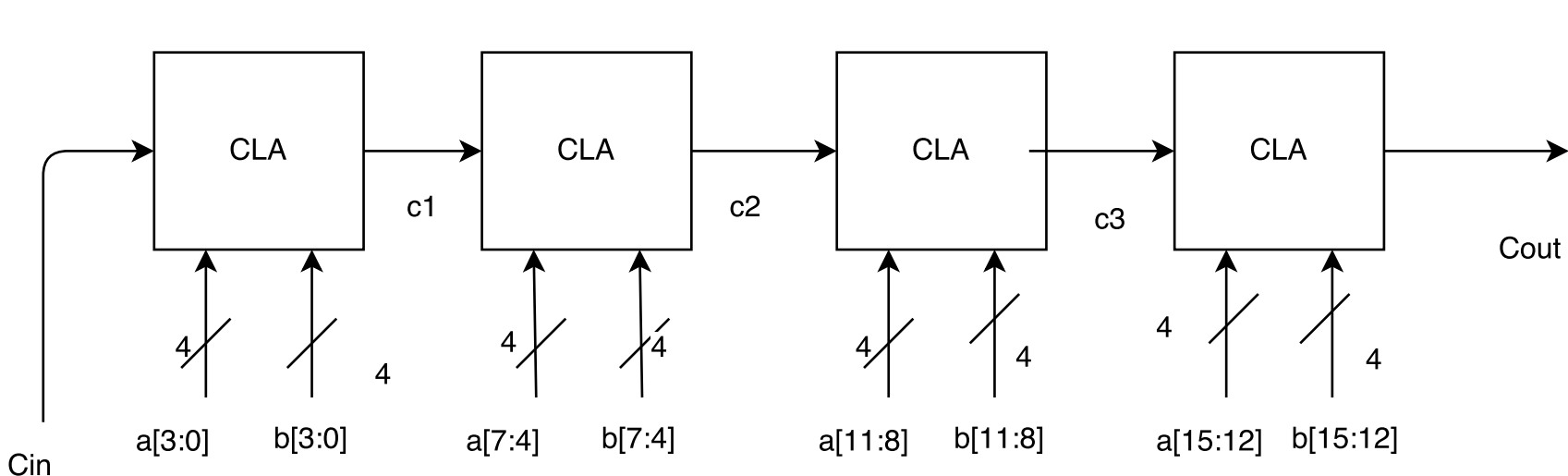
REGISTER BANK



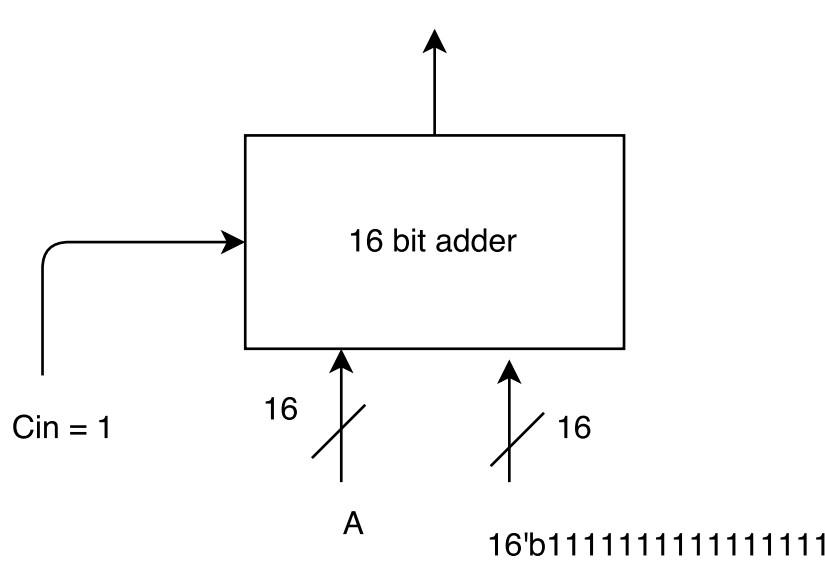
ALU



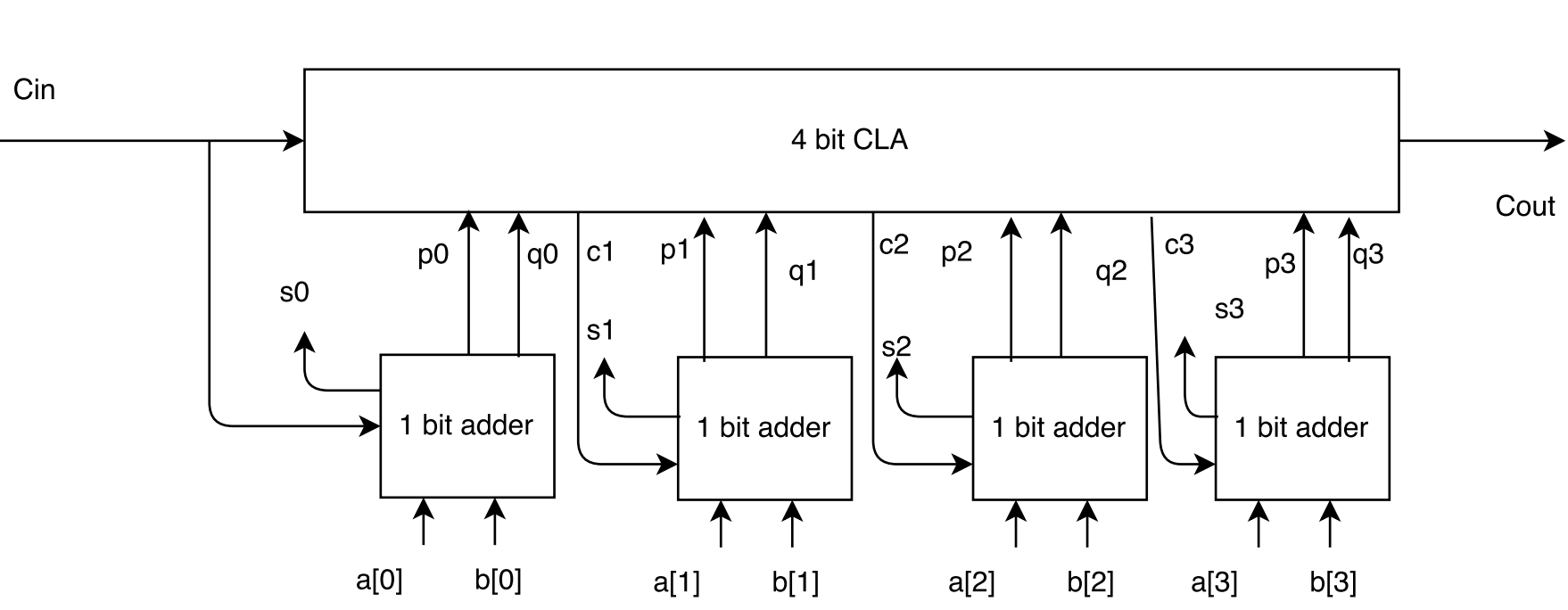
16 bit adder



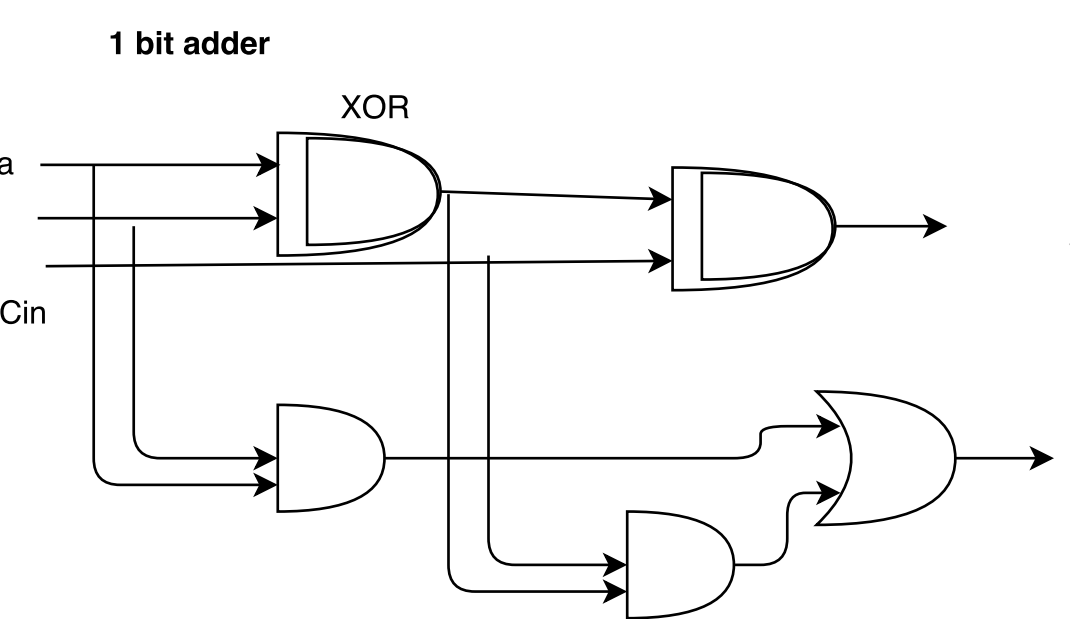
2's complement



Carry Look Ahead Adder



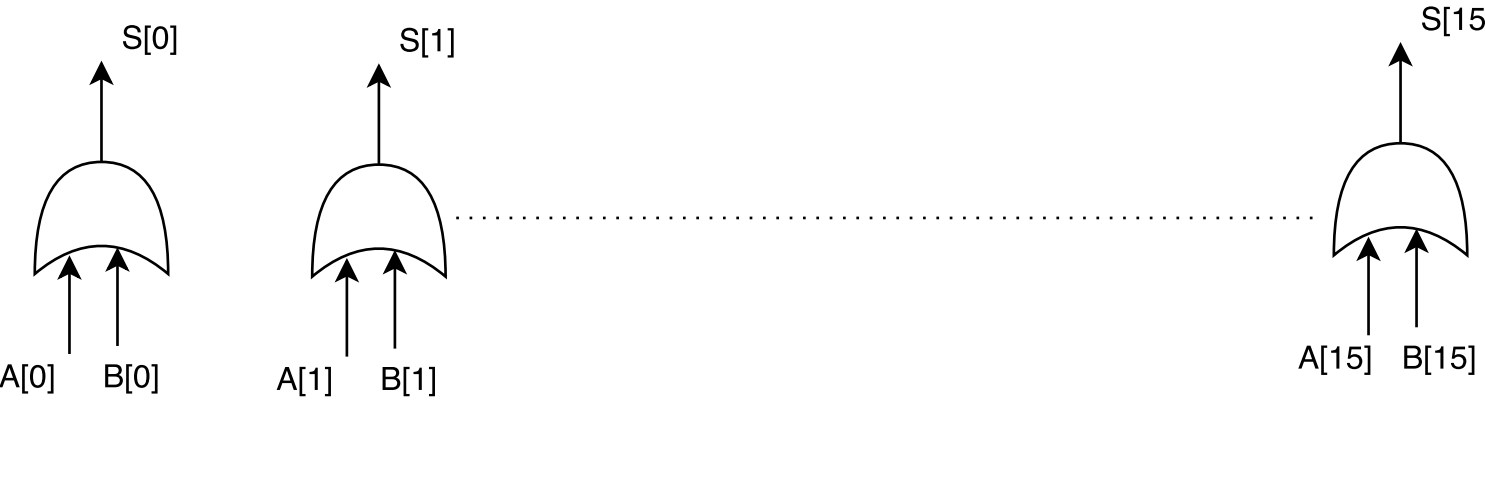
1 bit adder



AND MODULE



OR MODULE



SUBTRACT MODULE

