

VLSI Digital Lab Report

Assignment: CORDIC

Group 20

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Note:

i) The theta is considered as $64 \rightarrow \pi/4$

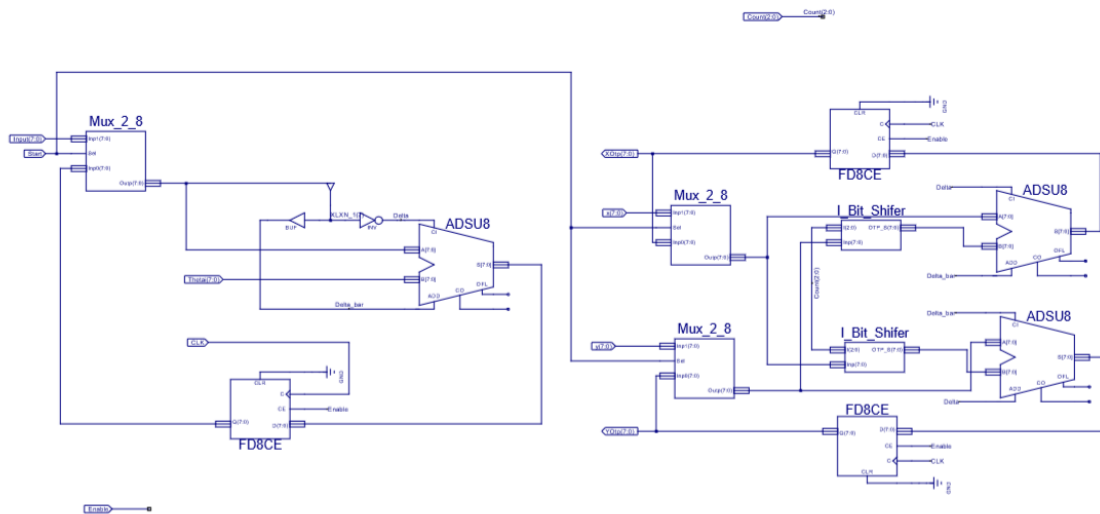
ii) Initial vector is (64, 0). Hence Sine and Cosine value will be $OTPX/64$ and $OTPY/64$ resp.

1. Objective

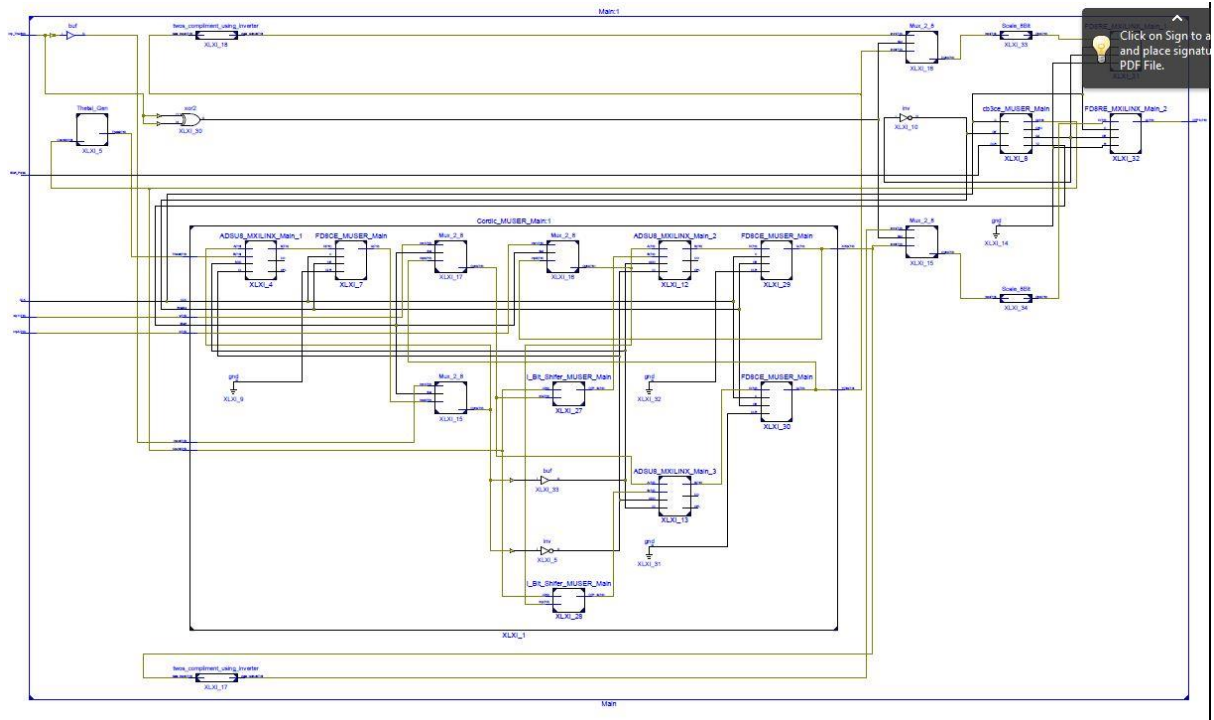
To make a CORDIC Block with following features:-

- 1.1.1. 8 Bit operation
- 1.1.2. Completely Structural
- 1.1.3. All 4 Quadrant compatible

2. Block Diagram



3. RTL Schematic



4. Timing Summary:

Speed Grade: -4

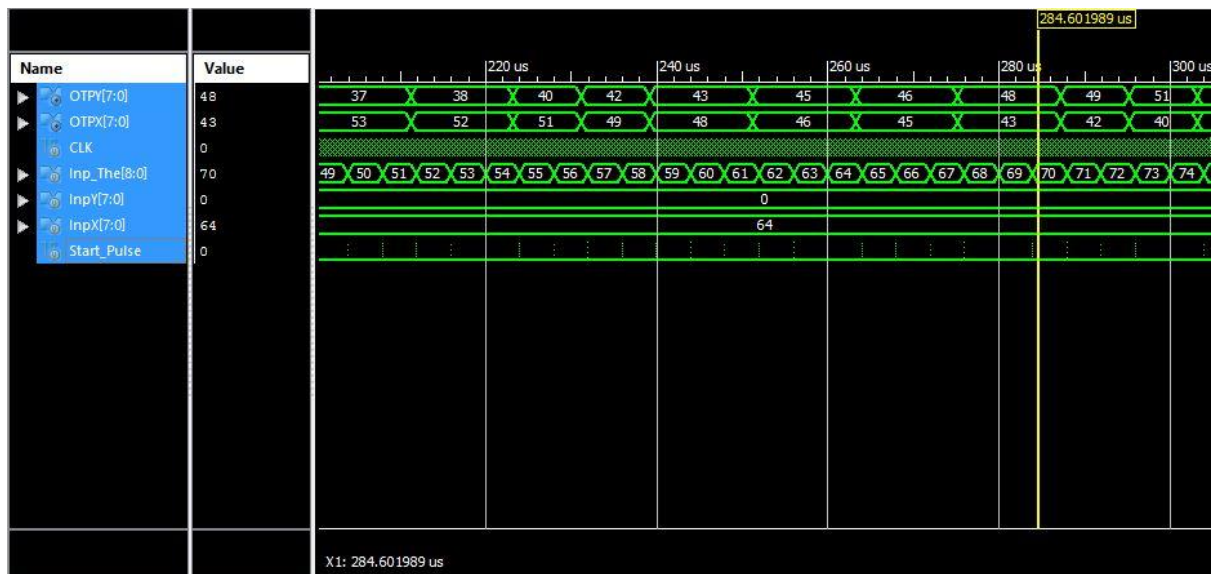
Minimum period: 28.018ns (Maximum Frequency: 35.691MHz)

Minimum input arrival time before clock: 21.326ns

Maximum output required time after clock: 4.283ns

Maximum combinational path delay: No path found

5. Post Route Simulation



6. Expected result and Observation

Sr. No.	Angle(deg)		Expected Output		Observation	
	Deg	Inp	y	x	y	x
1	10	14.22	11.11	63.02	10	64
2	30	42.66	32	55.42	31	56
3	45	64	45.25	45.25	45	46
4	60	85.33	55.42	32	56	31
5	90	128	64	0	66	0

7. Discussion

- 7.1.1. Conventional CORDIC produce bit erroneous output in the case of small angles while scaling free CORDIC is suitable for small angle but not for larger angles.
- 7.1.2. In conventional CORDIC a scaling factor is multiplied with the result obtained.
- 7.1.3. Special care as to be taken while deciding the number of bits since the accumulator can overflow. So maximum value that can be given to CORDIC is $2^{b-1} * 0.609$ where b is the number of bits.
- 7.1.4. For making the block applicable for all 4 quadrants appropriate scaling is given to input theta.
- 7.1.5. For changing sign of the input depending on the quadrant of the input theta multiplexing is done between outputs of the CORDIC block and their two's complement is done. Last two bits of the input theta is used for sensing the quadrants.