Sardar Patel Institute of Technology

Munshi Nagar Andheri (West), Mumbai-400 058

Electronic and Telecommunication Engineering Department

Academic Year: 2021-2022

Weekly Progress Report

Class: B.E Electronics & Telecommunication (Sem VII) Subject: ETP71: Major Project - I

Sr. No.	Week	Progress Achieved	Guide Remark	Guide Sign
1	30 Aug – 5 Sep	Request for project mentorship and approval of project topic.		
2	6 – 12 Sep	Literature review on Filter Banks and Trans-multiplexers.		
3	13 – 19 Sep	Literature review on Wavelet Transform and related topics.		
4	20 -26 Sep	Literature review on WT-based Filter Banks and simulation software.		
5	27 Sep – 3 Oct	Finalizing project outcomes and objectives and preparation for Phase – I presentation.		
6	4 – 10 Oct	Phase – I evaluation and related discussions.		
7	11 – 17 Oct	Designing of system flow and functional parameters.		
8	18 – 24 Oct	Translation of Filter Design algorithms to work with proposed system.		
9	25 – 31 Oct	Implementation of algorithm on MATLAB.		
10	1 – 7 Nov	Designing example system using given system parameters and plotting the overall response.		
11	8 – 14 Nov	Prototyping system simulation using designed filters in MATLAB.		
12	15 – 21 Nov	Implementing the system in MATLAB using designed filters.		
13	22 – 28 Nov	Phase – II evaluation and related discussions.		
14	29 Nov – 5 Dec	Preparing documentation for Phase – II evaluation.		
15	6 – 12 Dec	Performing preliminary testing of the system using various parameters.		

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Weekly Progress Report

Class: B.E Electronics & Telecommunication (Sem VIII) Subject: ETP81: Major Project - II

Sr. No.	Week	Progress Achieved	Guide Remark	Guide Sign
1	17 - 23 Jan	Review of various channel models and wavelet families for system simulation.		
2	24 - 30 Jan	. System simulation using various parameters and channel models.		
3	31 Jan – 6 Feb	Implementation of Conventional system		
4	7 -13 Feb	Simulation of Conventional system under similar parameters.		
5	14 - 20 Feb	Comparison of Conventional and Proposed system, Plotting graphs		
6	21 - 27 Feb	Optimization of system to improve performance.		
7	28 Feb – 6 Mar	Running more intensive simulations to get better understanding of system performance.		
8	7 – 13 Mar	Preparing documentation and PPT for Phase – III presentation		
9	14 - 20 Mar	Translating MATLAB inbuilt functions to HDL Coder compatible functions.		
10	21 - 27 Mar	Writing scripts for HDL Coder and test bench for the system.		
11	28 Mar -3 Apr	Emulating FPGA using MATLAB HDL Coder and analyzing performance.		
12	20-24 Mar	Using Audio Signals to test system performance, Plotting graphs		
13	4 – 10 Apr	Preparing documentation and PPT for TPP and PE presentation		
14	11 - 17 Apr	Final Report and IEEE format paper, Preparing for Phase – IV		
15	18 - 24 Apr	Preparing Black Book and ESE – II.		