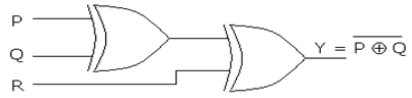
Darshan Institute of Engineering and Technology, Rajkot,
Subject: Digital Electronics (2131004)
GTU Question Bank

Unit	Group	Questions	Summer-16	Winter-15	Summer-15	Winter-14	Summer-14	Winter-13	Summer-13
1	A	Do as directed : I. Given that (16)10 = (100)x, find the value of x. II. Add $(6E)_{16}$ and $(C5)_{16}$ III. $(4433)_5$ = ( )$_{10}$ = ( )$_2$	3						
		What are the different types of the codes used in digital systems? Explain them.	4						
		Do as directed : I. $(1011011101101110)_2$ = ( )$_{16}$ II. Subtract $(45)_8$ from $(66)_8$ III. Covert the Gray code 1101 to binary IV. Find the XS-3 code of 37	4						
		Design 4 bit binary to gray code converter.	7						
		Convert decimal number (0.252)10 to binary with an error less than 1 %.		3					
		Convert $(75)_{10}$ = (_____)2			1				
		Convert $(101011)_2$ = (_____)$_{10}$			1				
		Convert $(10101101)_2$ = (_____)$_{16}$ = (_____)$_8$			2				
		What is self-complementing code? Represent $(472)_{10}$ in 2421 self-complementing code.			2				
		Convert $(96)_{10}$ to its equivalent gray code and EX-3 code.			4				
		Perform addition in BCD format $(79)_{BCD}$ + $(16)_{BCD}$			3				
		Perform subtraction of $(78)_{10}$ – $(58)_{10}$ using 2's complement method.			3				
		Convert the decimal number 187 to 8-bit binary.				1			
		Convert the binary number 1001.0010_2				1			
		What is the 2's complement of number 1101110?				1			
		Design a BCD to excess 3 code converter using minimum number of NAND gates.				7			7
		Covert following: (1) $(4E7.2)_{16}$ = (?)$_8$ (2) $(521.3)_8$ = (?)$_2$					6		
		Write a brief not on Gray codes. Also discuss methods for conversion from gray to binary code and vice versa					7		
		Convert the following numbers as directed: (1) $(130)_{10}$ = ( )$_2$ (2) $(1011011)_2$ = ( )$_{10}$ (3) $(1011101111)_2$ = ( )$_8$ (4) $(110111011101111011)_2$ =( )$_{16}$						7	
		Convert the decimal number 250.5 to base 3, base 4, base 7and base 16.							7
		Perform the subtraction with the following decimal numbers using 1's compliment and 2's compliments. (a) 11010-1101 , (b) 10010-10011							7
	B	Find the logic required at R input. 			1				
		Show that the dual of the exclusive-OR is equal to its compliment.							7
		Give following Definitions: (1) Fan in (2) Fan out (3) Noise margin (4) Propagation delay	1		4				
		Define the followings. (1)Fan in (2) Noise margin (3) Propagation delay (4) Negative logic				4			
	D	Discuss NAND gate as universal gate (implement NOT, AND, OR & NOR gate using NAND gate).			4			1	
	F	When used with an IC, what does the term "QUAD" indicate?				1			

2	A	Reduce the expression F = Σm(0,2,3,4,5,6) using K-map and implement using NAND gates only.	7							
		Using D as the MEV, reduce Y = A'B'C'D' + A'B'CD' + AB'C'D' + AB'C'D + AB'CD + AB'CD'.		4						
		Minimize following Boolean function using K-map & design the simplified function using logic gates. F = Σ m(1, 2, 4, 6, 7, 11, 15) + Σ d(0, 3)		7						
		Reduce the given function using K-map and implement the same using gates. F(A,B,C,D) = Σm (0,1,3,7,11,15) + Σd (2,4)			7					
		Minimize the following logic function using K-maps and realize using NAND and NOR gates. F(A,B,C,D) =Σ_m(1,3,5,8,9,11,15) + d(2,13).				7				
		Minimise the logic function F (A,B,C,D) = Π_ M (1, 2, 3, 8, 9, 10, 11,14) · d (7, 15) Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.				7				
		Using K-map find the Boolean function and its complement for the following: F(A,B,C,D) = Σ(1,2,3,4,6,8,9,10,11,12,14)					7			
		Simplify the Boolean Function with Karnaugh map: F(w,x,y,z) = Σ(0,1,2,4,5,6,8,9,12,13,14) and F = A´B´C´+B´CD´+A´BCD´+AB´C´						7		
		Simplify the Boolean Function: F(w,x,y,z) = Σ(1,3,7,11,15) and the Don't care conditions : d(w,x,y,z) = Σ(0,2,5)						7		
		Obtain the simplified expression in sum of product for the following Boolean functions. (a) F= Σ(0,1,4,5,10,11,12,14) and (b) F=Σ (11, 12, 13, 14, 15).								7
		Implement the functions F=Σ(1,3,7,11,15) with don't care conditions d=Σ(0, 2,5) Discuss the effect of don't care conditions.								7
	B	State and prove De'Morgan's Theorems with the help of truth tables.	4		4	1		7		
	C	Convert F (A, B, C) = BC +A into standard minterm form.			3					
		Attempt following: (1) Covert into Sum-of-Minterms : A' + B + CA (2) Covert into Product-of-Maxtems : A(A'+B)(C')					7			
		Define the following terms: (1) Literal (2) Minterm (3) Maxterm						3		
		Simplify the following Boolean functions to a minimum numbers of literals. (a) xyz+x'y+xyz' and (b)(A+B)'(A'+B')'								7
	D	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations: A is False, B is True A is False, C is True A, B, C are False A, B, C are True (i) Write the Truth table for F. Use the convention True=1 and False = 0. (ii) Write the simplified expression for F in SOP form. (iii) Write the simplified expression for F in POS form.				7				
	E	Reduce the expression F = ((AB)'+A'+AB)'	3							
		Show that A XNOR B = AB + A'B' = (A XOR B)' = (AB'+A'B)'. Also construct the corresponding logic diagrams.	7							
		Minimize the following Boolean expressions. 1. X = ((A'B'C')' + (A'B)')' 2. Y = AB + ABC' + A'BC + A'BC'		4						
		Simplify using Boolean laws and draw the logic diagram for the given expression. $F = \overline{ABC} + \overline{AB}\,C + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + A\,\overline{B}\,C$				7				
		Prove the following Boolean identities. (i) $XY + YZ + \overline{Y}\,Z = XY + Z$ (ii) $A.B + \overline{A}.B + \overline{A}.\overline{B} = \overline{A} + B$				7				
		Simplify : (1) A'B + A'BC' + A'BCD + A'BC'D'E (2) (P+Q+R) (P' + Q' + R') P					8			
		Prove that: (1) ((AB'+ABC)' + A(B+AB'))' = 0 (2) AB'C + A'BC + ABC = AC + AB					7			
	F	Derive Boolean function using Tabulation Method for the following: F(P,Q,R,S) = Σ(0,1,3,4,5,7,10,13,14,15)					7			
		Simplify the Boolean Function by using the tabulation method: F = Σ(0,1,2,8,10,11,14,15)						7		
	G	Reduce following Boolean function and then realize the reduced one using NOR gate only. X = A (B'+C') (A+D)		4						
		(1) Draw the logic circuit for following function using only NAND gates: F= ABC+A´B+AC´D´ (2) Draw the logic circuit for following function using only NOR gates: F= ABC´+AB(C+D)						7		
		Implement the Boolean functions. (a) xyz+x'y+xyz' (b) (A+B)'(A'+B')' and (c) F= xy+xy'+y'z with logic gates.								7
	H	Obtain the truth table of the function F= xy+xy'+y'z.								7
	I	Define Negative logic	1							
	J	Write short note on half adder and full adder.	7							

3	A	What is encoder? With logic circuit and truth table explain the working of Octal to binary Encoder.						7	
	B	Give the applications of Decoder.	3						
		Design a full adder using 3X8 decoder followed by gates.		7					
		Design 4 X 16 decoder using two 3 X 8 decoder.	4		7				
		Design a 4-to-16 decoder by using only 2-4 decoder circuits					7		
		With logic circuit and truth table explain the working of 3 to 8 line decoder.						7	
	C	Implement the given function using multiplexer F(A,B,C) = Σm(1,2,4,7)	4						
		Explain the working of multiplexer.	3						
		Implement following logic function using 8X1 MUX. F = Σ m(0, 1, 3, 5, 7, 11, 13, 14, 15)		7					
		Implement the given function using 8 X 1 Multiplexer F (A,B,C,D) = Σm (0,1,2,3,5,8,9,11,14)			7				
		Design a 8 to 1 multiplexer by using the four variable function given by F(A,B,C,D) =Σm(0,1,3,4,8,9,15).				7			
		What is Multiplexer? With logic circuit and function table explain the working of 4 to 1 line multiplexer.						7	7
	D	With logic circuit describe the function of: (1) Full adder (2) Full subtractor. Also write the simplified Boolean functions for their outputs.		14				7	
		Explain half and full adders in detail.							7
	E	Draw & explain in brief pin diagram of 7485 four-bit magnitude comparator.		3					
		Design a circuit for 2-bit magnitude comparator.			7				
		With logic circuit explain the working of 4-bit magnitude comparator.						7	
	F	Write a brief note on parity checker/generator.			7		7		
4	A	Draw & explain in brief a high assertion input SR latch.		3					
		For the figures 1, 2, & 3, plot the output waveforms referenced to the clock signal assuming the initial contents of all FFs is Q = 0. Assume all FFs are edge triggered.		7					

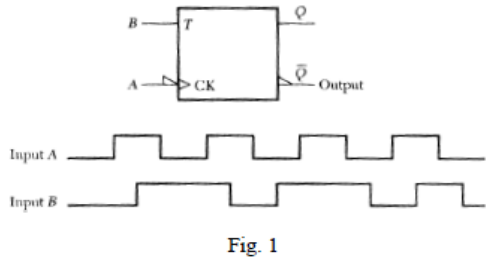


Fig. 1

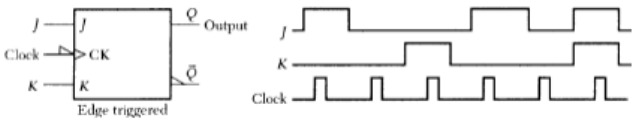


Fig. 2

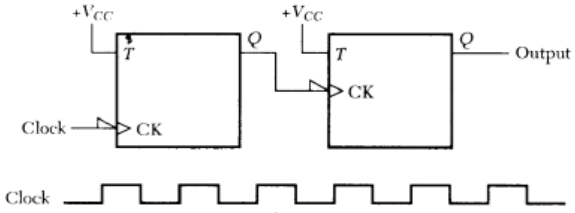
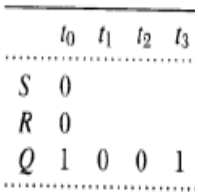
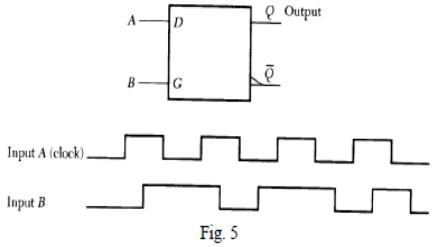
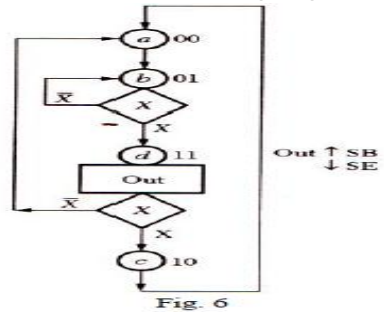
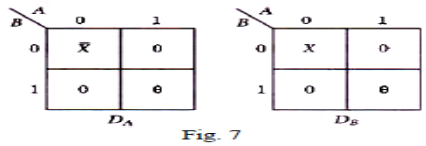


Fig. 3

4	A	(1) Fill in values for S & R to cause the Q values of the SR FF given in figure 4. (2) 2. Plot the output waveform for the inputs shown in figure 5, assuming the initial contents of the FF is Q = 0.  Fig. 4  Fig. 5		4					
		With the help of function table and circuit diagram explain the working of clocked SR flip flop.			7				
		Draw the circuit diagrams and Truth table of all the Flip flops (SR, D, T and JK).				7			
		Write a brief note on edge-triggered SR and JK Flip-Flops.					7		
		Write a note on Master-Slave Flip-Flop.					7		
		(1) Define: combinational logic circuit and sequential logic circuit. (2) With logic diagram explain the function of master-slave flip-flop.						7	
		Explain D type positive edge triggered flip flop.							7
		Define the following terms: (1) Flip flop (2) Counter (3) Register						3	
	B	Implement T flip flop using D flip flop.	3						
		Convert D flip flop into SR flip flop			7				
		Implement D flip flop using JK flip flop.				7			
	C	With neat sketch design 4-bit bidirectional shift register.			7				
		Write short note on four bit Universal Shift Register.				7			
		Design a circuit for 4-bits parallel register with load with D Flip-Flops. Load input decides whether to load new input or to apply no change conditions.					7		
	D	Design a synchronous BCD counter with JK flip-flops.	7						
		Draw a frequency divider using JK FFs to divide input clock frequency by a factor of 8.		3					
		Design a 3-bit synchronous up counter using K-maps and positive edge-triggered JK FFs.		7					
		Design 4-bit ripple counter using negative edge triggered JK flip flop.			7				
		Design a mod-12 Synchronous up counter using D-flipflop.				7			
		Design a sequential circuit using JK Flip-Flops and two states Q0 and Q1 such that , (1) It moves to the next state for input 0. (00 to 01, 01 to 10,..., 11 to 00) (2) It moves to the previous state for input 1. (reverse from the above mentioned steps)					9		
		Design and Implement a Mod-10 asynchronous counter with T FF.					7		
		Write a note on Binary Ripple Counter.					7		
		With logic diagram explain the operation of 4 bit binary ripple counter. How up counter can be converted into down counter?						7	
		Design a synchronous BCD counter with JK flip flops.							7
	E	Design a sequential with JK flip-flops to satisfy the following state equations: A(t+1) =A´B´CD+A´B´C+ACD+AC´D´ B(t+1) = A´C +CD´+A´BC´ C(t+1) = B D(t+1) = D´						7	
	F	Distinguish between combinational and sequential logic circuits. Give the applications of flip-flops.	7						
	G	Give the comparison between synchronous and asynchronous counters.	4						
5	A	Give following definitions: (1)State table (2) Melay machine (3) Moore machine			3				
		Discuss the General State machine Architecture.		3		7			
	C	Explain the types of finite state machines?	4						

6	A	Construct next state table for the state diagram given in figure 6.  Fig. 6		4					
	B	What do you mean by an output glitch problem? Explain any one method to eliminate the glitch from an OFL circuit. Draw suitable waveforms and logic diagrams.		7					
	C	With the help of next state D input maps given in figure 7, construct IFL using MUXs of suitable size and number.  Fig. 7		3					
7	A	Explain the Fundamental Mode Model of Asynchronous State Machine with suitable example.				7			
	B	Explain critical race problem of an asynchronous state machines with the help of one example.		4					
	C	Explain oscillation problem of an asynchronous state machines with the help of one example.		4					
8	A	Which TTL logic gate is used for wired ANDing?				1			
		Compare the Following in every aspect: TTL and CMOS				3			
	B	Give definition of Totem pole output.				1			
	C	Explain two input CMOS NAND gate.	7						
9	A	Write a note on Memory.	7						
		Compare ROM, PLA and PAL.			7				
		Compare the Following in every aspect: RAM and ROM				4			
	B	Define PROM	1						
	C	Give definition of EPROM.				1			
	D	Write short note on Programmable Logic Arrays.				7	7		7
	E	Implement following functions using ROM. F1 = Σ m(1, 3, 4, 6) F2 = Σ m(2, 4, 5, 7) F3 = Σ m(0, 1, 5, 7) F4 = Σ m(1, 2, 3, 4)		7					
	F	Write a short note on FPGA.	3	3					