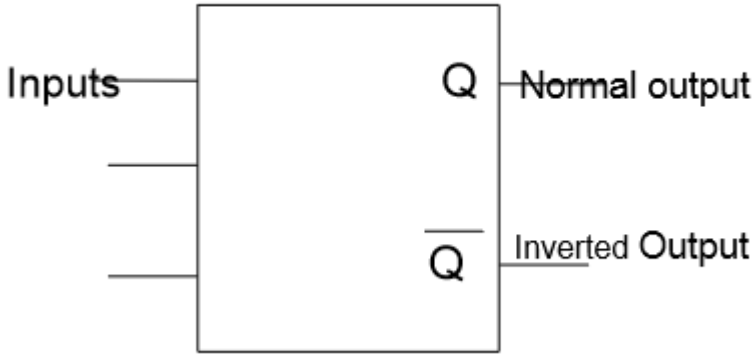
Design Engineering

FLIP-FLOPS

Flip Flop (Sequential Circuits)

- What is Flip flop?
- Answer: In digital circuits, the flip-flop, is a kind of bi-stable multivibrator.
- It is a Sequential Circuits / an electronic circuit which has two stable states and thereby is capable of serving as one bit of memory , bit 1 or bit 0.

Introduction – Flip Flop



They have two stable conditions and can be switched from one to the other by appropriate inputs. These stable conditions are usually called the states states states states of the circuit.

- They are 1 (HIGH) or 0 (LOW).
- Whenever we refer to the state of flip flop, we refer to the state of its normal output (Q).
- More complicated Flip flop complicated Flip flop complicated Flip flop complicated Flip flop use a clock as the control input. These clocked flip-flops are used whenever the input and output signals must occur within a particular sequence.

Introduction: Types Of Flip Flop

1. SR Flip Flop SR Flip Flop SR Flip Flop SR Flip Flop
    a. SR Flip Flop Active Low = NAND gates
    b. SR Flip Flop Active High = NOR gates
2. Clocked SR Flip Flop
3. JK Flip Flop
4. JK Flip Flop With Pre-set And Clear
5. T Flip Flop
6. D Flip Flop
7. Master-Slave Edge-Triggered Flip-Flop

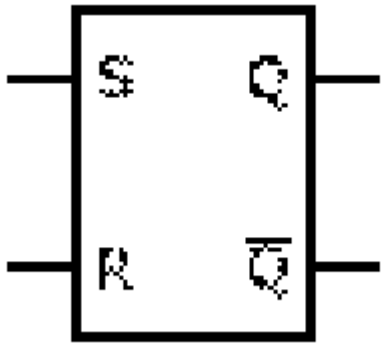
The Used of Flip Flop

- For Memory circuits
- For Logic Control Devices
- For Counter Devices
- For Register Devices

SR Flip Flop

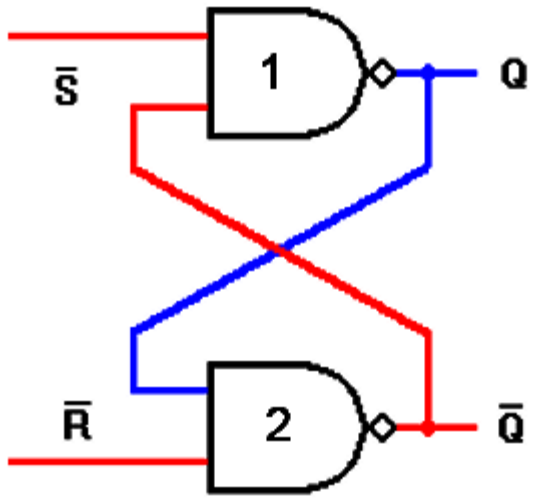
- The most basic Flip Flop is called SR Flip Flop SR Flip Flop SR Flip Flop SR Flip Flop.
- The basic RS flip flop is an asynchronous device.
- In asynchronous device, the outputs is immediately changed anytime one or more of the inputs change just as in combinational logic circuits.
- It does not operate in step with a clock or timing.
- These basic Flip Flop circuit can be constructed using two NAND gates latch or two NOR gates latch.
- SR Flip Flop Active Low SR Flip Flop Active Low SR Flip Flop Active Low SR Flip Flop Active Low = NAND gates
- SR Flip Flop Active High SR Flip Flop Active High SR Flip Flop Active High SR Flip Flop Active High = NOR gates

SR Flip Flop



- The SR Flip Flop has two inputs, SET (S) and RESET (R).
- The SR Flip Flop has two outputs, Q and $\overline{\ }$
- The Q output is considered the normal output and is the one most used.
- The other output $\overline{\ }$ is simply the compliment of output Q.

SR Flip Flop - NAND GATE LATCH



- The NAND gate version has two inputs, SET (S) and RESET (R).
- Two outputs, Q as normal output and $\bar{Q}$ as inverted output and feedback mechanism.
- The feedback mechanism is required to form a sequential circuit by connecting the output of NAND-1 to the input of NAND-2 and vice versa.
- The circuit outputs depends on the inputs and also on the outputs.

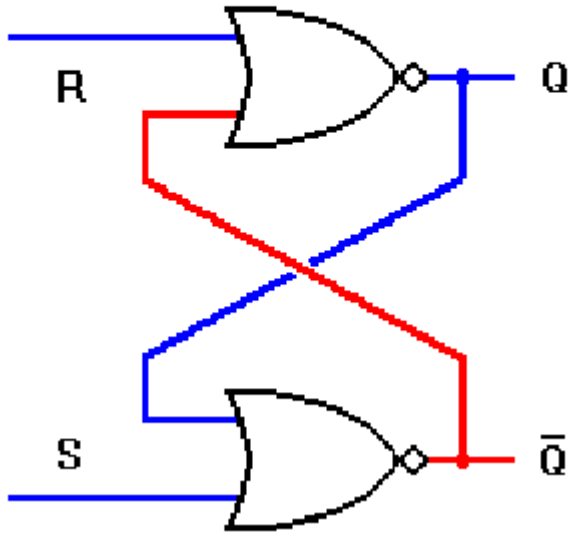
SR Flip Flop - NAND GATE LATCH

- From the description of the NAND gate latch operation, it shows that the SET and RESET inputs are active LOW.
- The SET input will set Q = 1 when SET is 0 (LOW).RESET input will reset Q = 0 when RESET is 0 (LOW)
- In the prohibited/INVALID state both outputs are 1. This condition is not used on the RS flip-flop. The set condition means setting the output Q to 1.
- Likewise, the reset condition means resetting (clearing) the output Q to 0. The last row shows the disabled, or hold , condition of the RS flip-flop. The outputs remain as they were before the hold condition existed. There is no change in the outputs from the previous states

S	R	Q	$\bar{Q}$	STATUS
0	0	1	1	INVALID
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q	$\bar{Q}$	HOLD (NoChange)

SR Flip Flop - NOR GATE LATCH NOR GATE LATCH NOR GATE LATCH NOR GATE LATCH

- **NOR GATE LATCH**



- The latch circuit can also be constructed using two NOR gates latch.
- The construction is similar to the NAND latch except that the normal output Q and inverted output $\bar{}$ have reversed positions.

SR Flip Flop - NOR GATE LATCH

- S = 1, R = 0; This will set Q to 1, it works in SET mode operation.
- S = 1, R = 1; This condition tries to set and reset the NOR gate latch at the same time, and it produces Q = $\overline{\ }$ = 0 This is an unexpected condition and are not used.
- Since the two outputs should be inverse of each other. If the inputs are returned to 1 simultaneously, the output states are unpredictable.
- This input condition should not be used and when circuits are constructed, the design should make this condition SET=RESET = 1 never arises

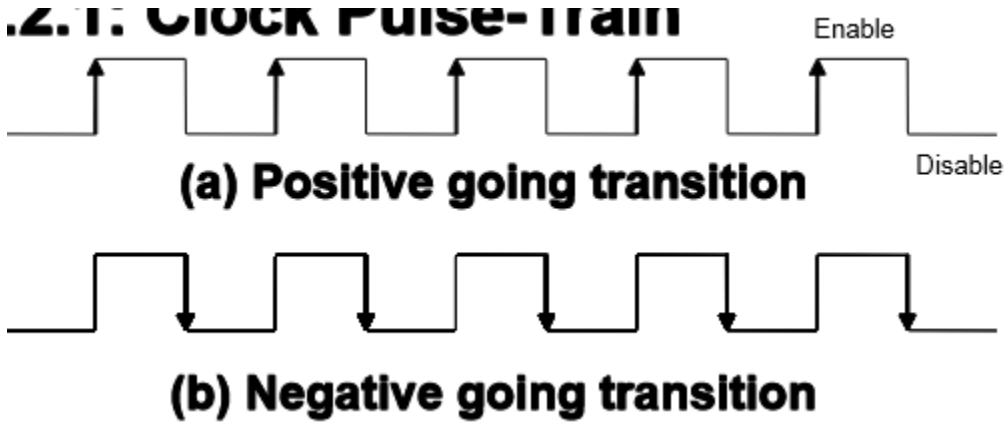
SR Flip Flop - NOR GATE LATCH

S	R	Q	$\bar{Q}$	STATUS
0	0	Q	$\bar{Q}$	HOLD (NoChange)
0	1	0	1	RESET
1	0	1	0	SET
1	1	0	0	INVALID

- From the description of the NOR gate latch operation, it shows that the SET and RESET inputs are Active HIGH.
- The SET input will set Q = 1 when SET is 1 (HIGH). RESET input will reset Q when RESET is 1 (HIGH).

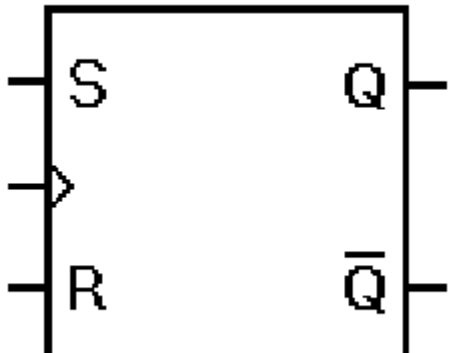
The CLOCK

- When the clock changes from a LOW state to a HIGH state, this is called the positive-going transition (PGT) or positive edge triggered.
- When the clock changes from a HIGH state to a LOW state, it is called negative going transition (NGT) or negative edge triggered.



Clocked SR Flip Flop

- Additional clock input is added to change the SR flip- flop from an element used in asynchronous sequential circuits to one, which can be used in synchronous circuits.
- The clocked SR flip flop logic symbol that is triggered by the PGT is shown in Figure.
- Its means that the flip flop can change the output states only when clock signal makes a transition from LOW to HIGH.

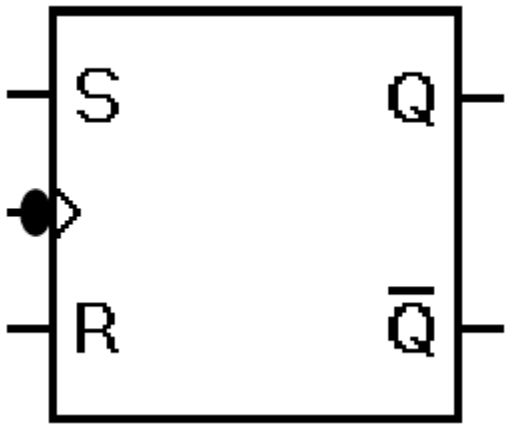


Clocked RS Flip Flop

clock	S	R	Q	$\overline{Q}$	STATUS
↑	0	0	Q	$\overline{Q}$	**HOLD** (NoChange)
↑	0	1	0	1	**RESET**
↑	1	0	1	0	**SET**
↑	1	1	0	0	**INVALID**

- The Truth Table in figure shows how the flip flop output will respond to the PGT at the clocked input for the various combinations of SR inputs and output.
- The up arrow symbol indicates PGT.

Clocked SR Flip Flop

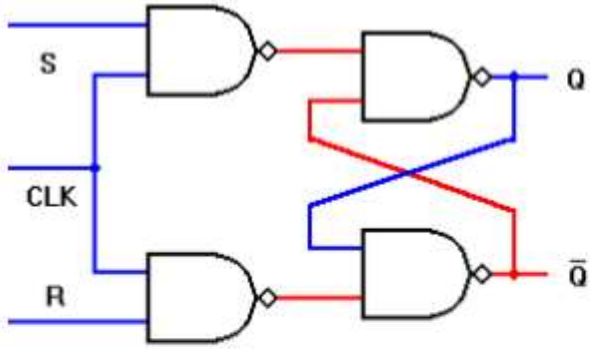


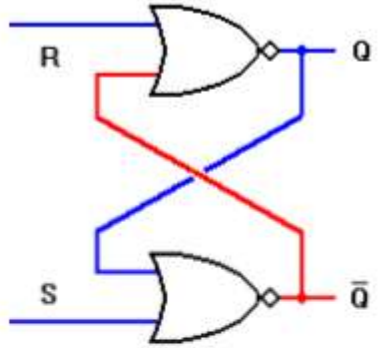
- The clocked SR Flip Flop logic symbol that is triggered by the NGT is shown in Figure.
- It means that the Flip flop can change the output states only when clocked signal makes a transition from HIGH to LOW

Clocked SR Flip Flop

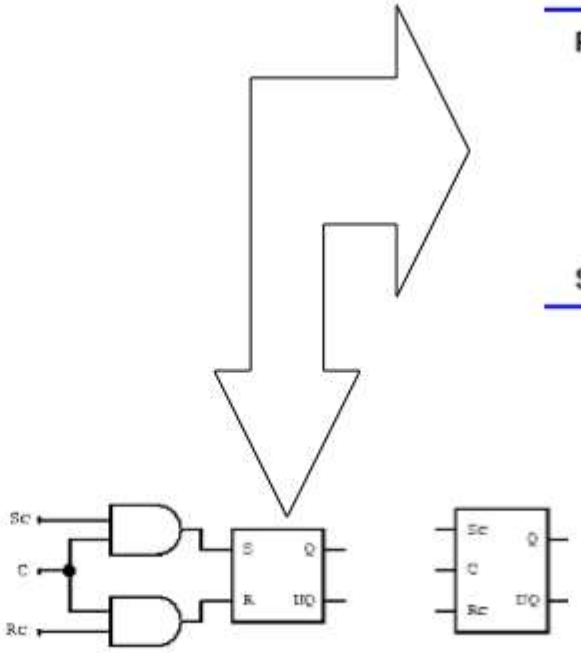
- CLOCKED SR FLIP FLOP LOGIC CIRCUIT

If used NOR Gate NOR Gate NOR Gate NOR Gate, must used AND Gate in front





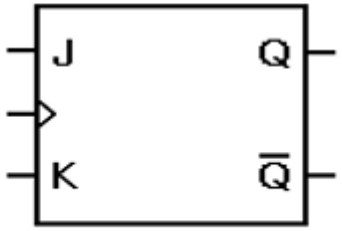
S_C	R_C	C	Q	$\bar{Q}$
x	x	0	no change	
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	undefined	
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	undefined	



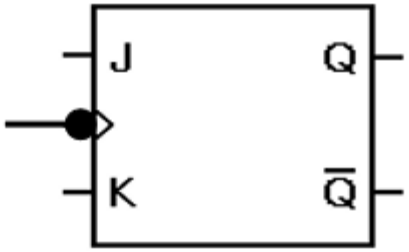
JK Flip Flop - Symbol

- Another types of Flip flop is JK flip flop.
- It differs from the RS flip flops when J=K=1 condition is not indeterminate but it is defined to give a very useful changeover (toggle) action.
- Toggle means that Q and $\overline{Q}$ will switch to their opposite states.
- The JK Flip flop has clock input Cp and two control inputs J and K.
- Operation of Jk Flip Flop is completely described by truth table in Figure.

- Figure 4.3.1 : **PGT JK Flip flop symbol**



- Figure 4.3.2 : **NGT JK Flip flop symbol**

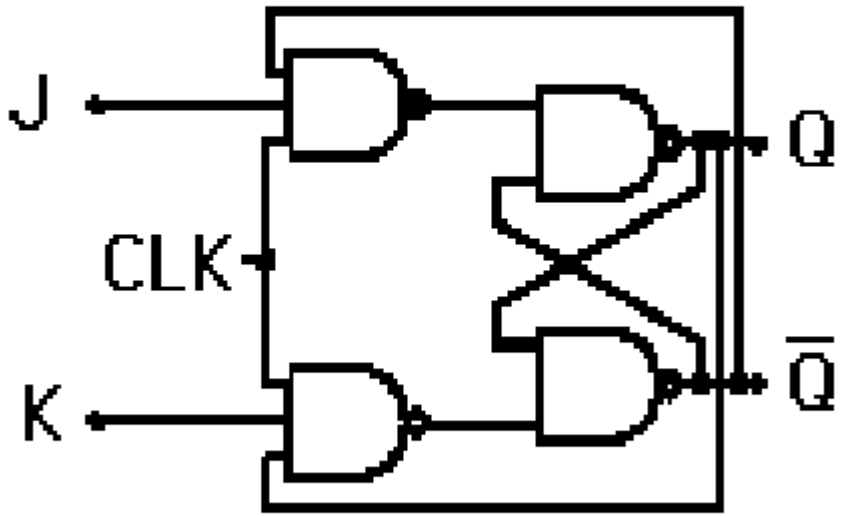


JK Flip Flop – Truth Table And Logic Circuit

Figure 4.3.3: **Truth Table for JK Flip Flop**

clock	J	K	Q	$\bar{Q}$	STATUS
↑	0	0	Q	$\bar{Q}$	HOLD (No Change)
↑	0	1	1	0	RESET
↑	1	0	0	1	SET
↑	1	1	$\bar{Q}$	Q	Toggle

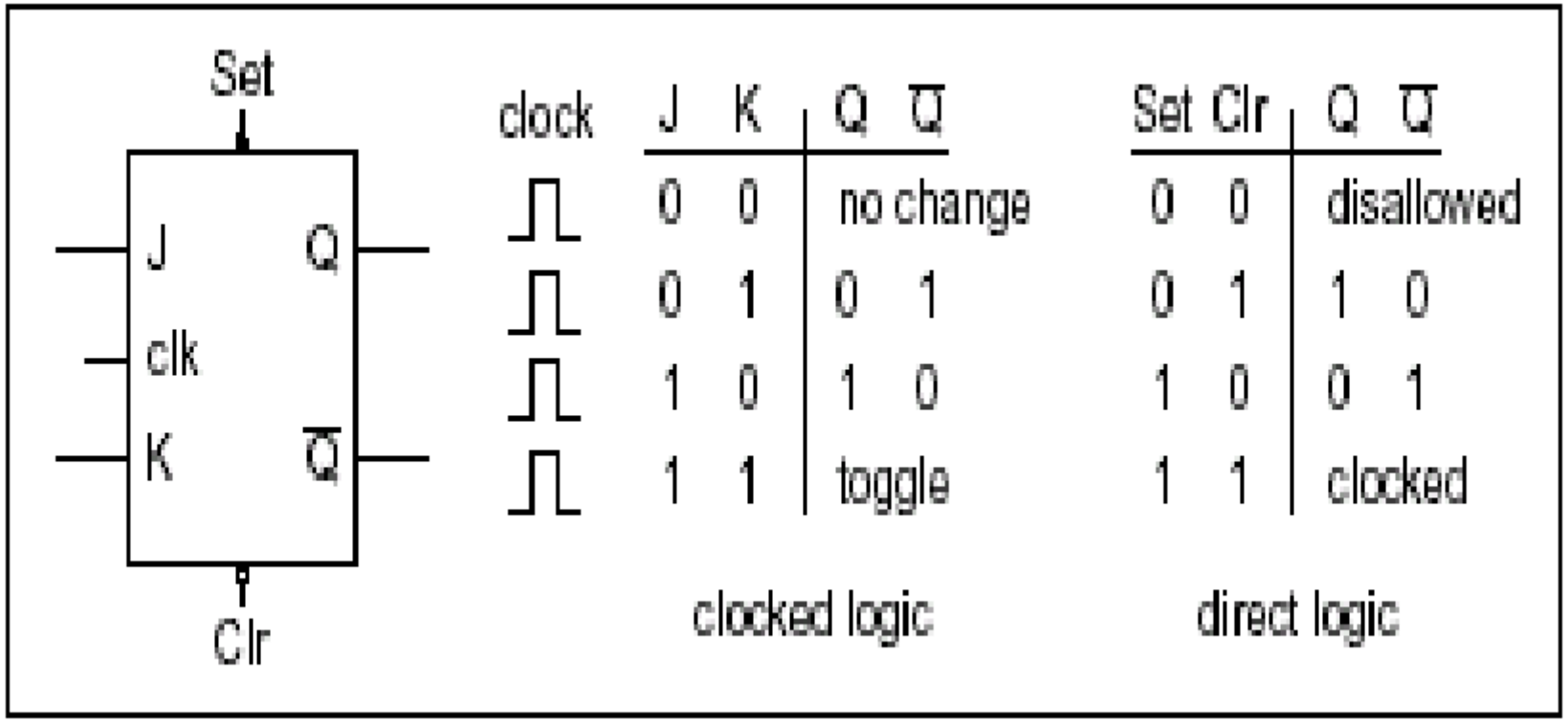
- Figure 4.3.4: **JK FLIP FLOP LOGIC CIRCUIT**



JK Flip Flop with Asynchronous Input

- The J and K inputs are called synchronous inputs since they only influence the state of the flip flop when the clocked pulse is present.
- This flip flop can also have other inputs called Pre-set (or SET) and clear that can be used for setting the flip flop to 1 or resetting it to 0 by applying the appropriate signal to the Pre-set and Clear inputs.
- These inputs can change the state of the flip flop regardless of synchronous inputs or the clock

JK Flip Flop with Preset and Clear



clock	J	K	Q	$\overline{Q}$
⎍	0	0	no change	
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	toggle	

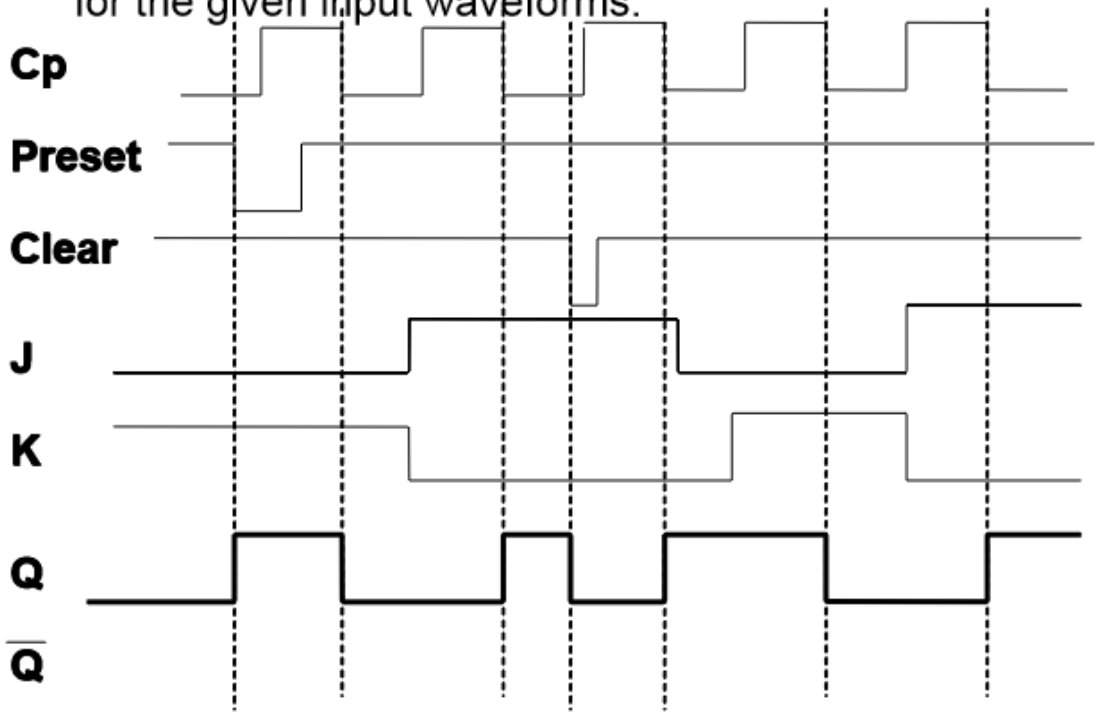
clocked logic

Set	Clr	Q	$\overline{Q}$
0	0	disallowed	
0	1	1	0
1	0	0	1
1	1	clocked	

direct logic

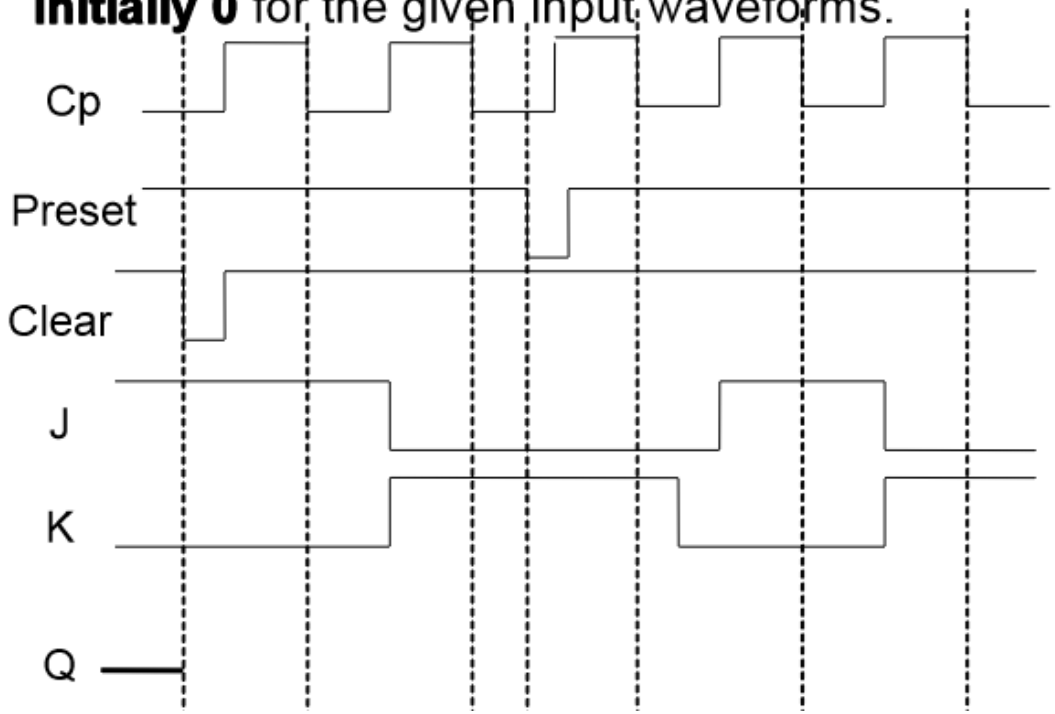
JK Flip Flop with Asynchronous Input

- **Example 4.4.2** : The output of clocked JK flip flop which output **initially 0** for the given input waveforms.



JK Flip Flop with Asynchronous Input

- **Exercise 4.4.3** : The output of clocked JK flip flop which output **initially 0** for the given input waveforms.



T Flip Flop - Symbol

- The T flip flop has only the Toggle and Hold Operation.
- If Toggle mode operation. The output will toggle from 1 to 0 or vice versa.

- **Figure 4.5.1:** Symbol for T Flip Flop

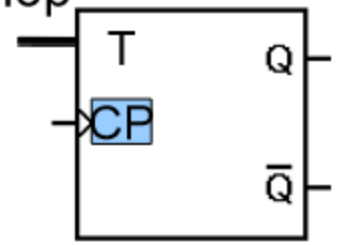


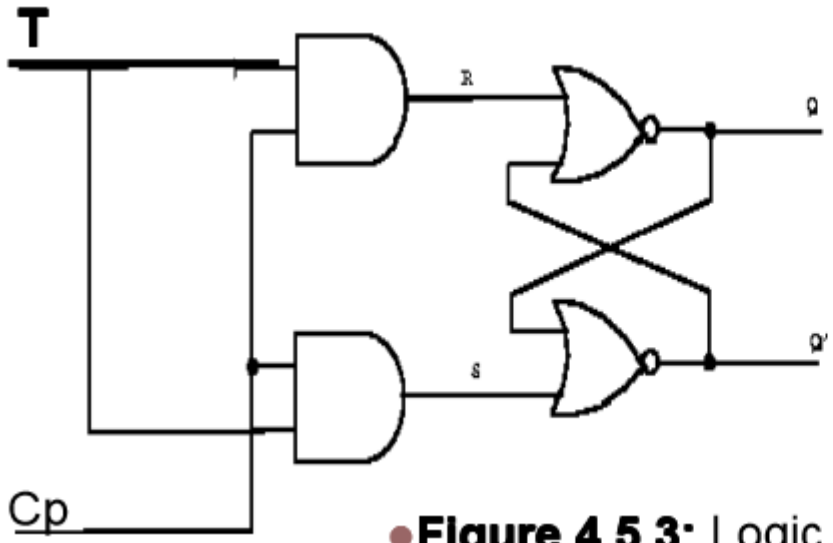
Figure 4.5.2 :Truth Table for T Flip Flop

T	clock	Q	$\bar{Q}$	status
0	↑	Q	$\bar{Q}$	HOLD
1	↑	$\bar{Q}$	Q	TOGOL

T Flip Flop – Logic Circuit

- Logic circuit T Flip flop using NOR gate

T Flip flop using NAND gate



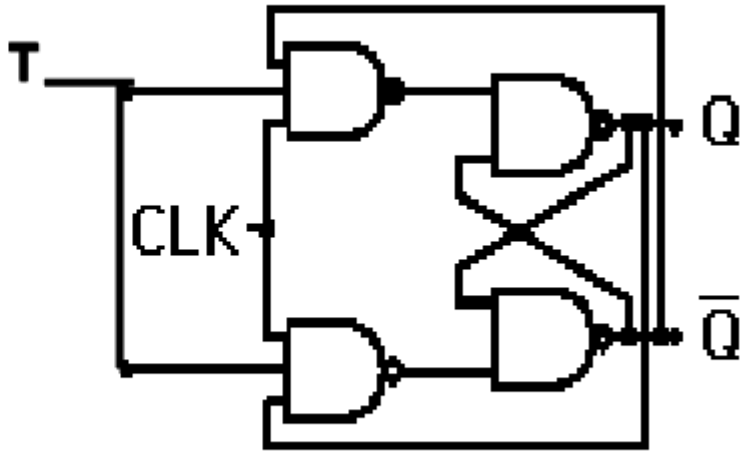
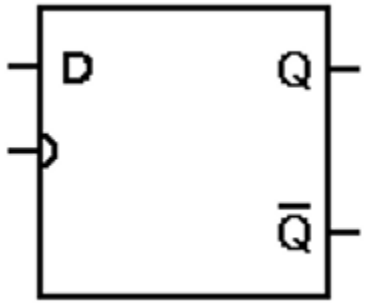


Figure 4.5.3: Logic circuit for T Flip Flop

D Flip Flop

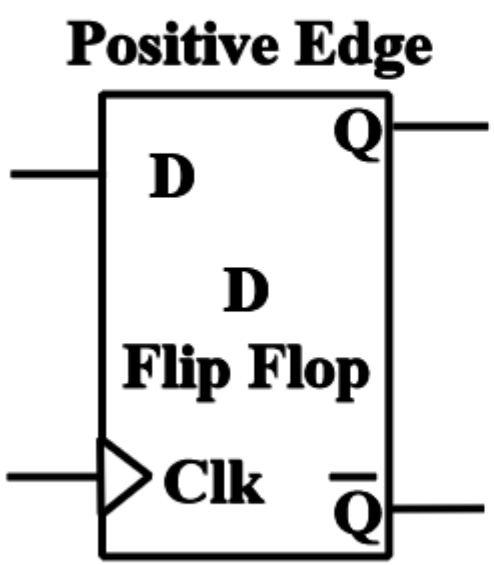
- Also Known as Data Flip flop
- Can be constructed from RS Flip Flop or JK Flip flop by addition of an inverter.
- Inverter is connected so that the R input is always the inverse of S (or J input is always complementary of K).
- The D flip flop will act as a storage element for a single binary digit (Bit).

- **Figure 4.6.1 :**
- **D Flip flop symbol**



D Flip Flop - Symbol

- PGT



- NGT

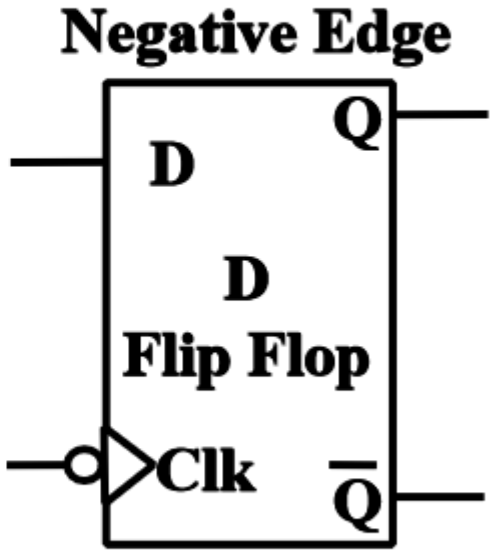
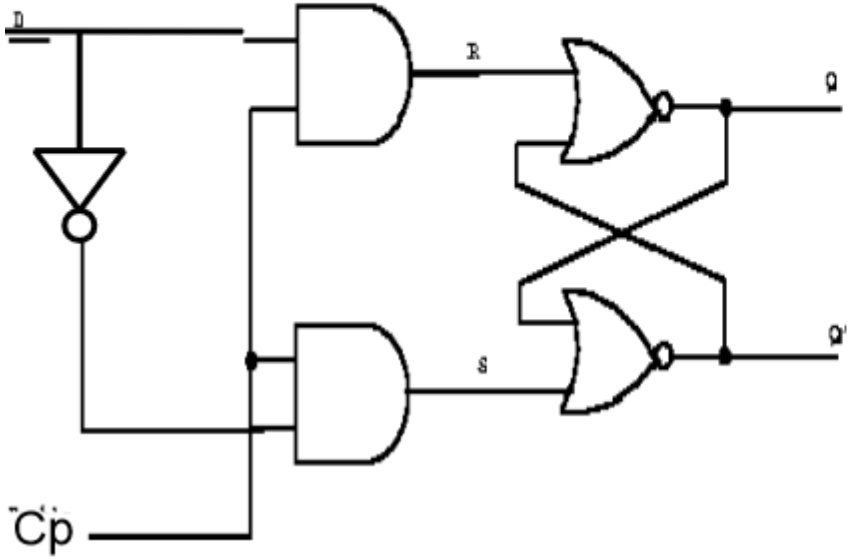


Figure 4.6.2 : D Flip flop symbol using JK Flip Flop / SR Flip Flop

D Flip Flop- Logic circuit-Truth Table

- **Figure 4.6.3:** Logic circuit for D Flip Flop



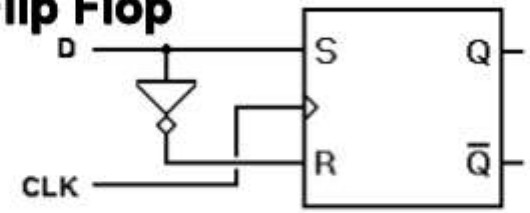
- **Figure 4.6.4:** Truth Table for D Flip Flop

D	clock	Q	$\overline{Q}$	status
0	↑	0	1	RESET
1	↑	1	0	SET

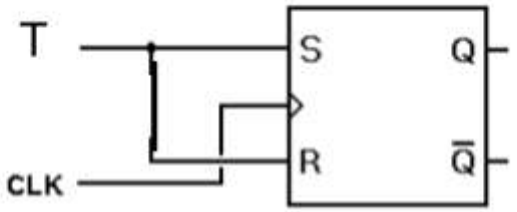
T Flip Flops and D Flip Flops can be Built using JK Flip Flop

- The JK flip flop is considered as a universal flip flop.
- A combination of JK flip flop and an inverter can construct a D Flip Flop as shown in Figure.
- It also can construct T Flip Flop by combine both J and K inputs with HIGH level input as shown in Figure.

- Figure 4.7.1 : **D Flip flop symbol using JK Flip Flop / SR Flip Flop**

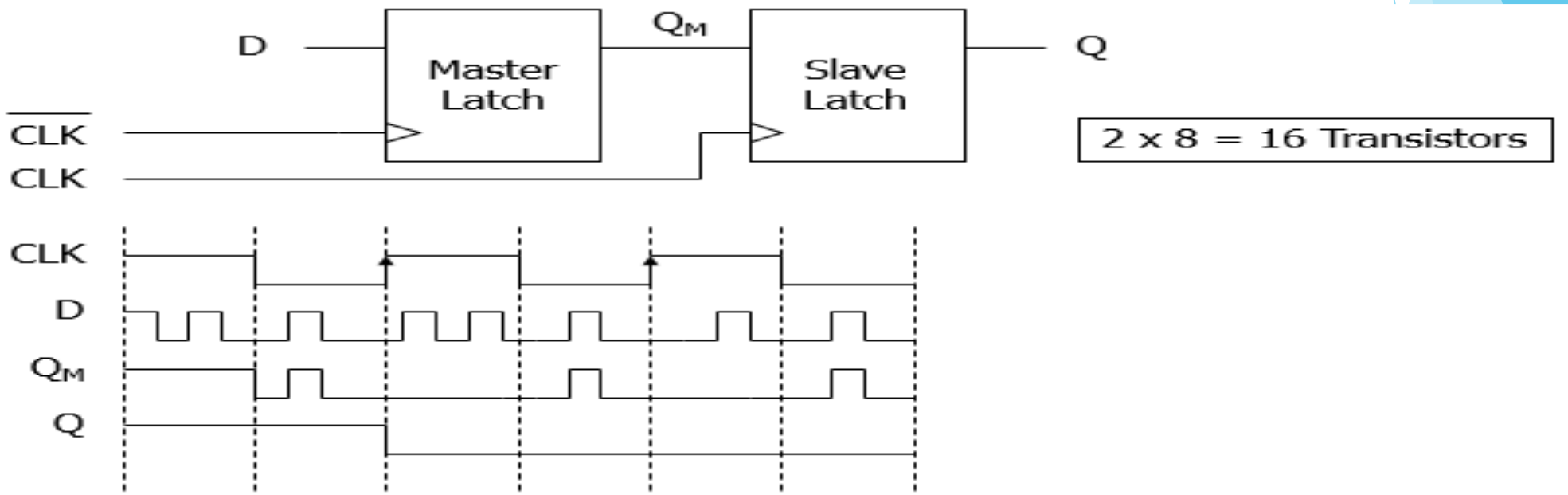


- Figure 4.7.2 : **T Flip flop symbol using JK Flip Flop / SR Flip Flop**

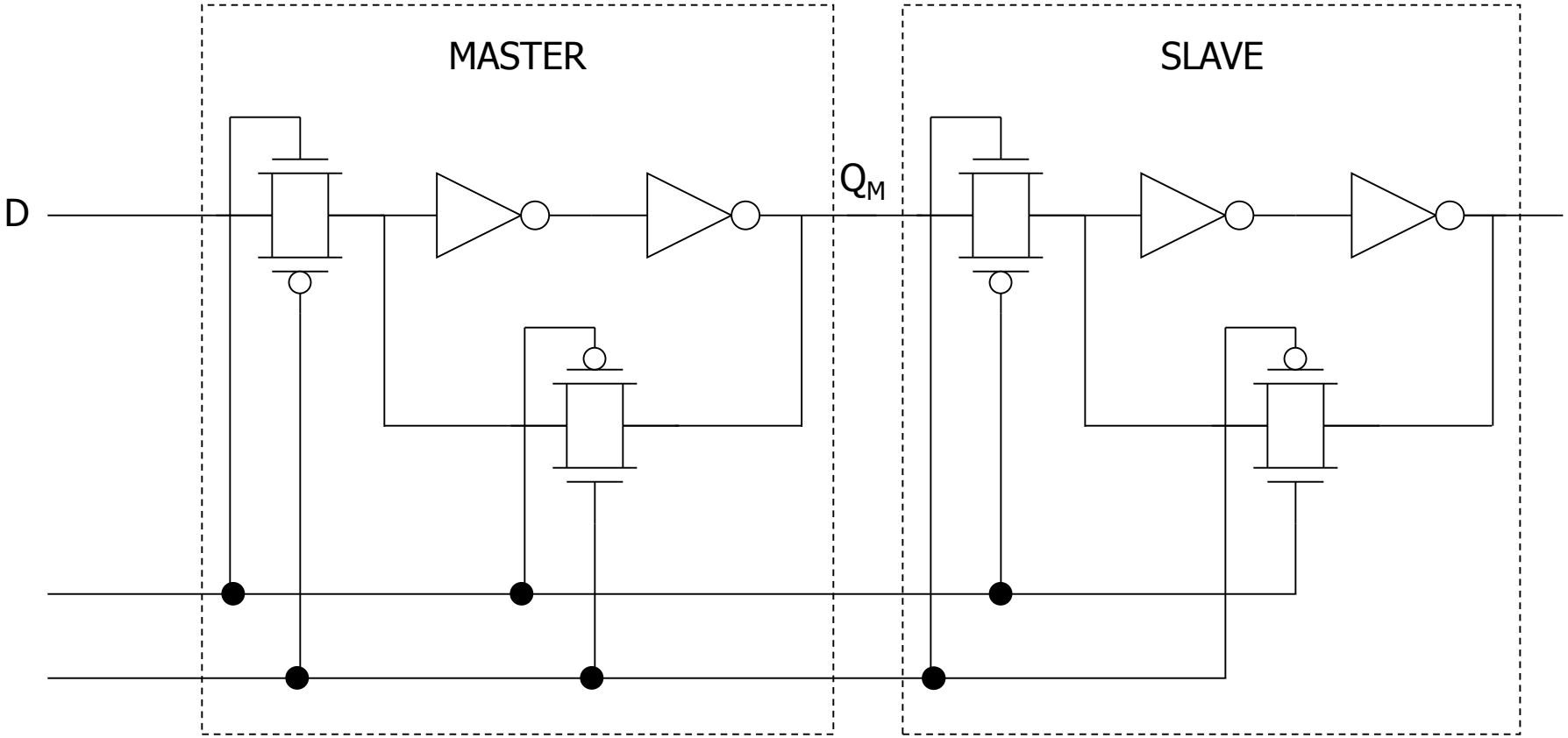


Master-Slave Edge-Triggered Flip-Flop

- Can connect two level-sensitive latches in Master-Slave configuration to form edge-triggered flip-flop.
- Master latch “catches” value of “D” at “Q_M” when CLK is low.
- Slave latch causes “Q” to change only at rising edge of CLK.

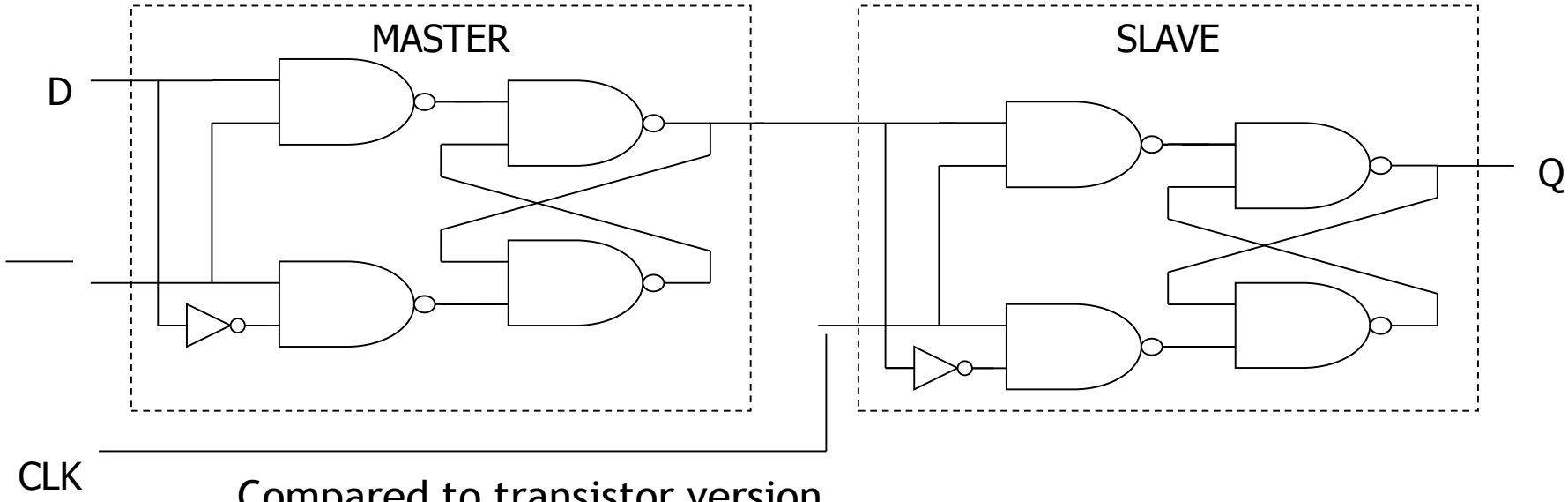


Master-Slave Edge-Triggered Flip-Flop

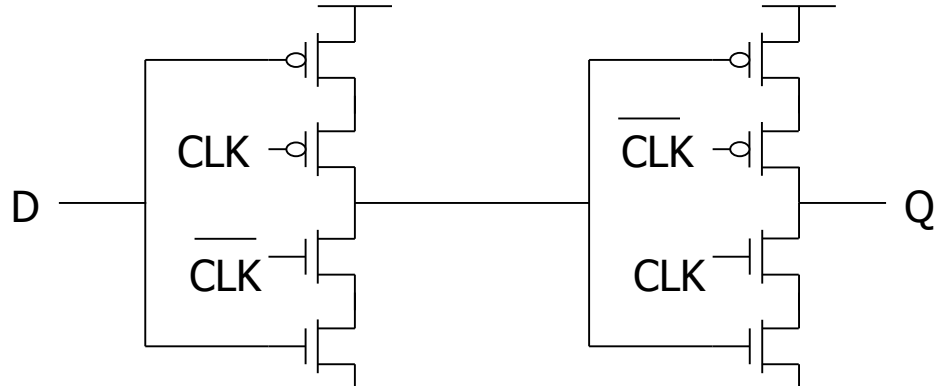


Master-Slave Edge-Triggered Flip-Flop

Master-Slave configuration



Compared to transistor version



36 Transistors

8 Transistors