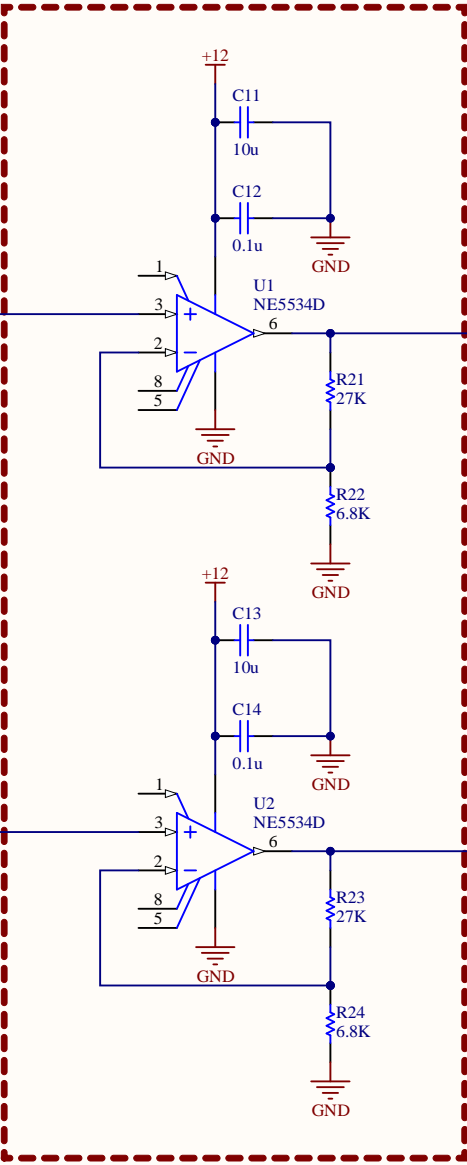


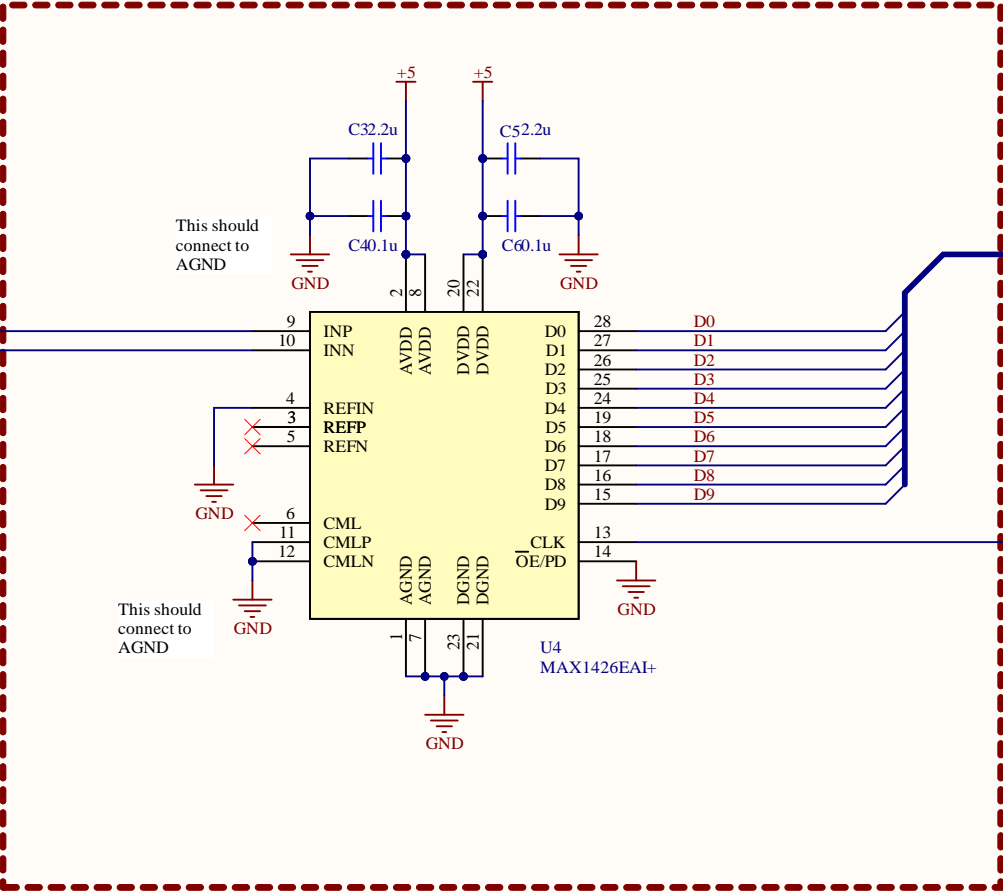
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Amplification



These non inverting amplifiers have a again of approximately 5x.
The output signals VP and VN will be 8.25 +/- 1 V.

ADC



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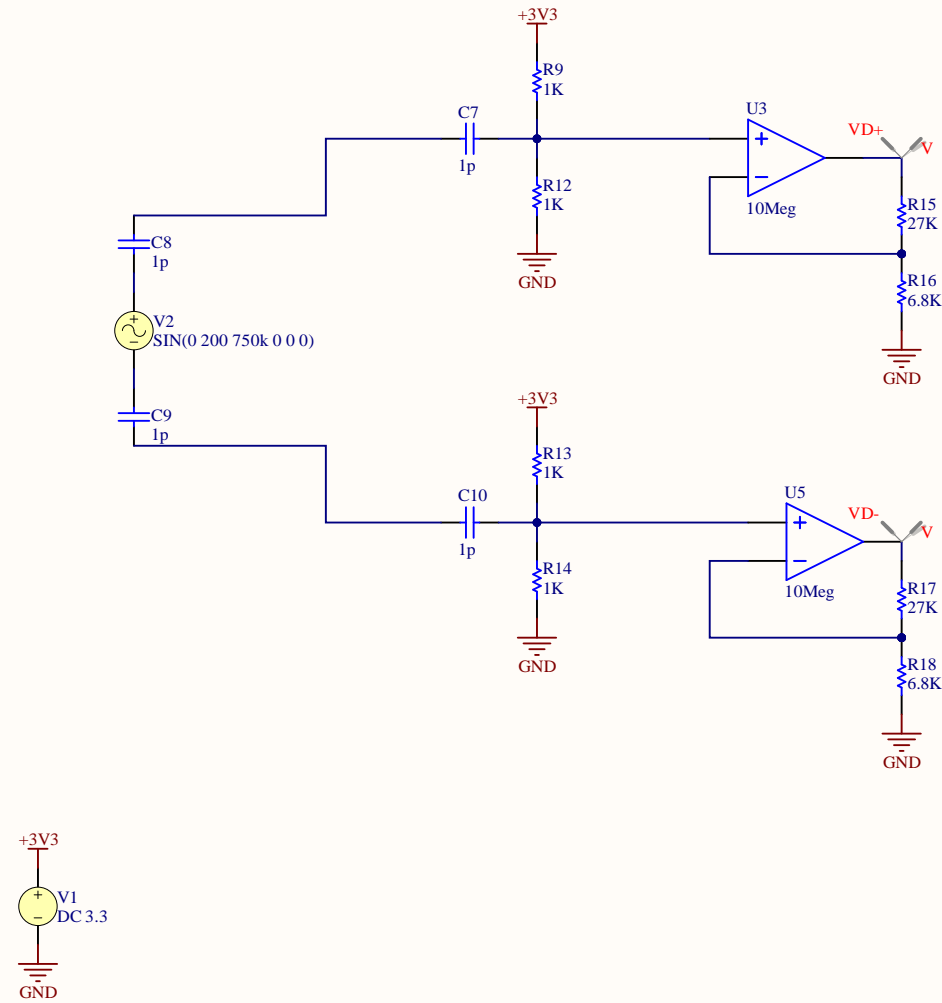
The diagram illustrates a 4-bit ripple-carry adder circuit. It consists of two main stages, each using an NE5534D op-amp configured as a comparator. The first stage (top) takes two 4-bit inputs (A and B) and produces a 4-bit sum (S) and a carry-out (Cout). The second stage (bottom) takes the 4-bit sum (S) and the carry-in (Cin) and produces the final 4-bit sum (S) and a carry-out (Cout). The circuit uses two 12V power supplies and various passive components (resistors and capacitors) for timing and signal conditioning.

Components and Connections:

- Op-Amps:** U6 and U9 are NE5534D op-amp comparators.
- Power Supplies:** Two +12V supplies are shown. The top supply is connected to the non-inverting input of U6 and the inverting input of U9. The bottom supply is connected to the non-inverting input of U9 and the inverting input of U6.
- Resistors:** R25, R26, R28, R29, R30, R31, R32 are 220Ω resistors.
- Capacitors:** C15, C17, C20, C21, C22, C23 are 10μF capacitors. C16, C18, C19 are 0.1μF capacitors.
- Logic Levels:** The circuit uses logic levels 1, 2, 3, 5, 8, and GND.

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Simulation



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