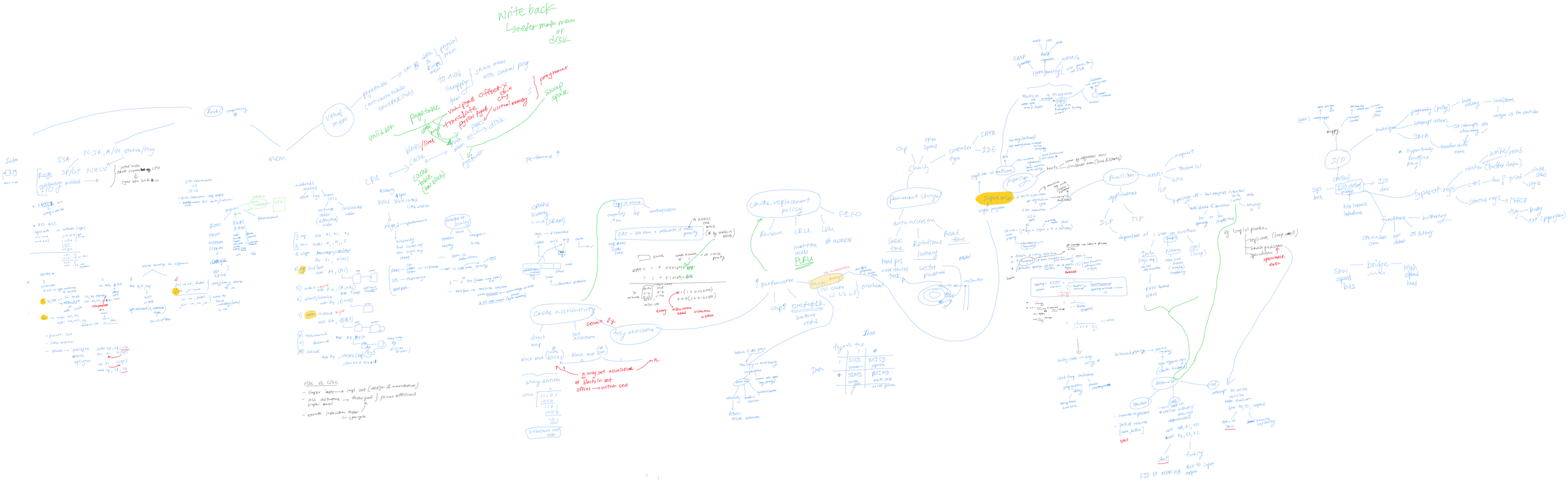
Intro
ISA
PC, IR, A/M status/flag
Regs SP/GP N Z C V
addressing modes
I/O
MEM
Ask! complexity
Virtual mem
pagetable → VM 32 data & instr mem
page table
to avoid
sharing mem with several prg
swapping
programmer
swap space
write back
refer main mem or disk
page table
valid bit
virtual page# offset
translate
physical page# virtual memory
page
disk
blocks/lines
cache
CPU
cache hierarchy (new blocks)
performance ↑
Von Neumann
Harvard
ROM
PROM
EPROM
EEPROM
RAM
SRAM
DRAM
memory
CPU
Permanent
addressing modes
calculated addr (effective)
cache hierarchy
L1 L2 L3
principle of locality
speed
capacity
cost
cache replacement policy
FIFO
Random
LRU
LFU
access
PLRU
performance
cache
L1 L2 L3
overhead
compulsory
capacity
conflict
prefetch
before read
cache associativity
direct map
set associative
fully associative
search ify
block mod #blocks
place mod (#set)
binary division
ways set associative
blocks in set
offset → within set
FL
Dist
Data
Cost
Permanent storage
data access time
seek time
rotational latency
read time
sector placement
read
actuator
cylinder
head
controller type
IDE
SATA
rpm speed
capacity
SMP
AMP
Heterogeneity (use specific)
Multicore
pipelining
superscalar
single core vs multicore
cores by cpu/proc core
hearts
core by cpu/proc core
shared memory (time & storage)
Parallelism
arch
multiprocessor
thread lvl
GPU
ILP
applications
DLP
TLP
dependent of instr on another
Data (regs reg)
Name (memory)
ctrl (loop)
RAW hazard
WAW
e.g. loop lvl parallelism
replicate (loop unroll)
branch prediction
speculation
speculable code
RISC vs CISC
- simpler "ability" → impl cost (design & manufacture)
- less instructions → those part } power efficiency
simpler design
- execute instruction stages
↳ pipeline
I/O
controlled
sys bus
I/O controller
I/O dev
hide internals
interface
types of regs
ctrl
status regs → NRCH
flag → busy
err (opperation)
data regs
write/read
states (buffer data)
stable
stable
toggle
functions
buffering
cmd & status
cmd code
err detect
slow speed bus
bridge
high speed bus
polling
busy waiting
interrupt driven
pagination (policy)
interrupt driven
DMA
hardware
hyperthreading (multicore prog)
transfer data rate
Do interrupts cpu when busy
busy waiting
busy waiting
busy waiting