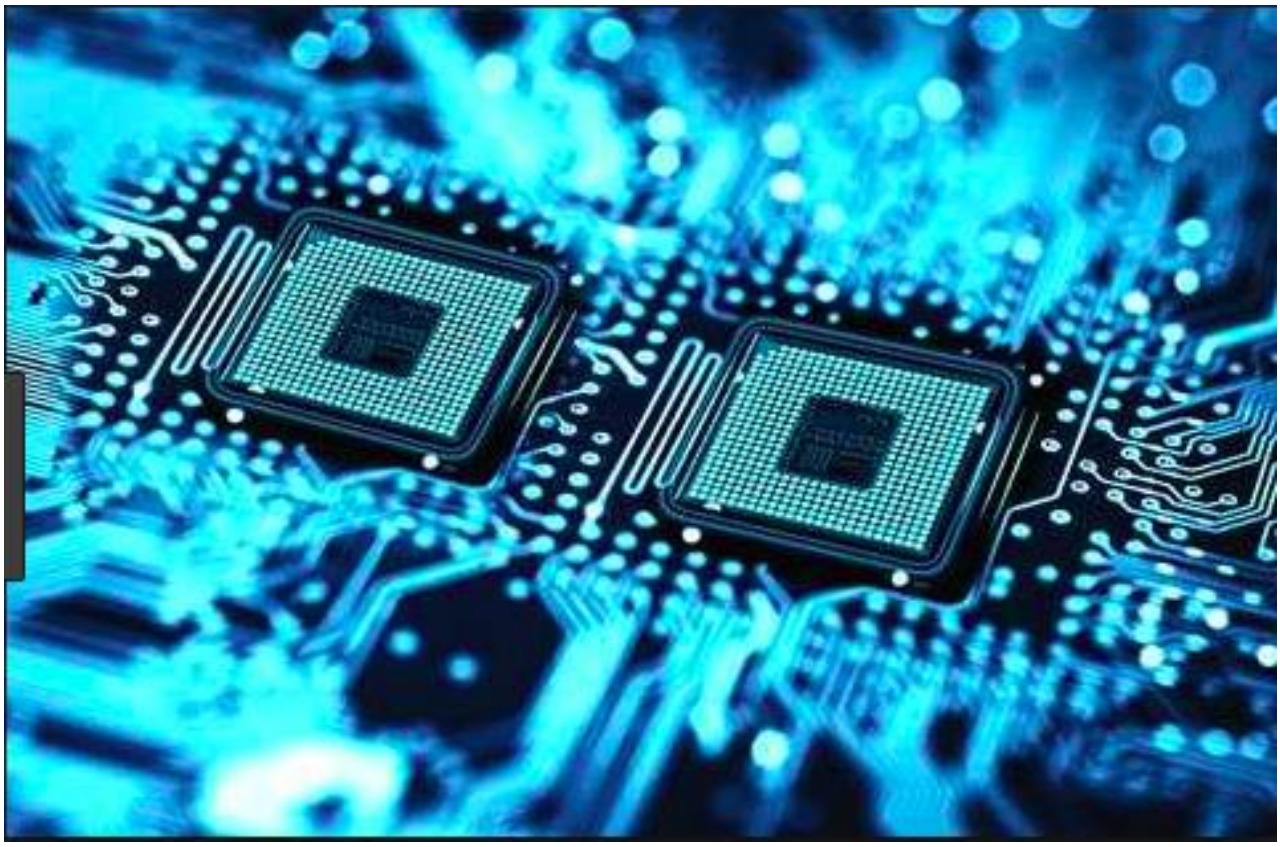
CS2022 COMPUTER ARCHITECTURE

Project 2

MICROCODED INSTRUCTIONS SET PROCESSOR



Submitted To: Mr. Michael Manzke

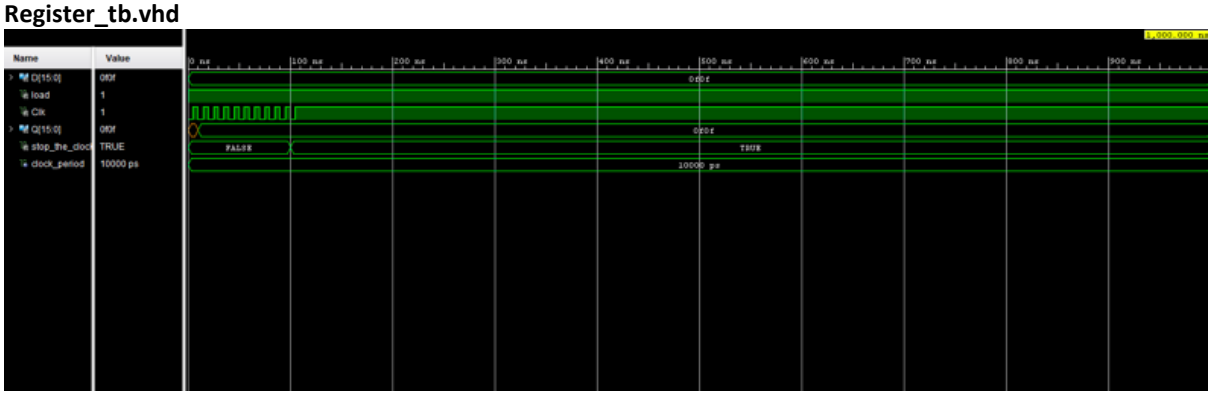
Submitted By: Kavin Gupta
17317505

The VHDL codes are in filenames given corresponding to the components.

COMPONENTS REQUIRED:

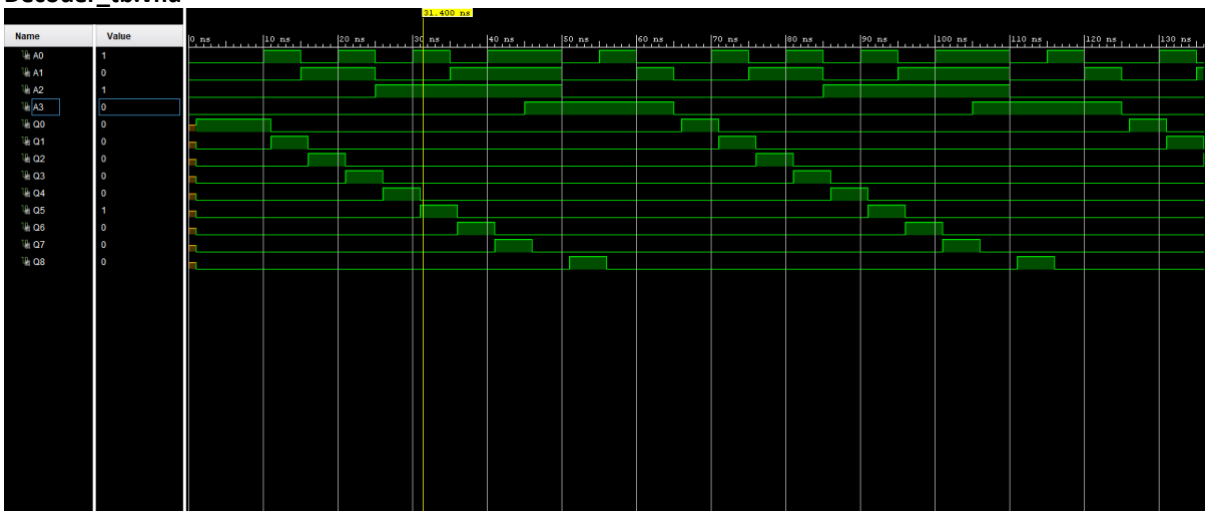
1. Register:

Register.vhd
Register_tb.vhd



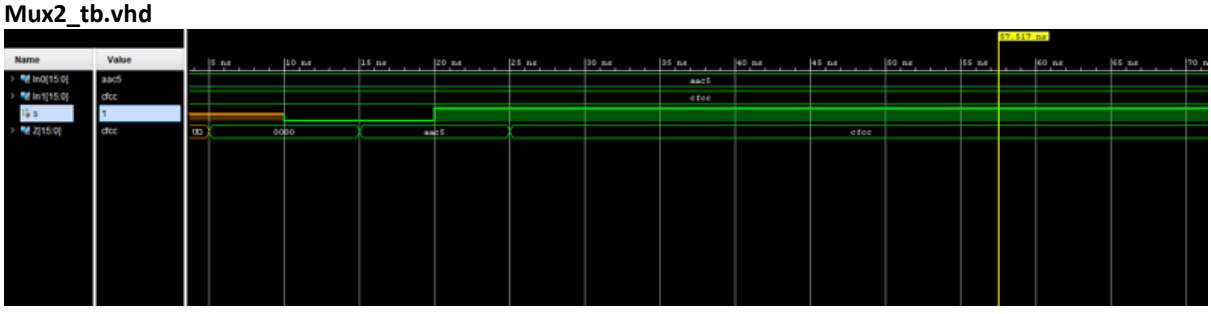
2. Decoder:

Decoder_4to9.vhd
Decoder_tb.vhd



3. Multiplexer 2 to1

Mux_2to1.vhd
Mux2_tb.vhd



4. Multiplexer 2 to 16

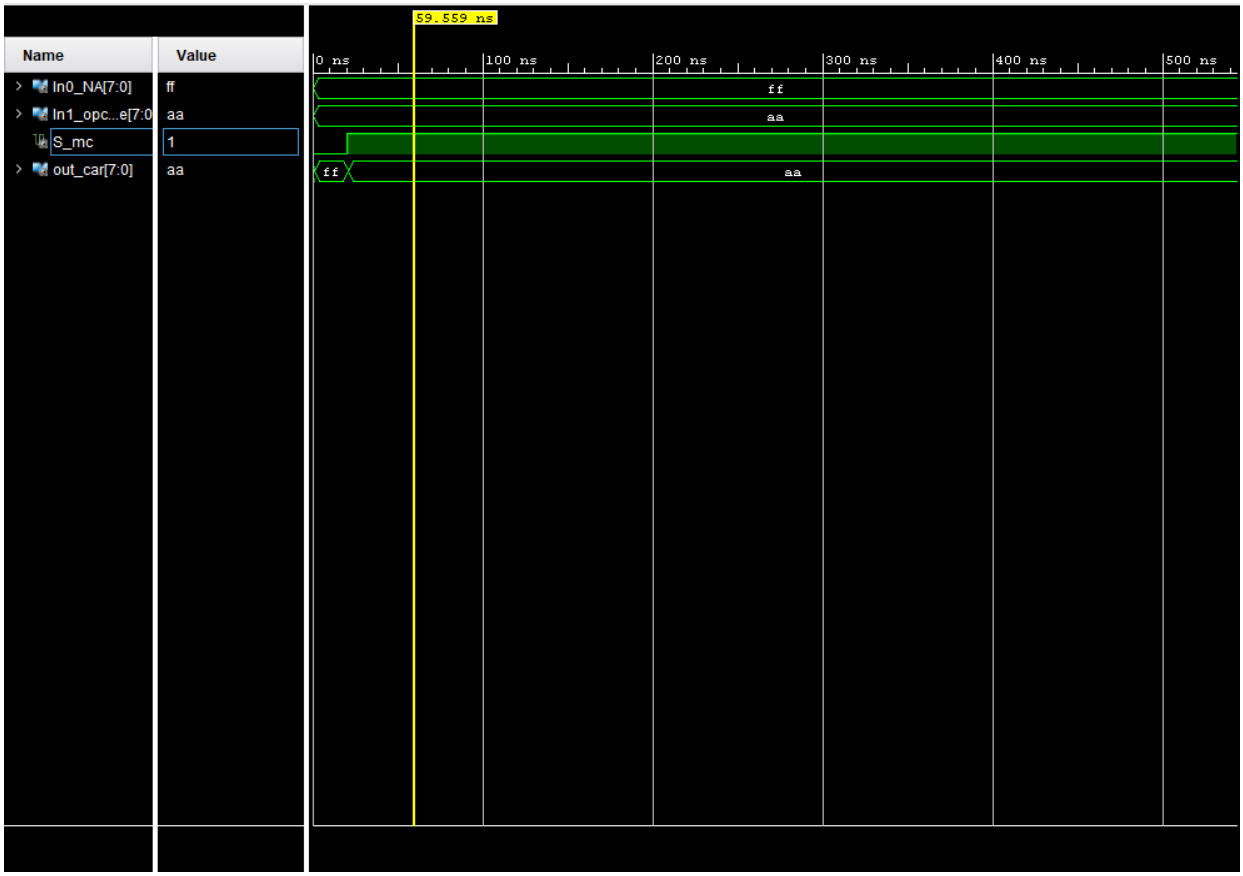
Mux_2to16.vhd

NO testbench required

5. Multiplexer 2 to 8

Mux2to8.vhd

Mux2to8_TB.vhd



6. Multiplexer 3 to1

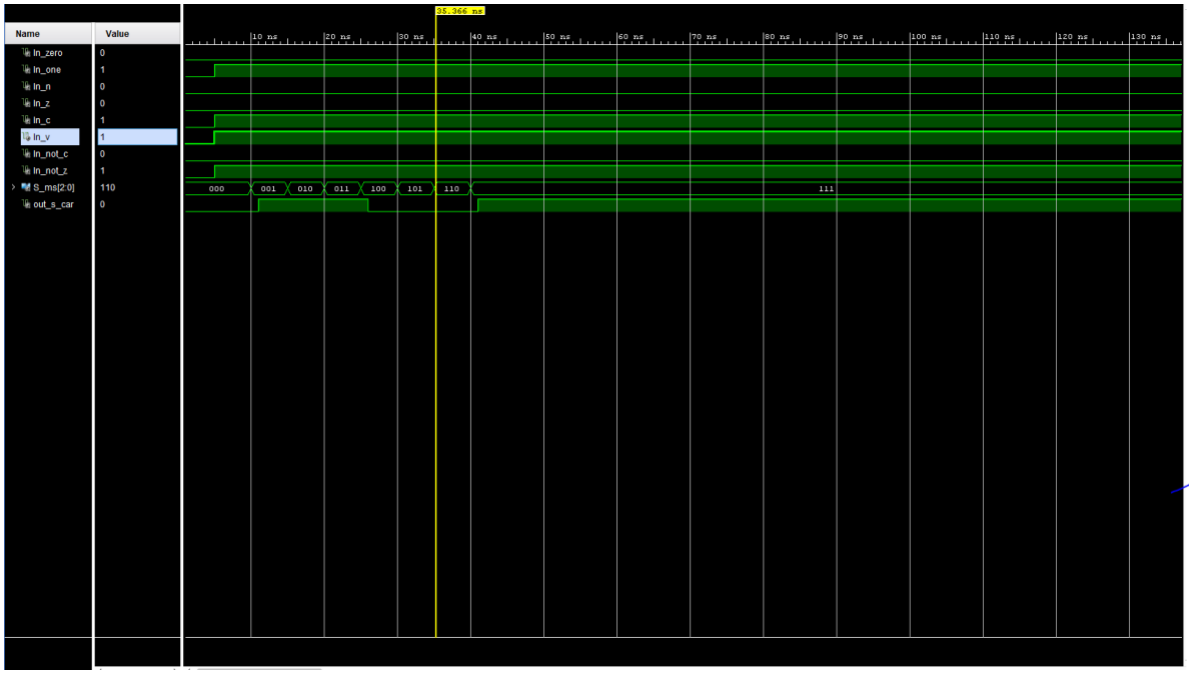
Mux_3to1.vhd

No test bench required as it used in Barrel shifter and it is shown working below.

7. Multiplexer 8to1

Mux8to1.vhd

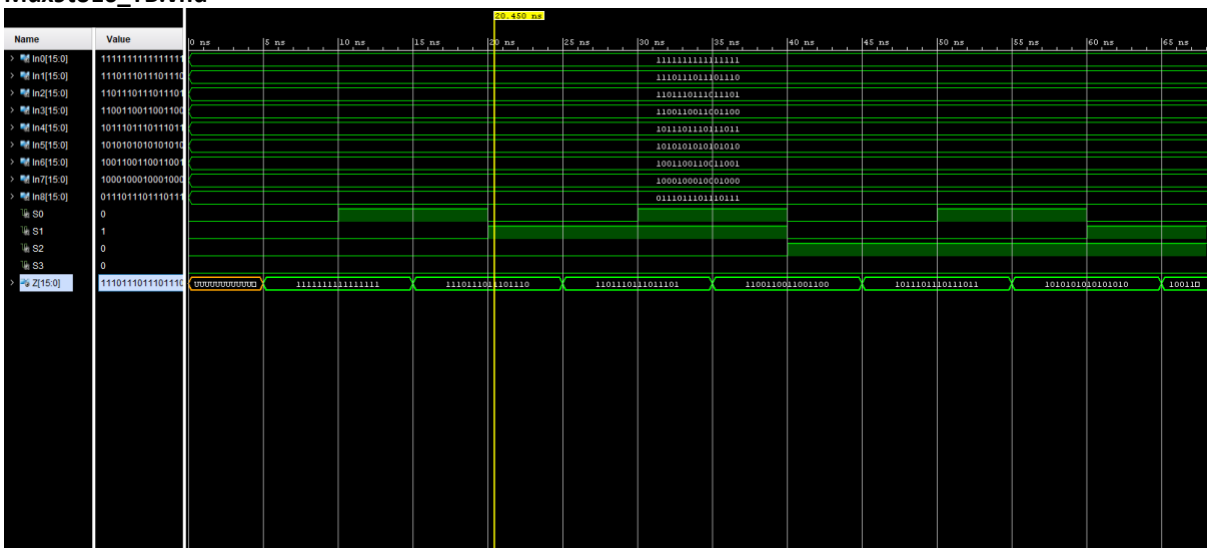
Mux8to1_TB.vhd



8. Multiplexer 9 to 16

Mux9to16.vhd

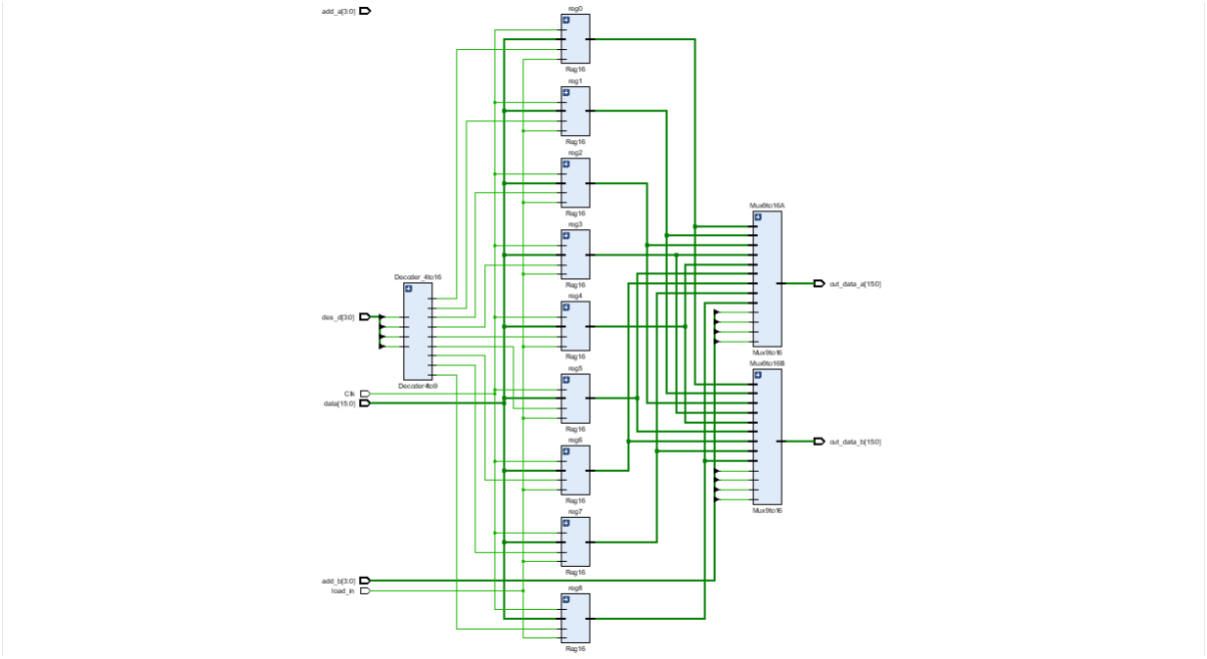
Mux9to16_TB.vhd



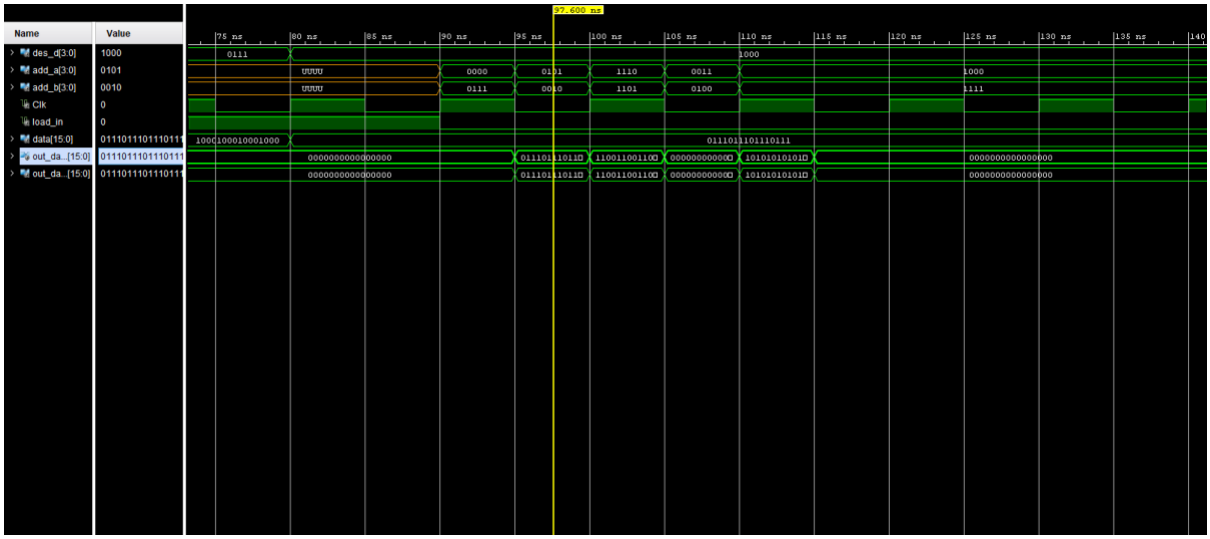
9. Register File

Reg_file.vhd

Regfile_tb.vhd



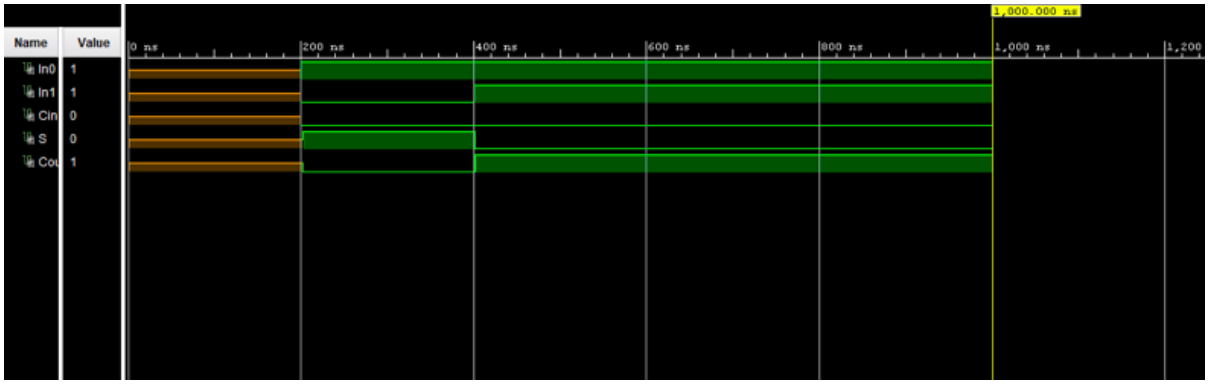
Schematic of Register File



10.Full Adder

Full-adder.vhd

Fulladder_tb.vhd



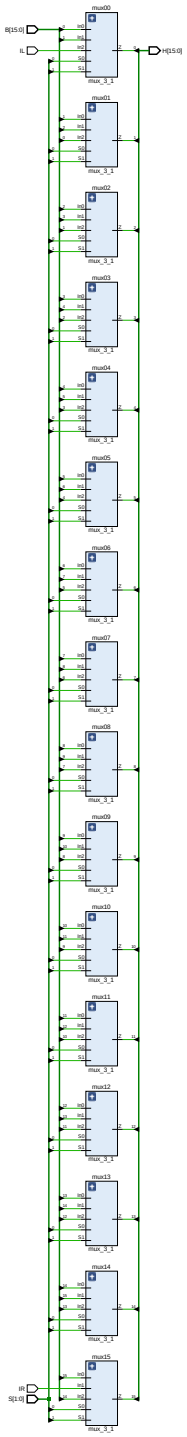
11.Ripple Adder

Ripple_adder.vhd

No test bench required as full adders are shown working and ripple adder is shown working below.

12.Barrel Shifter

Barrel_shifter.vhd

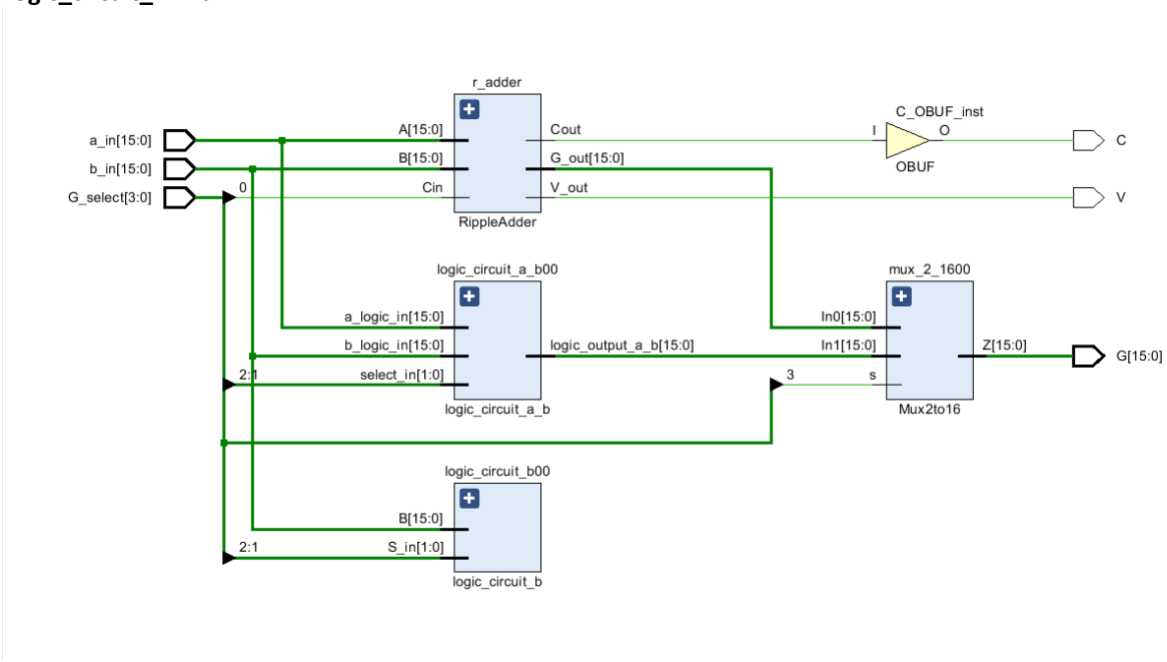


Schematic of Barrel Shifter

No test bench Required as it is shown working below.

13.Arithmetic Logic Unit

ALU_16bit.vhd
Logic_circuit_1.vhd
Logic_circuit_2.vhd

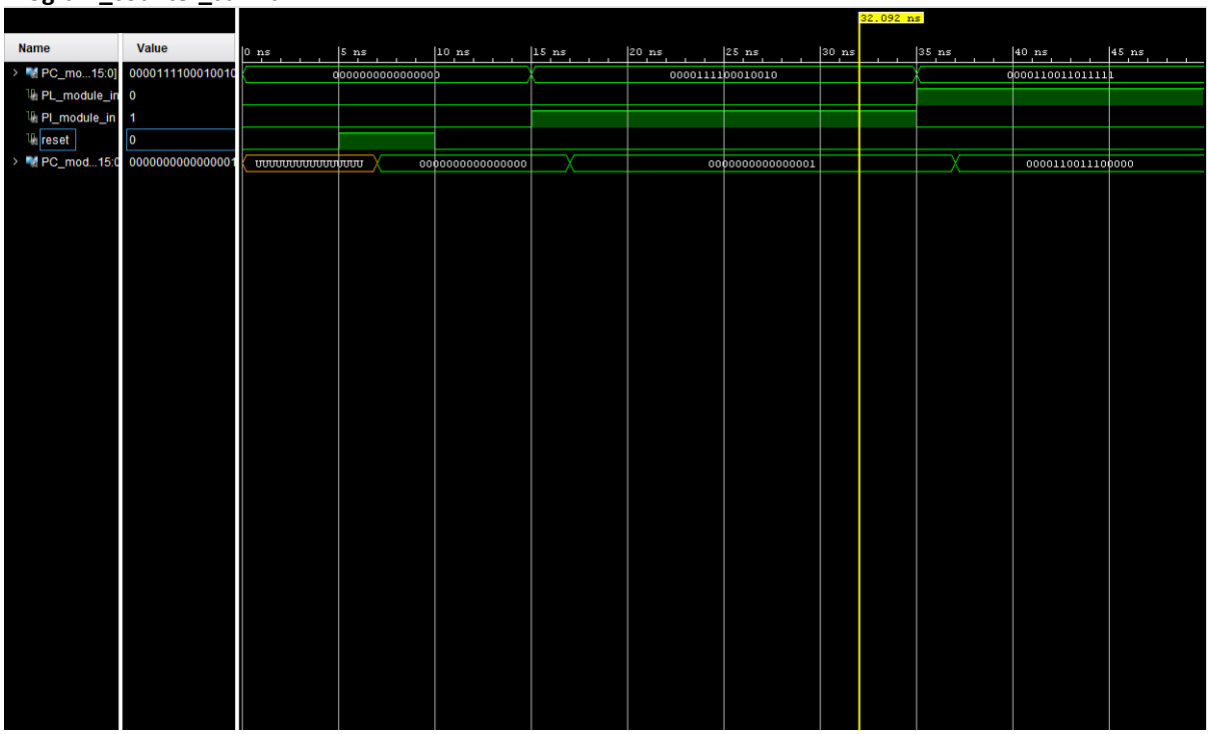


Schematic for Arithmetic Logic Unit

No testbench Required

14.Program Counter

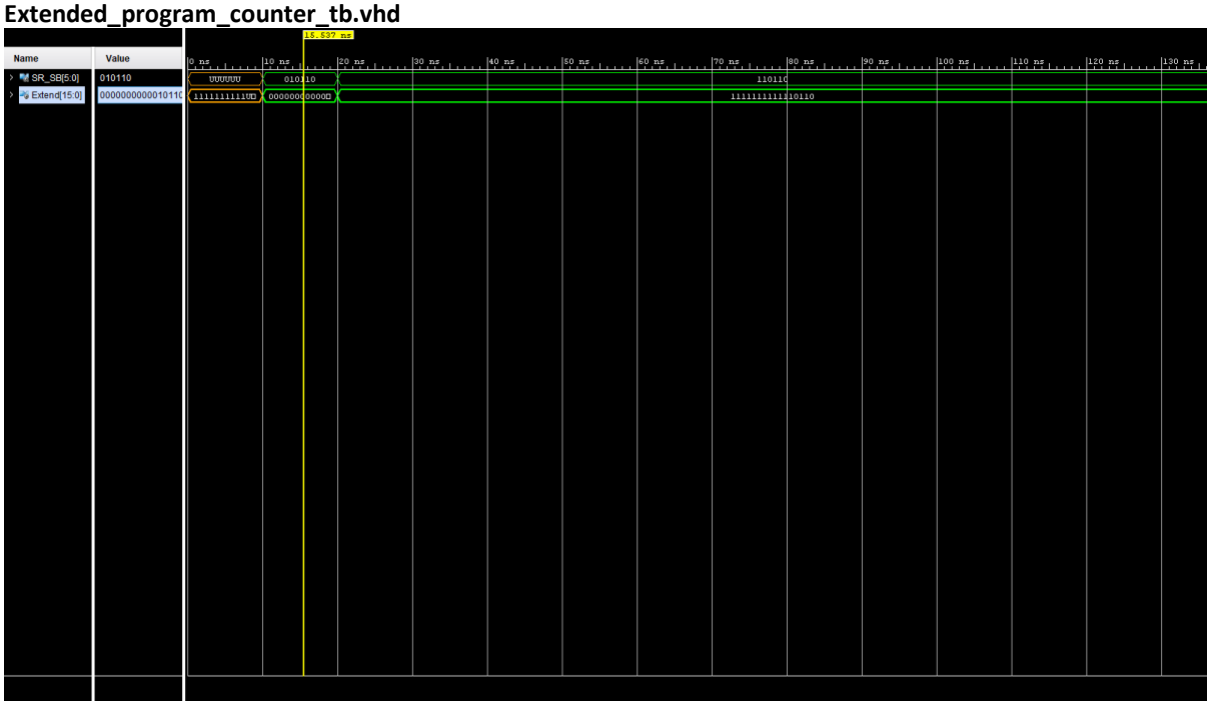
Program_counter.vhd
Program_counter_tb.vhd



15.Extended program Counter

Extended_program_counter.vhd

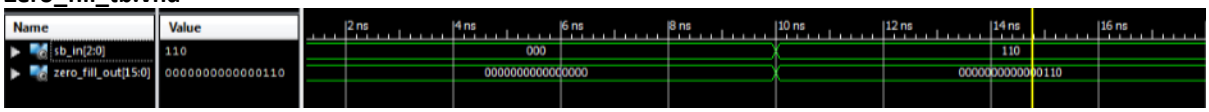
Extended_program_counter_tb.vhd



16.Zero fill

Zero_fill.vhd

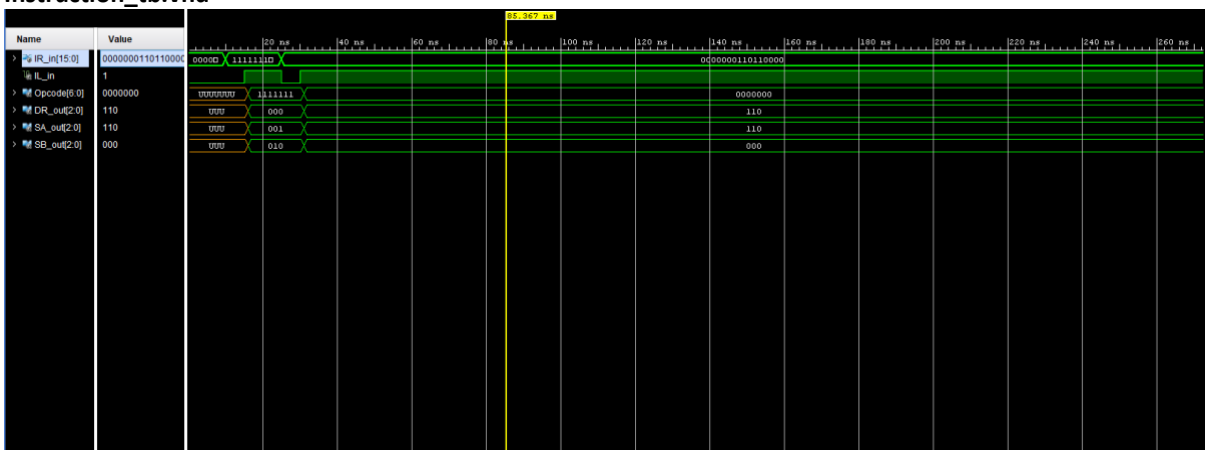
Zero_fill_tb.vhd



17.Opcode

Instructions.vhd

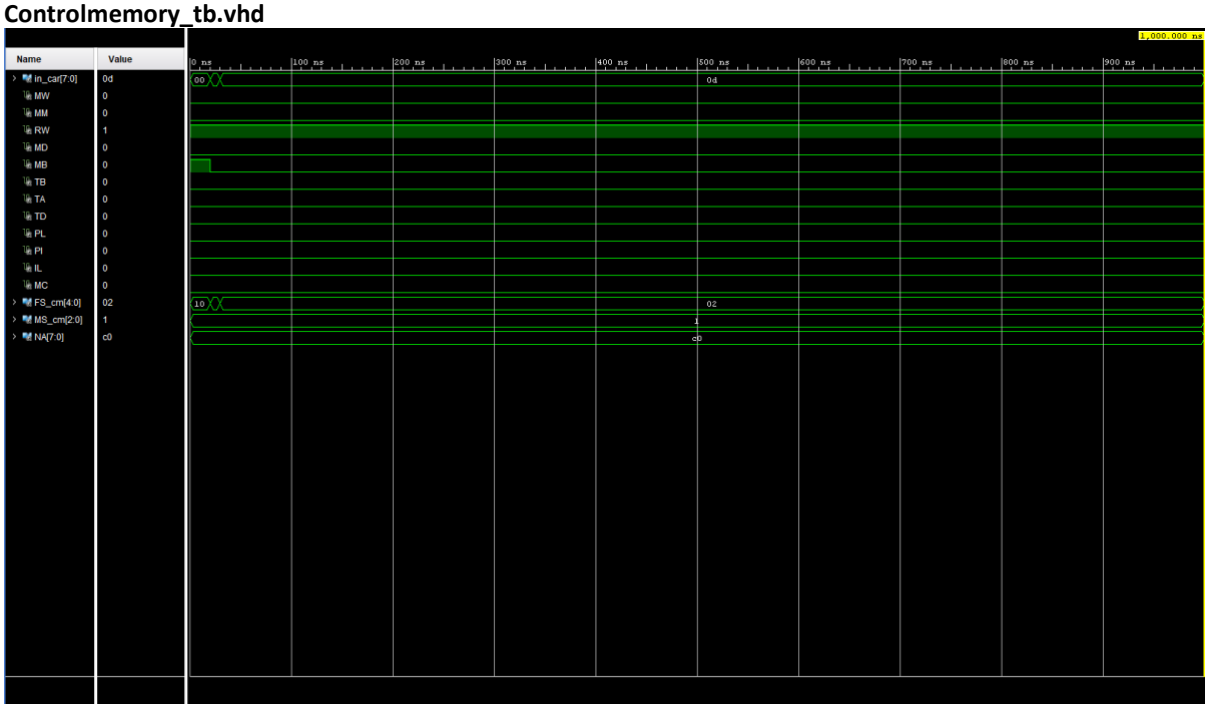
Instruction_tb.vhd



18.Control Memory

Control_memory.vhd

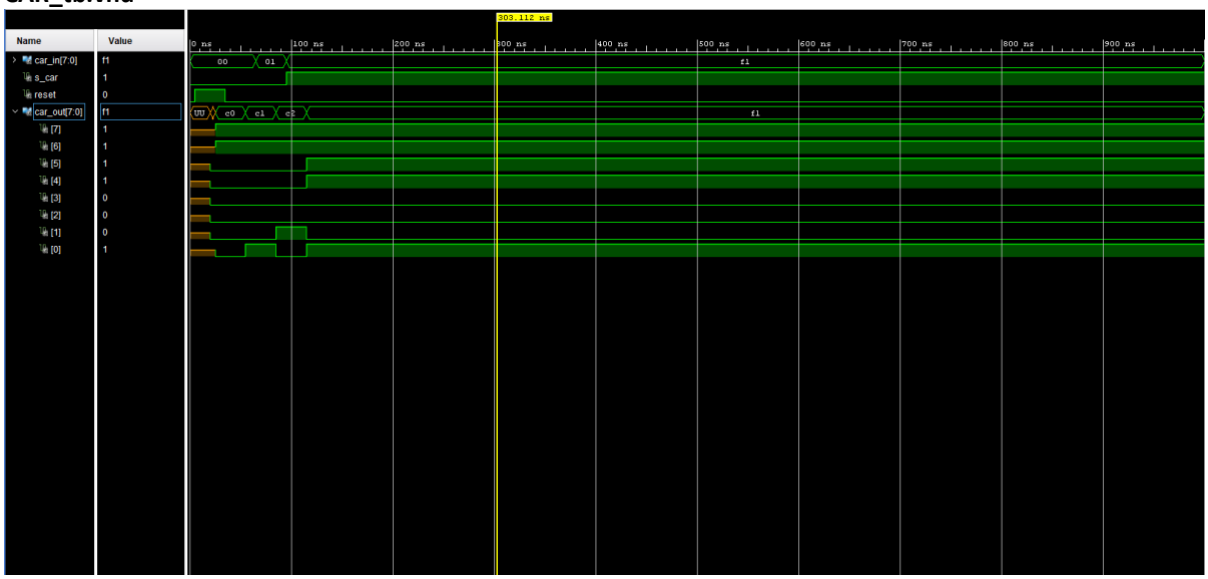
Controlmemory_tb.vhd



19.Control Address Register

Control_address_reg.vhd

CAR_tb.vhd



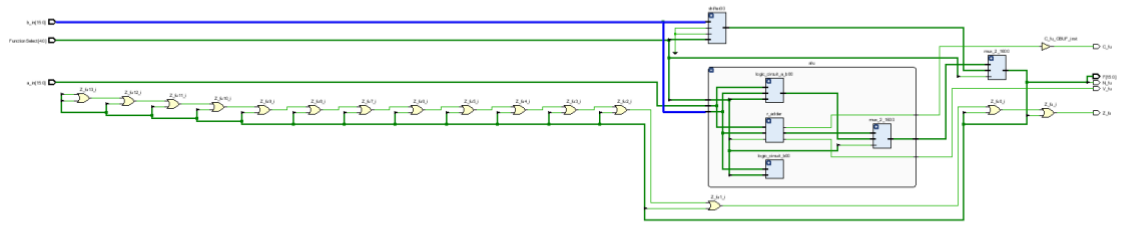
20.Memory

Memory.vhd

Memory_tb.vhd

21.Functional Unit

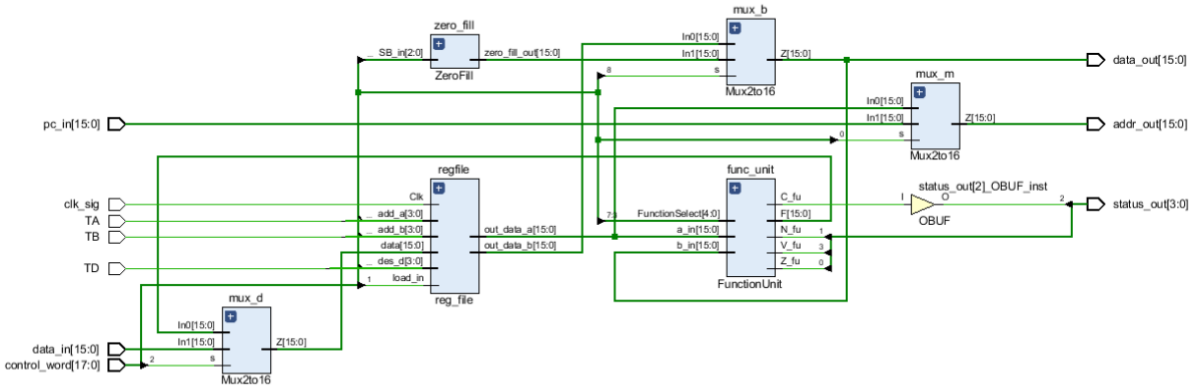
Functional_unit.vhd



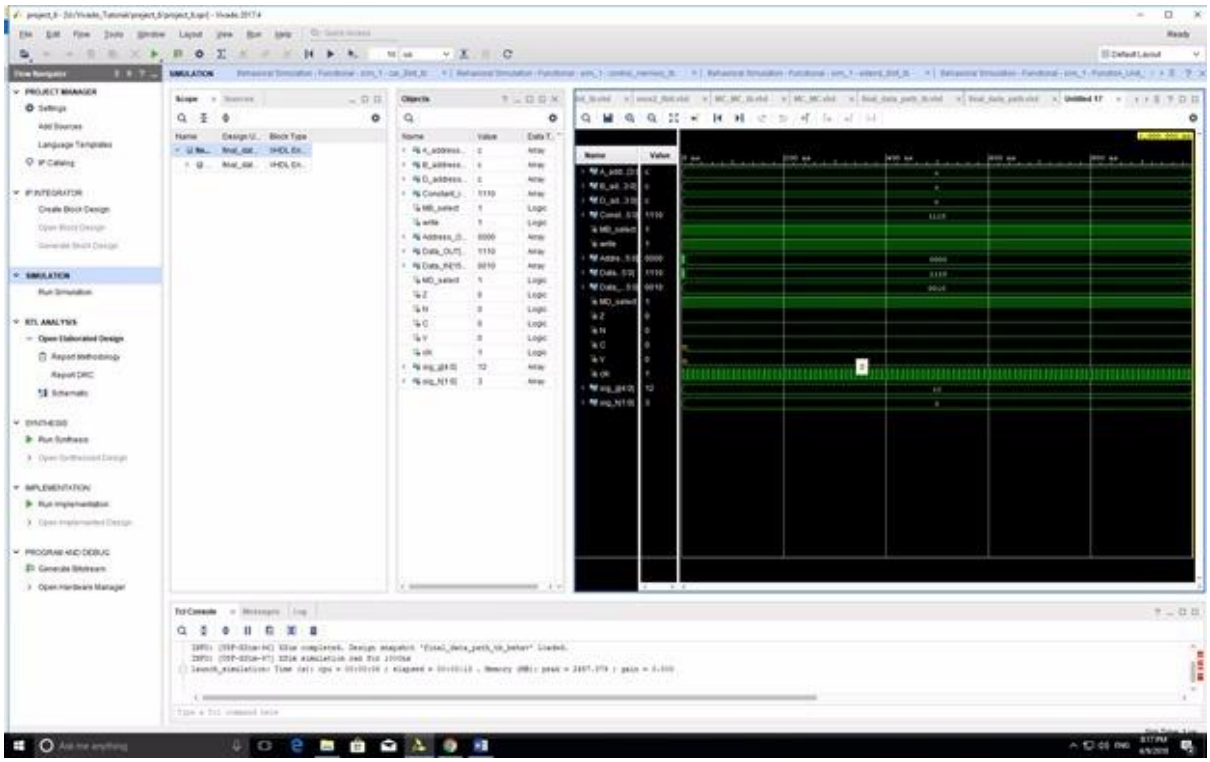
Schematic for Functional Unit

22.Data path

Datapath.vhd
Datapath_tb.vhd

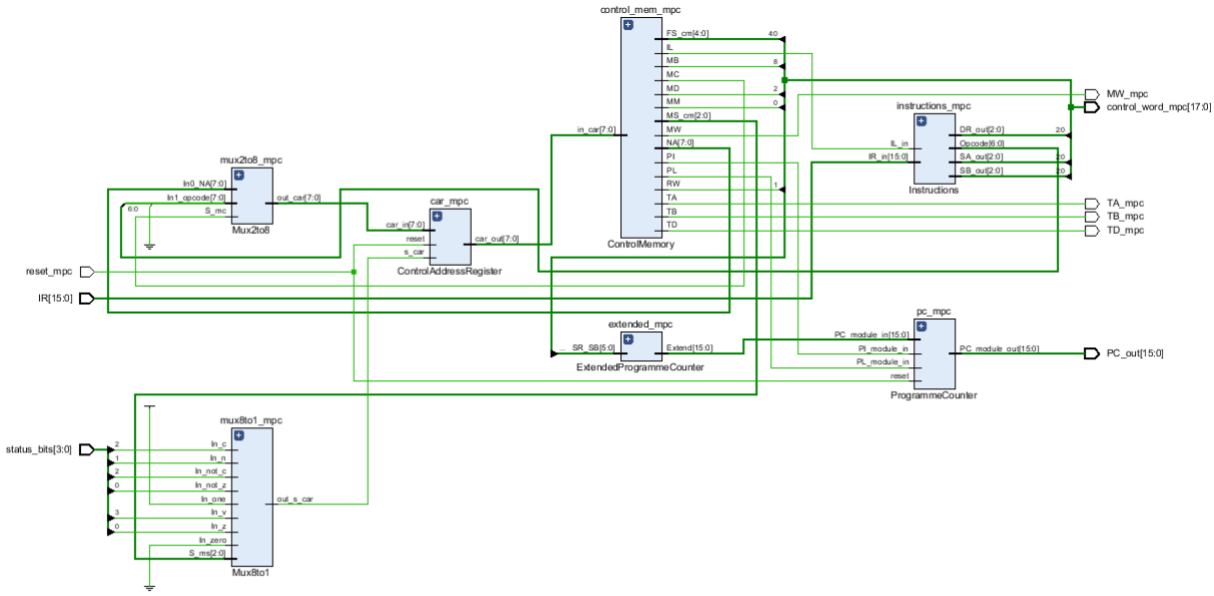


Schematic of Datapath



23.Microprogram controller

Microprogramer_controller.vhd

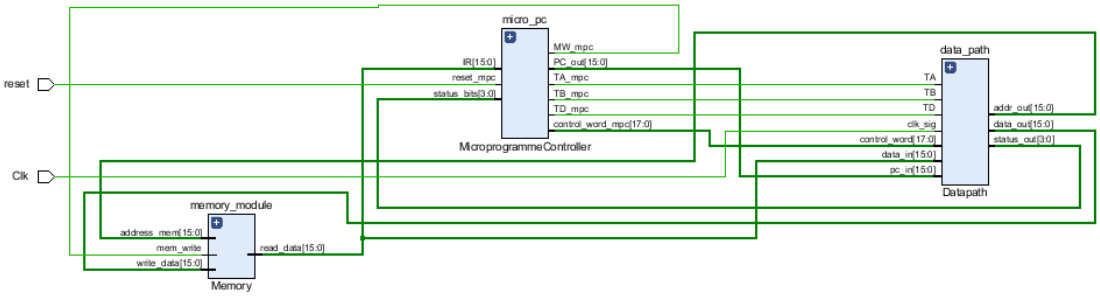


Schematic of Micro Program Control

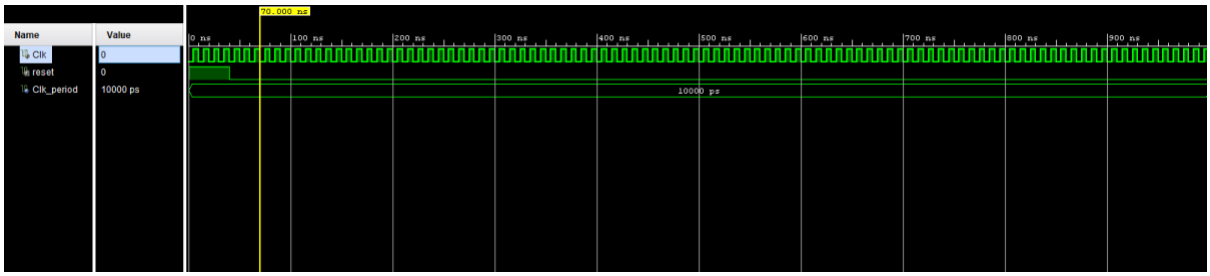
24.Final

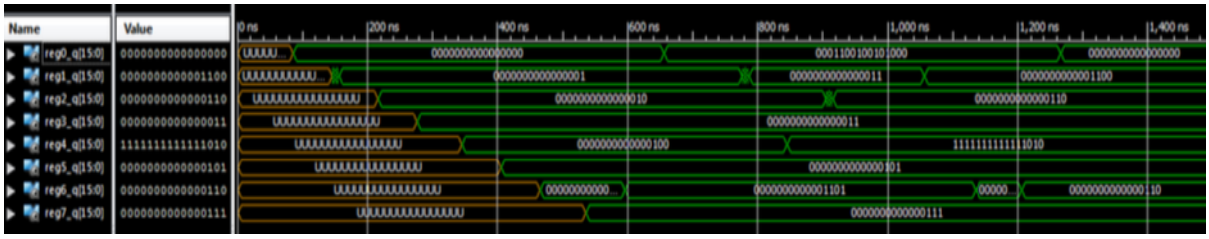
Proj2.vhd

Proj_tb.vhd



Schematic Overall





This testbench shows the output of registers in the final as the operations are being performed.

The test benches show the result of operands performed by each component with the arithmetic state machine.

With expansion of register file from the previous project, Memory and Control Memory have been added with sized 512X16 and 256X28, each with 16-bit width buses that utilize 9 lest significant bits of addresses provided in order to index to the 512-bit memory size.

Microprogram Operations have been implemented for control memory. Each change and resulting operation in time via the register test bench is reflected by loading, add Immediate operand (ADI), load to register (LDR), increment (INC), store (STR), add (ADD), inverse(NOT), unconditional branch (BCH) and conditional branch (BXX). These pertain to modify the content of registers in memory at given time intervals, and more easily seen in the control memory.