Competency 02

2.3 Explores the Von-Neumann Architecture

Time: 6 periods

Learning Outcomes

- Describes the stored program concept
- Names the major components of Von-Neumann architecture
- Describes fetch-execute cycle
- Briefly describes ALU, CU, Memory (Registers), data and control bus
- Draws the Von-Neumann Architecture model and names its components
- Describes the need of multi-core processors

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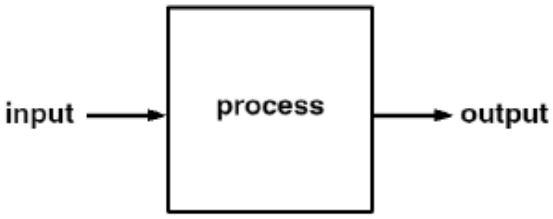
Computer

Input –Instructions and data

Process – Performed by the processor

Output - Information

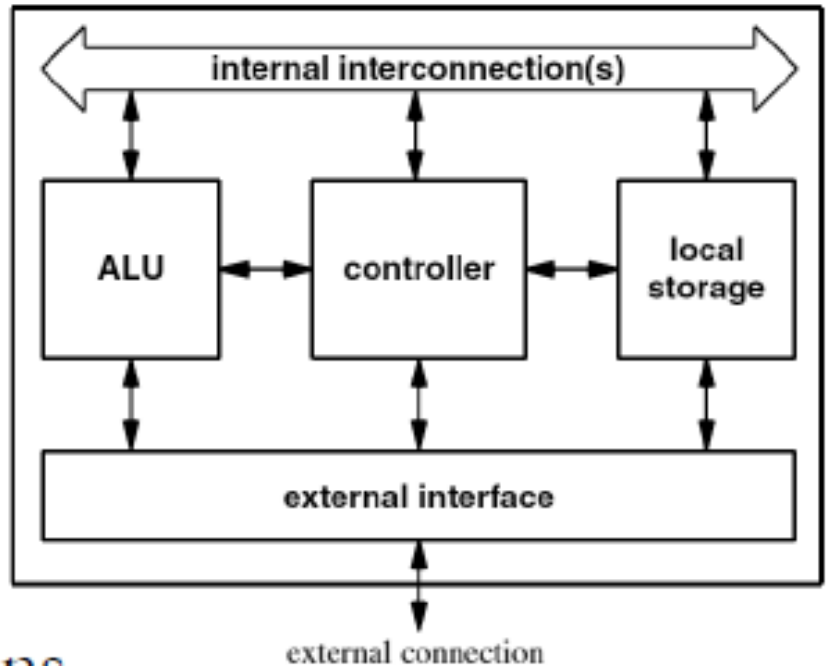


Processor

A processor is digital device that can perform one or more computations involving multiple steps. The processor is a one of building blocks of computer systems.

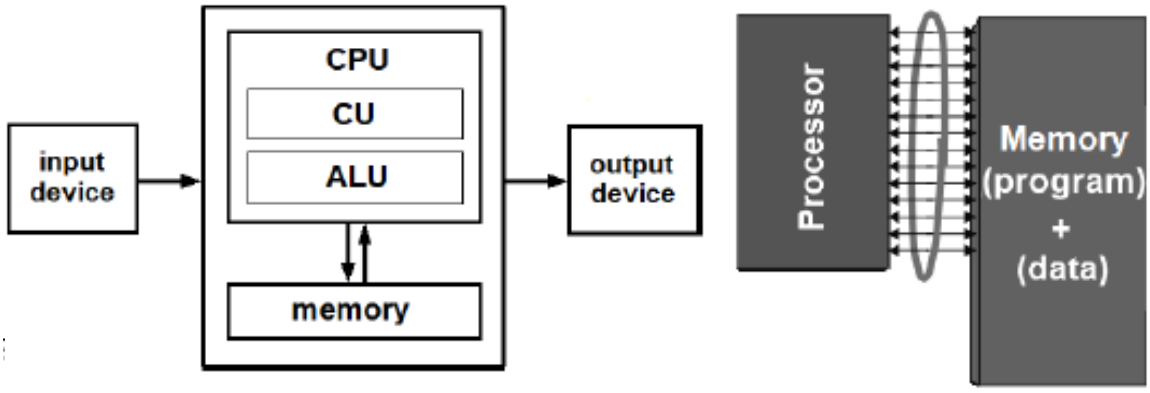
Components of Processor

- **Controller Unit (CU)** – Steps through programs and coordinates actions of other components.
- **Arithmetic and Logical Unit (ALU)** –Performs arithmetic and logical operations
- **Logical Storage** – Holds data and instructions for operations
- **Internal Interconnections** – move data and instructions among other internal components
- **External interface** – connect external devices

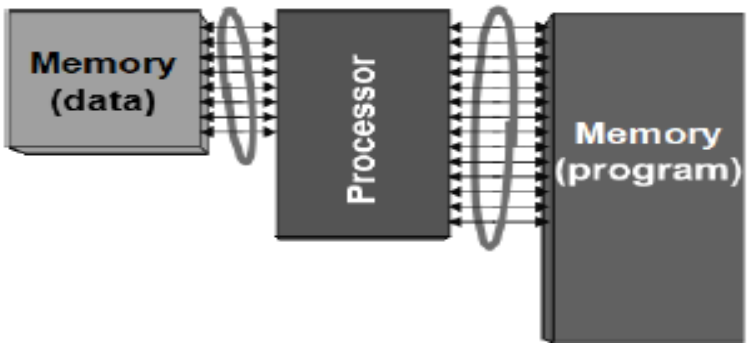


Computer Architectures

- Von Neumann architecture
  - Proposed by John von Neumann in the late 1940s
  - Bus is shared to access both instructions and data in memory (both instructions and data cannot be accessed at the same time)
  - Simple and inexpensive but limited performance
  - Bus becomes bottleneck (von Neumann bottleneck)



- Harvard architecture
  - Two separate memories for instructions and data
  - Two separate buses to access data memory and program memory
  - Complex and expensive but better performance
  - Avoid Von Neumann bottleneck



Stored Program Concept

The term Stored Program Control Concept refers to the storage of instructions in computer memory to enable it to perform a variety of tasks in sequence or intermittently.

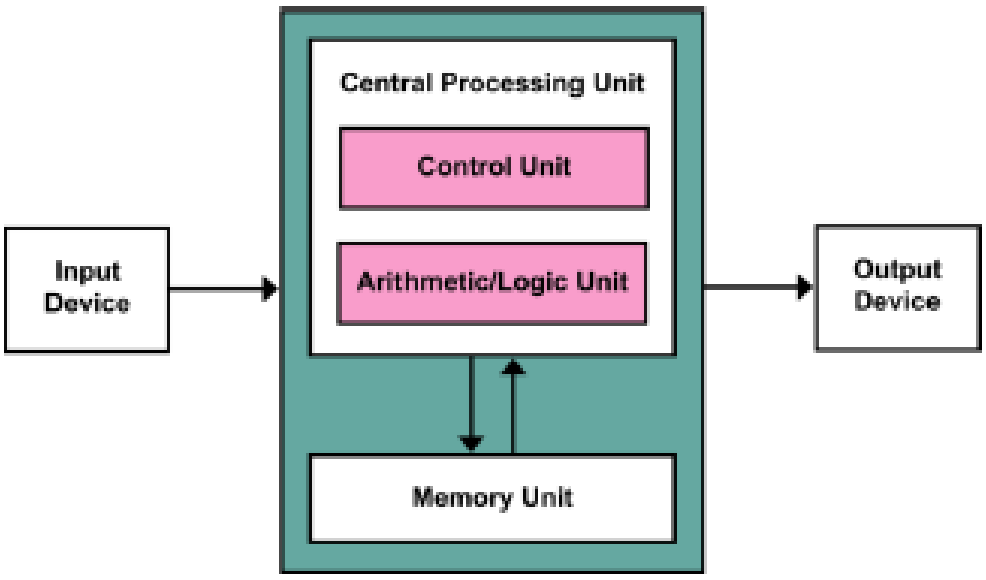
The idea was **introduced** in the late 1940s by **John von Neumann** who proposed that a program be electronically stored in the binary-number format in a memory device so that instructions could be modified by the computer as determined by intermediate computational results.

ENIAC (Electronic Numerical Integrator and Computer) was the first computing system designed in the early 1940s. It was based on Stored Program Concept in which machine use memory for processing data.

Stored program approach in brief,

- Program consists of set of **instructions** to be performed
- Program is **stored** in a location (**memory**) that the processor can access
- Processor accesses the program stored in memory (**stored program**) and follows instructions
- Convenient to change the instructions and processor performs accordingly (**programmable**)

Major components of Von-Neumann architecture



Von Neumann Architecture consists of a CPU, memory and input output devices. The program is stored in the memory. The CPU fetches an instruction from the memory at a time and executes it.

1. **Central processing unit**
   (i) Control unit (CU) - this unit controls signals of all devices of a computer system.
   (ii) Arithmetic and logic unit (ALU) - it carries out mathematical and logical operations.
2. **Memory register**

A CPU register is one of a small set of data holding places which is part of the computer processor. A register may hold an instruction, a storage address, or any kind of data.

Program Counter –

A program counter (PC) is a CPU register in the computer processor which has the address of the next instruction to be executed from memory. As each instruction gets fetched, the program counter increases its stored value by 1. It is a digital counter needed for faster execution of tasks as well as for tracking the current execution point.

Instruction Register –

In computing, an instruction register (IR) is the part of a CPU's control unit that holds the instruction currently being executed or decoded. An instruction register is the part of a CPU's control unit that holds the instruction currently being executed or decoded. Instruction register specifically holds the instruction and provides it to instruction decoder circuit.

Memory Address Register –

The Memory Address Register (MAR) is the CPU register that either stores the memory address from which data will be fetched from the CPU, or the address to which data will be sent and stored. It is a temporary storage component in the CPU (central processing unit) which temporarily stores the address (location) of the data sent by the memory unit until the instruction for the particular data is executed.

Memory Data Register –

The memory data register (MDR) is the register in a computer's processor, or central processing unit, CPU, that stores the data being transferred to and from the immediate access storage. Memory data register (MDR) is also known as memory buffer register (MBR).

General Purpose Register –

General purpose registers are high speed storage locations and used to store temporary data within the microprocessor. Supports two operations such as fetch and store. Usually large enough to hold an integer. It is a multipurpose register. They can be used either by programmer or by a user.

Floating Point Registers -

Separate from General Purpose Registers and large enough to hold one floating point value.

Programming with Registers

- Example
  Add values in variables X and Y in memory, and store the result in variable Z in memory

```
r3 ← load X
r4 ← load Y
r5 ← add r3, r4
Z ← store r5
```

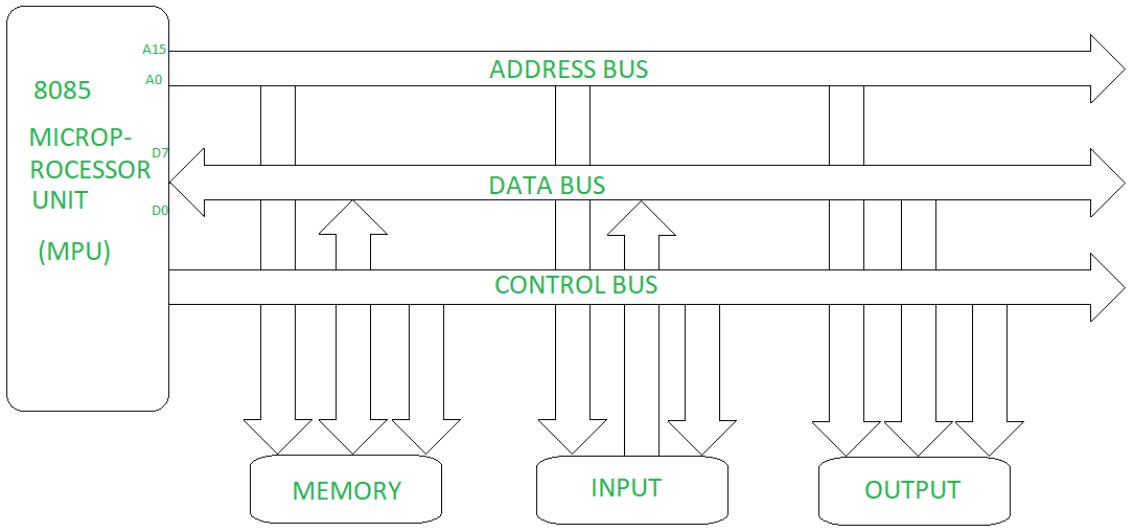
3. **Memory**
   (i) Primary memory
   (ii) Secondary memory

4. **Input device**

5. **Output device**

Bus

Bus is a group of conducting wires which carries information, all the peripherals are connected to microprocessor through Bus.



Bus organization system of 8085 Microprocessor

There are three types of buses.

Address bus –

It is a group of conducting wires which carries address only. Address bus is unidirectional because data flow in one direction, from microprocessor to memory or from microprocessor to Input/output devices (That is, Out of Microprocessor).

Length of Address Bus of 8085 microprocessor is 16 Bit and the microprocessor 8085 can transfer maximum 16 bit address which means it can address 65, 536 different memory location.

The Length of the address bus determines the amount of memory a system can address. Such as a system with a 32-bit address bus can address 2^32 memory locations. If each memory location holds one byte, the addressable memory space is 4 GB.However, the actual amount of memory that can be accessed is usually much less than this theoretical limit due to chipset and motherboard limitations.

Data bus –

It is a group of conducting wires which carries Data only. Data bus is bidirectional because data flow in both directions, from microprocessor to memory or Input/output devices and from memory or Input/output devices to microprocessor.

Length of Data Bus of 8085 microprocessor is 8 Bit.

When it is write operation, the processor will put the data (to be written) on the data bus, when it is read operation, the memory controller will get the data from specific memory block and put it into the data bus.

The width of the data bus is directly related to the largest number that the bus can carry, such as an 8 bit bus can represent 2 to the power of 8 unique values, this equates to the number 0 to 255.A 16 bit bus can carry 0 to 65535.

Control bus –

It is a group of conducting wires, which is used to generate timing and control signals to control all the associated peripherals, microprocessor uses control bus to process data that is what to do with selected memory location. Some control signals are:

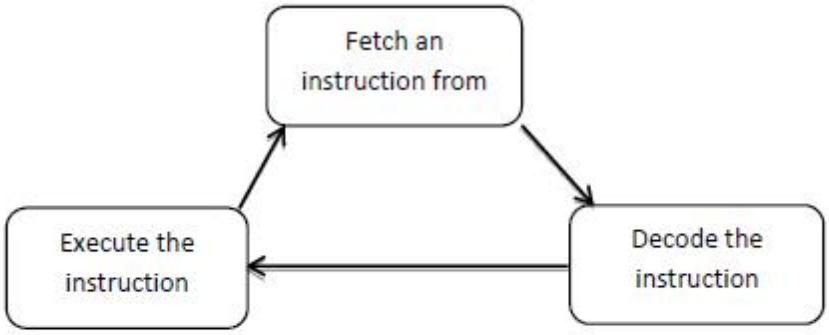
- Memory read
- Memory write
- I/O read
- I/O Write
- Opcode fetch

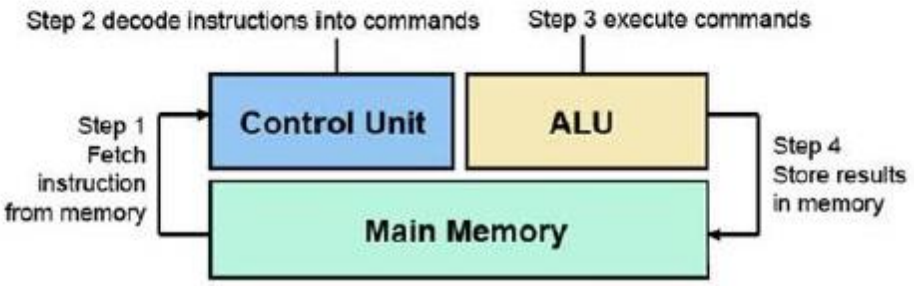
If one line of control bus may be the read/write line. If the wire is low (no electricity flowing) then the memory is read, if the wire is high (electricity is flowing) then the memory is written.

Fetch – Execution Cycle

- Basis of programmable processors
- Allows processor to move through program instructions automatically
- Implemented in processor hardware

```
repeat forever
{
    fetch : read the next instruction from the location
        that the program is stored
    execute : execute the fetched instruction
}
```





Fetch-Execute Algorithm

```
PC ← memory address of first instruction
repeat forever
{
   fetch : read the next instruction
           into IR using address in PC
   IAR ← address beyond the instruction
           that was just fetched
   execute : execute the instruction
           in IR
   PC ← IAR
}
```

memory

address	value
0x00000000	instruction 1
0x00000004	instruction 2
0x00000008	instruction 3
0x0000000C	instruction 4
0x00000010	instruction 5
0x00000014	instruction 6
0x00000018	instruction 7
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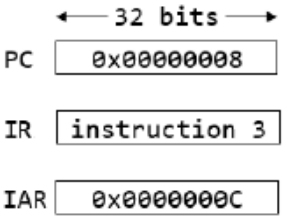

Multi-core processors

A multi-core processor is a single computing component with two or more independent actual processing units (cores), which are units that read and execute program instructions. Therefore, the single processor can run multiple instructions on separate cores at the same time.

Need of multi-core processor

- Can be run a program by dividing some parts. So it gets executed fast.
- It enables parallel programming.
- To get the high performance from a single machine.

References

Teachers' Guide 2017

https://www.javatpoint.com/store-program-control-concept

https://www.geeksforgeeks.org/computer-organization-alu-and-data-path/

T. O'Leary, L. O'Leary and D. O'Leary, Computing Essentials 2017: Making IT work for you, 26th Edition, pp. 116 - 128, McGraw-Hill, 2017