Low Power VLSI

PROJECT

Topic : Gating Techniques- Clock Gating

Gating Technique For Power Reduction :

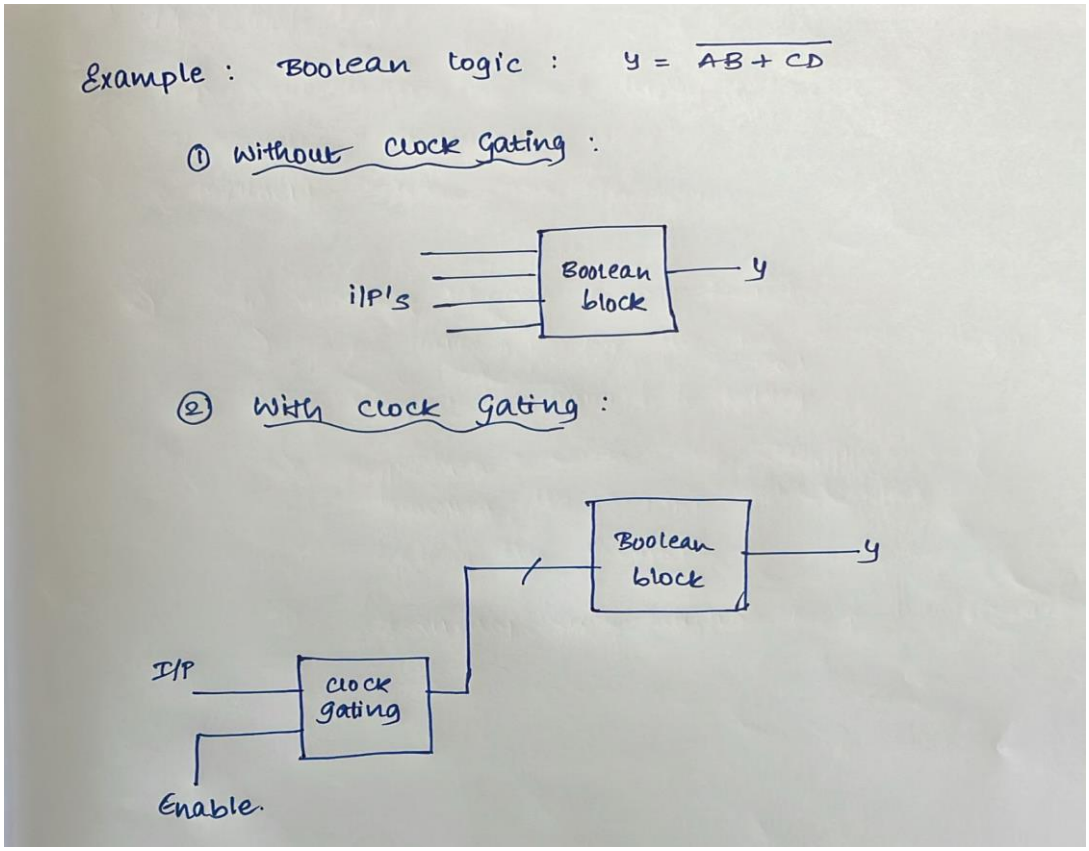
CLOCK GATING

Clock gating is a methodology to turn off the clock to certain parts of the digital design when not needed.

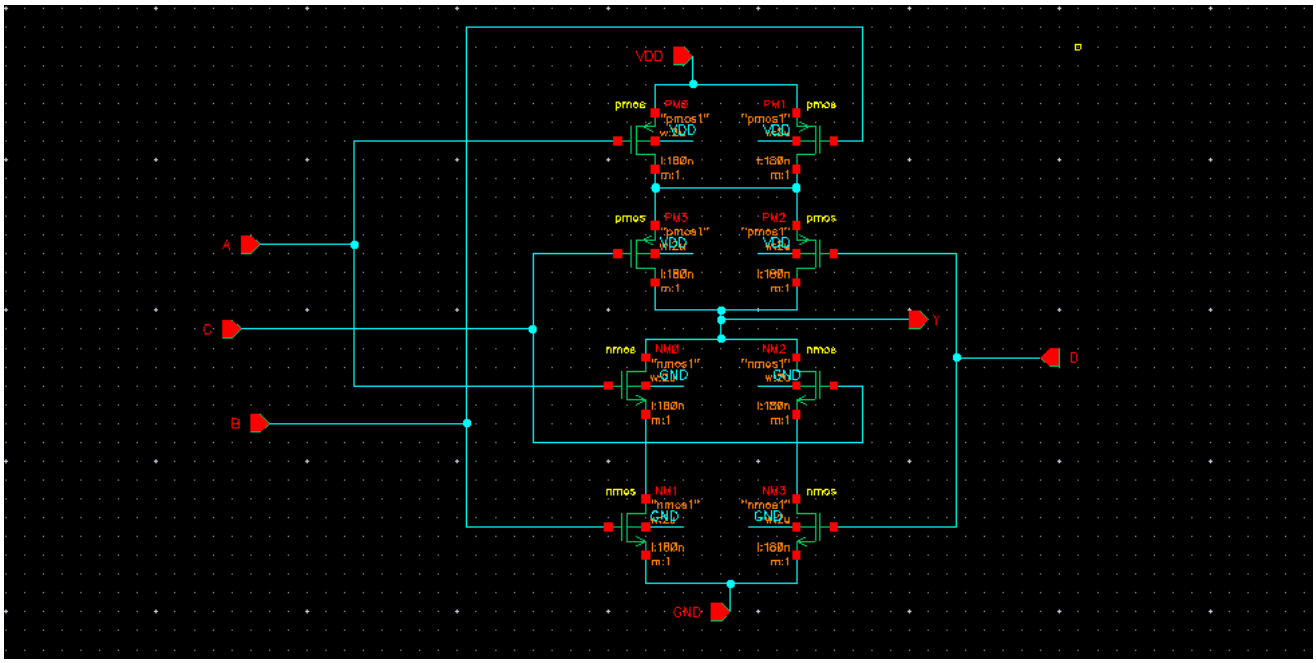
We use additional hardware in our circuits for this purpose.

The technique of clock gating is used to reduce the clock power consumption by cutting off the idle clock cycles.

Block Diagram:

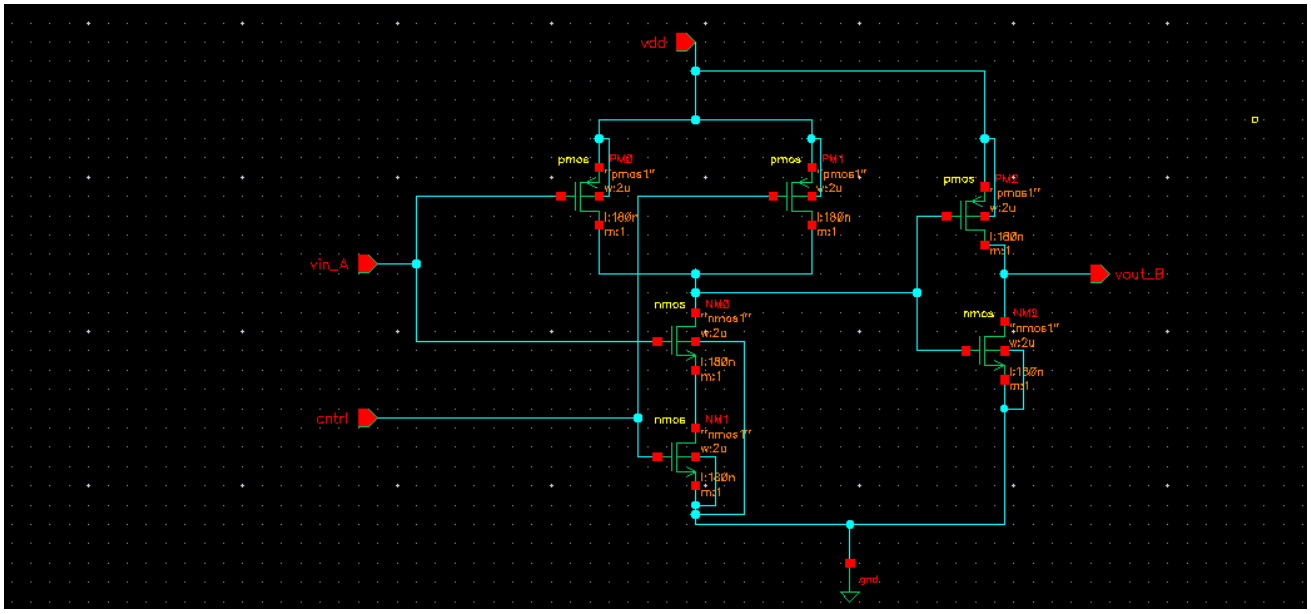


BOOLEAN LOGIC SCHEMATIC: Y=(AB+CD)’



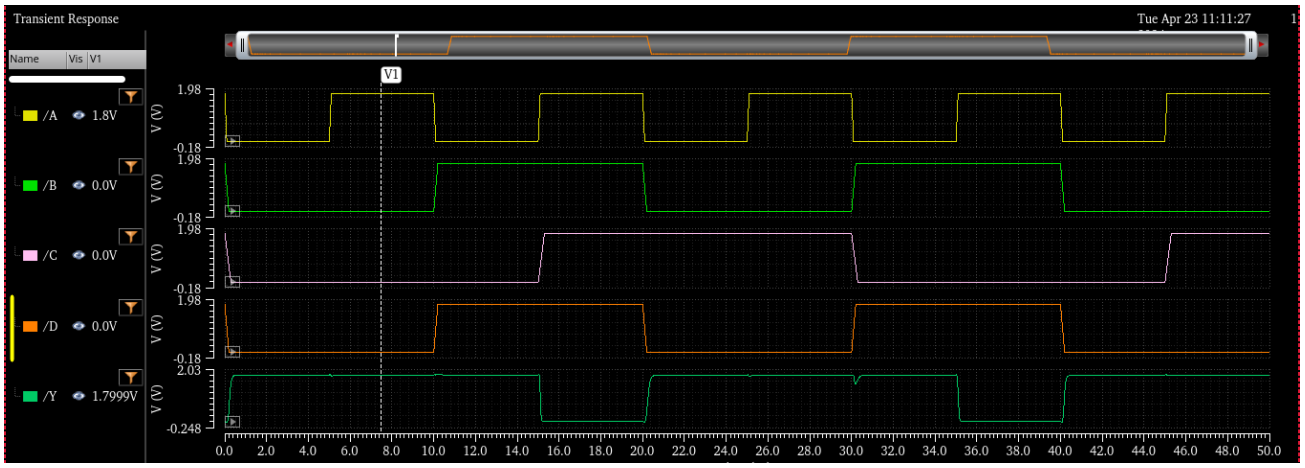
This is the boolean block that we are implementing clock gating on.

AND GATE:



AND Gate for clock gated circuit with cntrl as the deciding pin for gating.

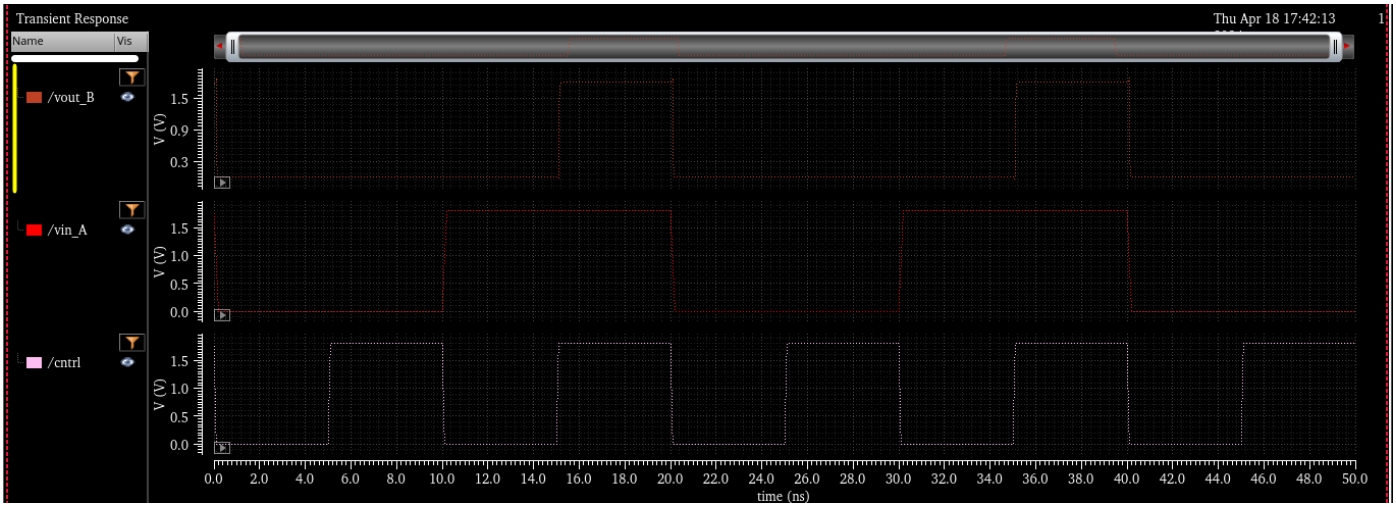
Testing for Boolean block:



When A=HIGH, B=LOW, C=LOW, D=LOW,

Therefore output Y=HIGH; from the Boolean example chosen.

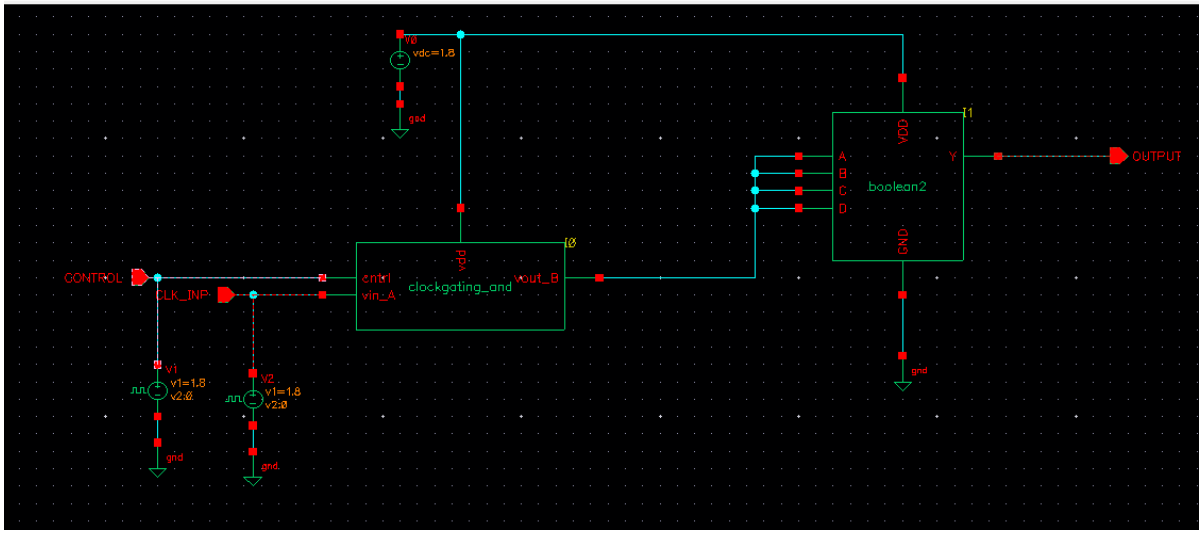
Testing for AND block for Clock Gating:



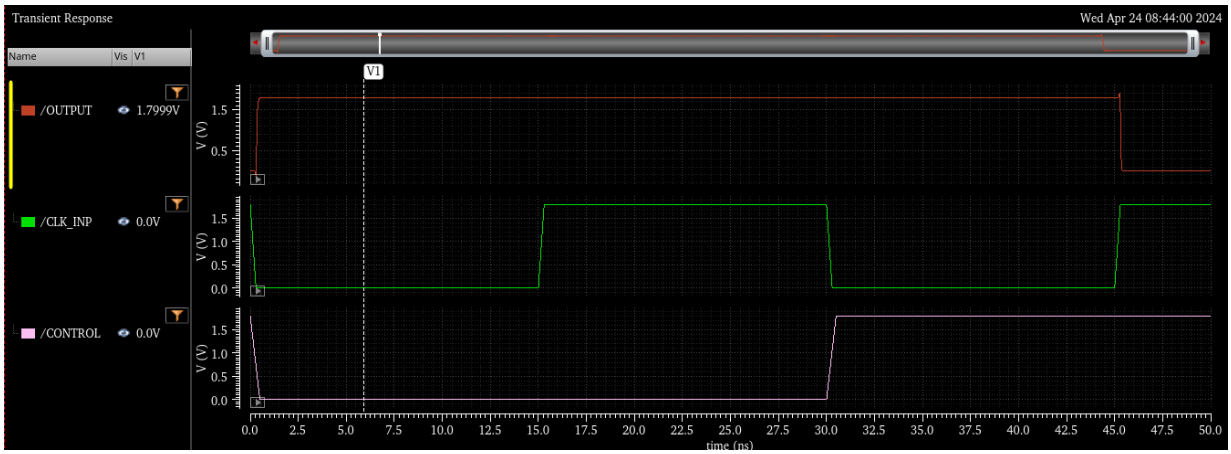
When cntrl signal is HIGH only then Vin= Vout.

Or else when Cntrl is LOW Vout will not be equal to Vin and rather be Low (zero) .

CLOCK GATED BOOLEAN BLOCK Schematic:



Analysis :



When control = LOW ; the output of clock gating block will be zero(low) so since the Boolean block gets this value as input the output will be y=(input)' because of Boolean logic example taken.

Note that here the input to Boolean is not having any switching activities.

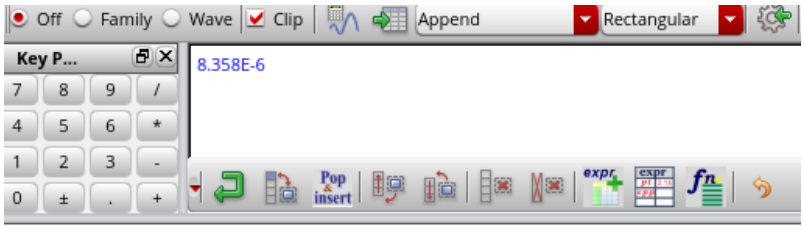
Similarly when control = HIGH; the output will be HIGH(Vin value) and hence the output will be y=(input)'.

Note that here the input to Boolean block will have switching activities.

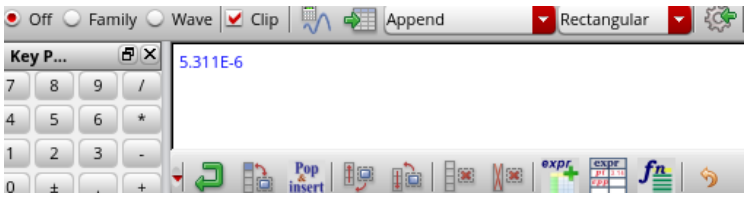
So by using clock gated block we are reducing the number of switching activities at the input of the clock gated block whenever it is not in use

(cntrl = 0) and hence reducing the power in comparison to a non gated block where gating is not done to switching activities even when it is not needed; as it contributes a big part to the power.

POWER ANALYSIS :



The power calculated for the block without clock gating turned out to be 8.358 microwatts.



The power calculated for the block with clock gating gave a value of 5.311 microwatts.

Hence we can observe a reduction in power of the digital circuit on the implementation of said gating technique as it helps reduce the unwanted switching activities at blocks where signals are not required that contribute to the power in the whole system.