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PRANVEER SINGH INSTITUTE OF TECHNOLOGY KANPUR

Session 2023-24 Pre-University

Odd Semester B. Tech.-III Semester

Computer Organization and Architecture (BCS-302)

CO	Course Outcome
CO1	Able to define **[1. Remember]** and relate **[1. Remember]** the various components of digital system, register, bus architecture, addressing mode, pipelining and interrupt types with digital system.
CO2	Able to describe **[2. Understand]** and discuss **[2. Understand]** the ALU and its micro operation, instruction format, instruction cycle, hardwired and micro programmed control and various modes of data transfer.
CO3	Able to apply **[3. Apply]** & calculate **[3. Apply]** various arithmetic operation techniques using different hardware algorithms.
CO4	Able to differentiate **[4. Analysis]** and categories **[4. Analysis]** various memory such as cache memory, auxiliary memory and virtual memory.

Time: 3 Hrs. M. M. 70

Section A

Q1. Attempt all questions: **(2X7 = 14 Marks)**

a) Show the following conditional control statement by two register transfer statement with control function. If(P=1)then (R3←R2) else if (Q=1)then (R3←R2) CO1

b) Describe Bus Arbitration with diagram. CO2

c) Compare Hardwired and Micro programmed Control Unit. CO2

d) Explain the difference between RISC and CISC. CO2

e) Illustrate the 'Direct 'and 'Indirect' addressing modes. CO3

f) Discuss 2D and 2.5D RAM organization. CO2

g) Describe Input Output Interface with diagram. CO2

Section B

Q2. Attempt all questions: **(7X3 = 21 Marks)**

a) Draw and explain the block diagram of Look ahead carry generator. CO2

b i) Analyze the step of multiplication process of (15) X (-13) using Booth's algorithm. CO4

OR

ii) Investigate arithmetic expression using stack organized computer with 1-address instruction: X=(A-B)*(((C-D*E)/F)/G) CO4

c i) Explain the procedure of mapping Cache memory to Main memory and its types with proper diagram. CO2

OR

ii) Describe how the computer buses can be used to communicate with memory and I/O. Also show the communication between CPU and IOP. CO2

Section C

Q3. Attempt any one part of the following questions: **(7X1 = 7 Marks)**

a) Draw and explain the block diagram of DMA controller. CO2

OR

b) Explain the concept of 5-bit by 3-bit Array Multiplier using diagram and example. CO2

Q4. Attempt any one part of the following questions: **(7X1 = 7 Marks)**

a) Draw a diagram of a Bus system using multiplexer and three state bus buffers. CO2

OR

b) Describe the signed magnitude division with help of flow chart and divide the following: 01110 00000 by 1000. CO2

Q5. Attempt any one part of the following questions: **(7X1 = 7 Marks)**

a) An instruction is stored at location 500 with its address field at location 501.The address field has the value 600.A processor register R2 contains the number 300.Identify the effective address if the addressing mode of the instruction is: CO1

i) direct
ii) indirect
iii) immediate
iv) relative
v) register indirect
vi) index with R2 as index register

OR

b) A digital computer has a common bus system for 16 registers of 32 bit each. The bus is constructed using multiplexers. CO1

a) Find select input are there in each multiplexer.
b) Calculate the size of multiplexers needed.
c) Find multiplexers are there in the bus.

Q6. Attempt any one part of the following questions: **(7X1 = 7 Marks)**

a) A four way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K x 32. CO3

a) Formulate all pertinent information required to construct the cache memory.
b) Find the size of the cache memory.

OR

b) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers. Calculate the following: CO3

a) Number of RAM and ROM chips needed and address range for RAM, ROM and interface.
b) Show the memory-address map for the system.

Q7. Attempt any one part of the following questions: **(7X1 = 7 Marks)**

a) Analyze the different types of pipelining and pipeline hazards. CO4

OR

b) Investigate asynchronous data transfer and explain strobe and handshaking control with block diagram and timing diagram for source and destination initiated mode. CO4