**PRANVEER SINGH INSTITUTE OF TECHNOLOGY KANPUR**

Odd Semester Session 2023-24 CT-I

B. Tech.- 3rd Semester

# Computer Organization & Architecture (BCS-302)

| CO | Course Outcomes |
|---|---|
| CO1 | Able to define **[1. Remember]** and relate **[1. Remember]** the various components of digital system, register, bus architecture, addressing mode, pipelining and interrupt types with digital system. |
| CO2 | Able to describe **[2. Understand]** and discuss **[2. Understand]** the ALU and its micro operation, instruction format, instruction cycle, hardwired and micro programmed control and various modes of data transfer. |
| CO3 | Able to apply **[3. Apply]** & calculate **[3. Apply]** various arithmetic operation techniques using different hardware algorithms. |
| CO4 | Able to differentiate **[4. Analysis]** and categories **[4. Analysis]** various memory such as cache memory, auxiliary memory and virtual memory. |

Time: 1.5 Hrs. M. M. 20

## Section A

**(1X5 = 5 Marks)**

**Q1. Attempt all questions:**

a) Define the terms 'computer architecture' and 'computer organization'. CO1

b) List and briefly define the main structural components of a computer. CO1

c) Represent the following conditional control statements by two register transfer statements with control functions. CO1

If (P=1 and Q=1) then (R2←R4) else if (S=1) then (R2←R5)

d) Describe Three-state bus buffer. CO2

e) Define System bus with example. CO1

## Section B

**(2.5X4 = 10 Marks)**

**Q2. Attempt all questions:**

a i) A bus-organized CPU has 16 registers with 32 bits in each, an ALU, and a destination decoder. CO3

a. Calculate multiplexers are there and what is the size of each multiplexer.
b. Calculate inputs and outputs are there in the decoder.
c. Identify a control word for the system assuming that the ALU has 35 operations.

**Or**

ii) Formulate the control word that must be applied to the processor to implement the following micro-operations: CO3

a. R1 ← R2 + R3
b. R4 ← R4
c. R5 ← R5 - 1
d. R6 ← shl R1
e. R7 ← input

b i ) Demonstrate Bus arbitration along with example CO3

**Or**

ii) Illustrate Stack organization with example. CO3

c i) Construct a bus system using multiplexers having four registers of two bits each. CO3

**Or**

ii) Show the block diagram of the hardware that implements the following register transfer statement: (XY) Z: R7 ← R2, R2 ← R7 CO3

d i) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result. CO3

$(3 + 4)\ [10\ (2 + 6) + 8]$

**Or**

ii) Demonstrate register stack by describing corresponding push and pop micro-operations. CO3

## Section C

Q3 **(5X1 = 5 Marks)**

i) A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is: CO3

a. direct b. indirect c. relative d. indexed

**Or**

ii) Perform evaluation for the arithmetic statement: X = A + B * [C * D + E * (F + G)] CO3

a) Using a one address instruction

b) Using a zero address instruction