

B. Tech. III Semester

Computer Organization and Architecture (KCS-302)

CO Number	Course Outcome
CO1	Able to define [1. Remember] and relate [1. Remember] the various components of digital system, register, bus architecture, addressing mode, pipelining and interrupt types with digital system.
CO2	Able to describe [2. Understand] and discuss [2. Understand] the ALU and its micro-operation, instruction format, instruction cycle, hardwired and microprogrammed control and various modes of data transfer.
CO3	Able to apply [3. Apply] & calculate [3. Apply] various arithmetic operation techniques using different hardware algorithms.
CO4	Able to differentiate [4. Analysis] and categorise [4. Analysis] various memory such as cache memory, auxiliary memory and virtual memory.

Time: 1.5 Hrs.

M. M. 15

Q1. Attempt all questions:

Section A

(1X3 = 3 Marks)

- What are different phases of instruction cycle.
- Define selective set and selective clear operation by a suitable example.
- Show 6.3 in IEEE 754 single precision format.

CO1

CO1

CO3

Q2. Attempt all questions:

Section B

(2X4 = 8 Marks)

- Describe carry-lookahead adder with the help of block diagram.
- Discuss an array multiplier? Design an array multiplier that multiplies two 4-bit binary numbers.
- Perform Division process of 00001111 by 0011 (use a dividend of 8 bits.)
- Draw a flowchart for adding and subtracting two fixed point signed magnitude numbers.
- An 8-bit register contains the binary value 10011100. Examine the register value after an arithmetic shift right? Starting from the initial number 10011100, Examine the register value after an arithmetic shift left, and state whether there is an overflow.

CO2

CO2

CO3

CO3

CO4

Or

ii) Explain the concept of Overflow and Underflow in floating point numbers representation CO4  
with the help of example.

d i) Draw the flow chart of Instruction cycle. CO3

Or

ii) Register A holds the 8-bit binary 11011001. Calculate the B operand and the logic micro-operation CO3  
to be performed in order to change the value in A to:

a. 01101101

b. 11111101

### Section C

(4X1 = 4 Marks)

Q3

i) Draw the flow chart of Booth's algorithm for multiplication and show the multiplication CO3  
process using Booth's algorithm for  $(-7)X(+3)$ .

Or

ii) Sketch diagram of an arithmetic circuit with one selection variable S and two n-bit data CO3  
inputs A and B. The circuit generates the following four arithmetic operations in conjunction  
with the input carry  $C_{in}$ . Draw the logic diagram for the first two stages.

S	$C_{in}=0$	$C_{in}=1$
0	$D = A + B$ (Add)	$D = A + 1$ (Increment)
1	$D = A - 1$ (Decrement)	$D = A + B' + 1$ (Subtraction)