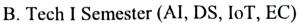
## PRANVEER SINGH INSTITUTE OF TECHNOLOGY KANPUR CT -I

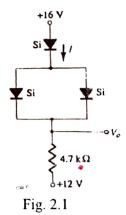
**Odd Semester** 

Session 2021-22



**Emerging Domain in Electronics Engineering (KEC-101T)** Course Outcome CO Number To Define [L1] the various terminologies of semiconductor devices, CO<sub>1</sub> communication system, Boolean algebra and number system. CO<sub>2</sub> To Discuss [L2] the working of different semiconductor communication technologies and logic gates. CO<sub>3</sub> To Apply [L3] the concepts of semiconductor devices to solve the various electronics devices. To Analyze [L4] the various semiconductor devices, communication CO<sub>4</sub> technologies and Boolean Algebra reduction methods.

T	Sime: 1.5 Hrs. M. M.	15	
Q1. Attempt all questions:  a) Define Depletion layer.		(1X3 = 3 Marks) CO1	
b)	Write down in brief about n-type and p-type semiconductors.	COI	
c )	Define PIV.	COI	
Q2. Attempt all questions: Section B (2X4 = 8 Marks)			
a i)	Classify the materials with the help of energy band.	CO2	
ii)	Or Explain the effect of temperature on V-I characteristics of semiconductor diode.	CO2	
bi)	Explain current flow mechanism in a p-n junction diode under forward bias and reverse bias condition.	e CO2	
ii)	Or Explain the working of Full Wave Bridge Rectifier. Find the values of PIV for each diode	CO2	
c i)	Calculate the value of $V_0$ and I for the network of Fig. 2.1.	CO3	



- A full wave centre tapped rectifier with 220V, 50 Hz sinusoidal input and turns ratio of CO3
   5:1 has a load resistance of 500Ω. Determine:
  - (a) RMS value of output voltage
  - (b) DC output voltage
  - (c) Rectifier Efficiency
  - (d) Ripple factor
- d i) Differentiate between Half Wave Rectifier and Full Wave Rectifier.

CO<sub>2</sub>

)r

ii) Differentiate between Ideal Diode and Practical Diode.

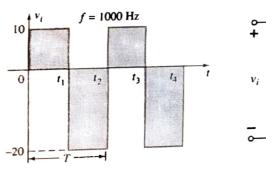
CO<sub>2</sub>

## Section C

(4X1 = 4 Marks)

Q3
i) Determine V<sub>o</sub> for the following network with the input shown (for ideal diode)

CO4



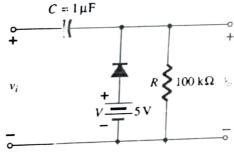
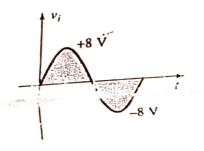


Fig. 3.1

CO4

ii) Determine  $V_0$  for the network of Fig. 3.2 for the input shown.



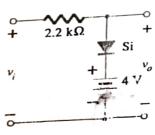


Fig. 3.2