

Project Report Title

Course Name: ESS 102, Digital Design Student Names: Vriddhi Agrawal, Arismita Mukherjee, Kavya Gupta Student ID: IMT2023611, IMT2023585, IMT2023016 Group ID: 09

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1 Combinational Circuit: 2 Bit Multiplier

1.1 Description

A 2-bit binary multiplier is used to multiply two 2-bit binary numbers and provide the result as output. The binary numbers used in the binary multiplication are called the multiplicand and the multiplier. On multiplying the two 2-bit binary numbers A1A0 and B1B0, we obtain a binary output P3P2P1P0.

1.2 Implementation

For bit by bit multiplication, we use the following rules: 0X0=0, 0X1=0, 1X0=0, 1X1=1

X		A1 B1	A0 B0	
	B1A1	B0A1 B1A0	B0A0 x	
P3	P2	P1	P0	

Boolean expressions:

P3 = A1*A0*B1*B0

P2 = A1*B1*(A0*B0)

P1 = (A1*B0) xor (A0*B1)

P0 = A0*B0

Inputs (A1 A0)	Inputs (B1 B0)	Outputs (P3 P2 P1 P0)
00	00	0000
00	01	0000
00	10	0000
00	11	0000
01	00	0000
01	01	0001
01	10	0010
01	11	0011
10	00	0000
10	01	0010
10	10	0100
10	11	0110
11	00	0000
11	01	0011
11	10	0110
11	11	1001

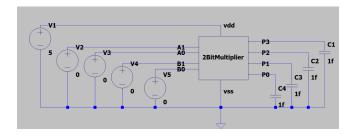


Figure 1: Testbench



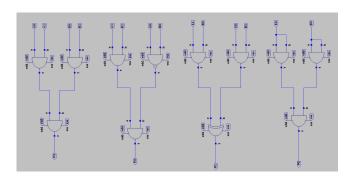


Figure 2: Subcircuit

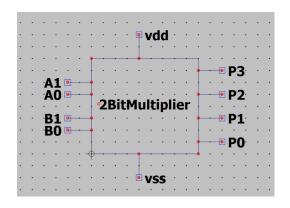


Figure 3: Symbol

1.3 Results

		A1 (I/P) (V)	A0 (I/P) (V)	B1 (I/P) (V)	B0 (I/P) (V)	P3 (O/P)	P2 (O/P)	P1 (O/P)	P0 (O/P)
		0	0	0	0	24.5 nV	24.5 nV	98.3 nV	24.5 nV
		0	0	0	5	24.5 nV	24.5 nV	98.3 nV	24.5 nV
		0	0	5	0	24.5 nV	24.5 nV	98.3 nV	24.5 nV
Lo	ogic-1 is represented by $5V$ and logic-0 is	0	0	5	5	24.5 nV	24.5 nV	98.3 nV	24.5 nV
re	presented by 0V. The results obtained on	0	5	0	0	24.5 nV	24.5 nV	98.3 nV	24.5 nV
pa	assing different input voltages in the test-	0	5	0	5	24.5 nV	24.5 nV	98.3 nV	5 V
be	ench circuit are as follows.	0	5	5	0	24.5 nV	24.5 nV	5 V	24.5 nV
24	.5 nV and 98.3 nV are negligible in com-	0	5	5	5	24.5 nV	24.5 nV	5 V	5 V
pa	rison to 5V and thus can be approximated	5	0	0	0	24.5 nV	24.5 nV	98.3 nV	24.5 nV
to	0 V. Hence, the outputs generated by the	5	0	0	5	24.5 nV	24.5 nV	5 V	24.5 nV
	stbench match the values in the truth table	5	0	5	0	24.5 nV	5 V	98.3 nV	24.5 nV
of	the 2-bit multiplier.	5	0	5	5	24.5 nV	5 V	5V	24.5 nV
		5	5	0	0	24.5 nV	24.5 nV	98.3 nV	24.5 nV
		5	5	0	5	24.5 nV	24.5 nV	5 V	5 V
			5	5	0	24.5 nV	5 V	5 V	24.5 nV
		5	5	5	5	5 V	24 5 nV	24.5 nV	5 V

2 Sequential Circuit: E.g., Mod-3 Up Counter

2.1 Description

A counter counts by one with each clock pulse. Counters which increase states when activated by a clock are said to operate in a "count-up" mode. MOD counters are based on the number of states that the counter will count before returning back to its original value.

2.2 Implementation

For example, a 2-bit counter that counts from 00 to 10 in binary, that is 0 to 2 in decimal, has a modulus value of 3 ($00 \rightarrow 01 \rightarrow 10$, and return back to 00) so would therefore be called mod-3 counter. It has taken three clock pulses to get from 00 to 10. So, a Mod-3 counter will require 2 flip-flops connected together to count a single data bit while providing 3 different output states.

2.3 Results



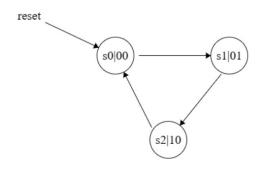


Figure 4: State transition Diagram

C	PS	NS
1	So	SI
1	51	\$2
,	52	So

PS Y

SO 00

SI 01

S2 10

Figure 5: State transition table (next state)

Figure 6: State trasition table (next state)

State encodings So=00	C	PS :	NS	 PS -	y
51 = 01		Q1Q0	アラウ	RIRO	YIYO
S2 = 10	1	00	01	00	00
	_ 1	01	10	01	01
	1.	10	00	10	10

Figure 7: Truth table with state encodings

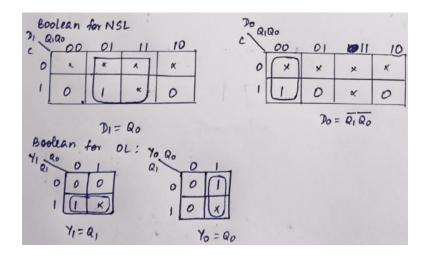


Figure 8: K-Maps



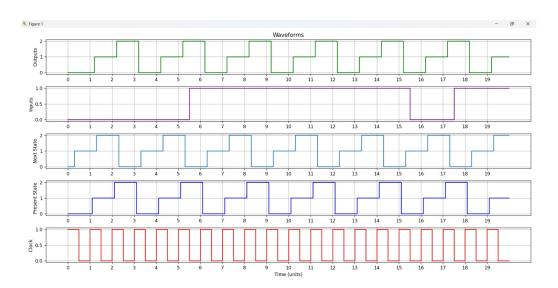


Figure 9: Waveforms

```
PS C:\Users\kavya\OneDrive\Desktop> python main.py
Time: 0.5, State: 000, Output: 000
Time: 1.5, State: 001, Output: 001
Time: 2.5, State: 010, Output: 010
Time: 3.5, State: 000, Output: 000
Time: 4.5, State: 001, Output: 001
Time: 5.5, State: 010, Output: 010
Time: 6.5, State: 000, Output: 000
Time: 7.5, State: 001, Output: 001
Time: 8.5, State: 010, Output: 010
Time: 9.5, State: 000, Output: 000
Time: 10.5, State: 001, Output: 001
Time: 11.5, State: 010, Output: 010
Time: 12.5, State: 000, Output: 000
Time: 13.5, State: 001, Output: 001
Time: 14.5, State: 010, Output: 010
Time: 15.5, State: 000, Output: 000
Time: 16.5, State: 001, Output: 001
Time: 17.5, State: 010, Output: 010
Time: 18.5, State: 000, Output: 000
Time: 19.5, State: 001, Output: 001
```

Figure 10: Output