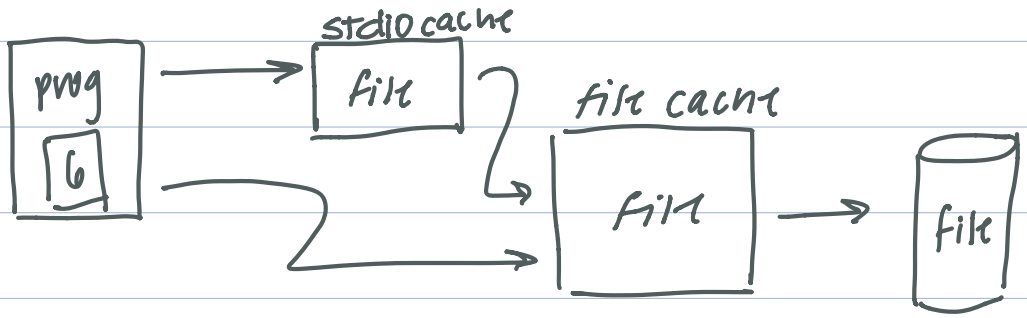
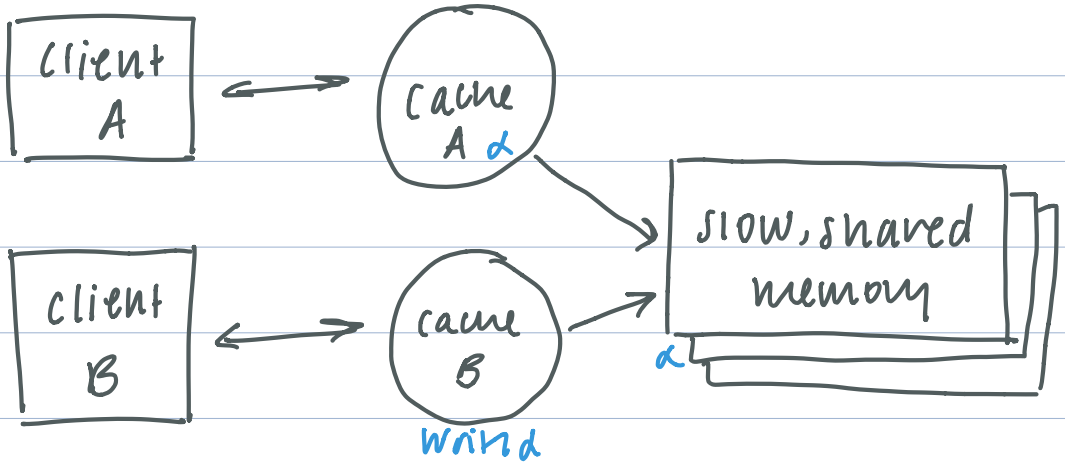
CS61 Lecture 19: Last Storage

November 5, 2019



Intersection of Reads and Writes



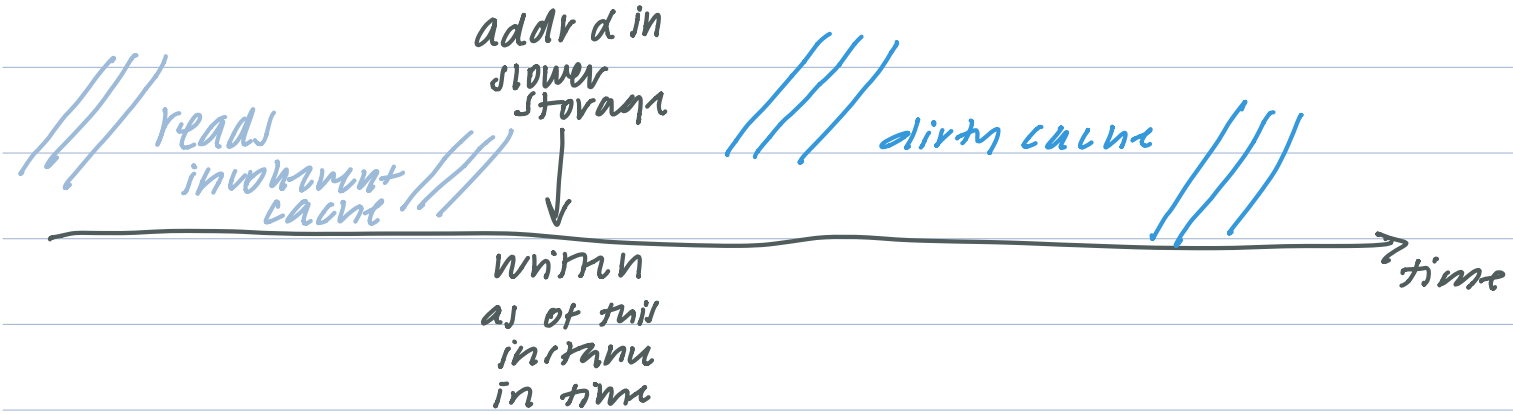
cache coherence = memory system is coherent if a read of data at addr α returns the most recently written value to addr α

different fd = different memory in file cache

- two caches, one cache (stdio) only worries about performance and not accuracy

- close flushes data out to file
- hardware caches should be coherent

Another Cache



dirty slot = slot in cache that contains data that is newer than slower storage

clean slot = slot in cache contains data that is no newer than slow storage

could be incoherent

← standard io cache

Writeback caches:

- write eliminations
- slower storage only sees last write
- can get dirty slots

Write through caches:

- IO/t optimization
- every write goes to slow-storage
- no dirty slots, makes coherence easier

Write back ⟶ write through

O_SYNC flag

Atomicity

an operation is atomic if it appears to occur in an indivisible instant in time

↳ when you start, you finish and nothing else happens inbetween

x86 call instruction: updates %rip, %rsp, old %rip on stack