Compsci 6/ 1-11/11/2 Pata Representation September 3,2019
problem set 1 is out, due in 2 weeks
late policy: 144 late hours (6 days)
memory address envoding for 297 235,
tist access
Zsi. array 1 17 1003 4
data
RAM: any byte, any access in law, any order about the access in random order rather than
stavinhaly
test insert 0: linked list
gsi. array 0,1,2
1ist * [2]/
address encoding for 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
address otnext
instrting in order is much slower man inserting from a
reversed list (for alinual list).

Vertors are sequentially ordered in memory, so they need less space in memory and it has a buge speed advantage. >1,000,000 linked list becomes faster. add 4 8 bj dymp program	test insert 1: rector
>1,000,000 linked list becomes faster. add	Verrory are sequentially ordered in memory, so they need
>1,000,000 linked list becomes faster. add	ILIS space in memory and it has a luge speed advantage.
	>1,000,000 linked list becomes faster.
* 9 bj dvmp program	add
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