ABV - Indian Institute of Information Technology, Gwalior

Department of Computer Science and Engineering

Assignment : ITIT-2103 "Computer Organization and Architecture"

Faculty : Dr. Deepak Kumar Dewangan

Note: *All the questions of the assignment should be solved in hard copy/hand written and the soft copy (scanned copy of hand written solution) of the assignment is to be submitted* ***strictly*** *on or before 11.11.2024. The submission link will be shared later.*

Q1. Given a digital circuit consisting of several flip-flops and combinational logic blocks, manually perform timing analysis, including setup and hold time checks, and calculate the maximum clock frequency.

Q2. Given a detailed microinstruction set for a hypothetical CPU, manually derive the correct sequence of microoperations for executing a complex assembly instruction (e.g., indexed array access).

Q3. Ultimately, the storage systems design requires consideration of usage scenarios as well as disk parameters. Different situations require different metrics. Explore difference in how storage systems should be evaluated by answering the question about the following applications: (a) Online NASA Satellite Database and (b) Video Gaming Systems.

Q4. Design a memory hierarchy with four levels (registers, cache, RAM, and virtual memory). Then, analyze the performance of memory accesses under different workloads. Also, discuss how you would implement memory protection.

Q5. Design a custom 16-bit processor with a unique instruction set architecture (ISA). Include specific details about registers, ALU operations, and control signals. Then, analyze its performance on a given workload and compare it to a traditional MIPS architecture.

Q6. Discuss cache write policies along with the "dirty blocks".

Q7. How does associative memory differs from regular memory? Which is more expensive and why?

Q8. Look up a specific vendor's specifications for memory, and report the memory access time, cache access time and cache hit rate.

Q9. Consider a system that has multiple processors where each processor has its own cache, but main memory is shared among all processors. What problems are caused if a processor has a copy of memory block **A** in its cache and a second processor, also having a copy of **A** in its cache, then updates main memory block **A**? Can you think of a way (perhaps more than one) of preventing this situation, or lessening its effects?

10. Discuss Moore's Law.

*****End of the Assignment*****