DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

FINAL PROJECT USER MANUAL

PROJECT PROPOSAL FOR CIS 634: OBJECT ORIENTED SOFTWARE ENGINEERING

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- **Objective of user manual:**
  We are designing the simulation model of SRAM memory using different hardware design tools. These EDA tools are complicated to use so this user guide will enable us to understand about the usage of software without facing difficulty by providing steps/ procedure to follow.

- **Static random-access memory:**
  Static RAM (SRAM) is a type of RAM which stores data till the power of the computer system is switched on. SRAM uses a number of transistors to store a single bit of digital information.

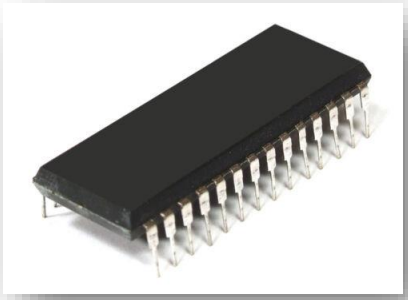


Fig: 1

- **Scope:**
  Every device consists of integrated circuits which are made up of semiconductors. Each device has its functions and certain applications to perform which are basically automated. The functions are fed into the devices using internal storage memories. Memory is used in any tiny device to huge equipment that has a CPU which is based on semiconductor technology. The demand for semiconductor memory is very high as the processors and computers are getting complex in nature.

- **Software tools used:**
  We are using Modelsim to design, verify the design using test bench, compile and simulate the code.
  We are using Vivado to simulate behavioral analysis of the design and extract hardware structure i.e., converting code into gate level netlist. So, RTL analysis (register transfer level) of the design is done.

1. ModelSim:

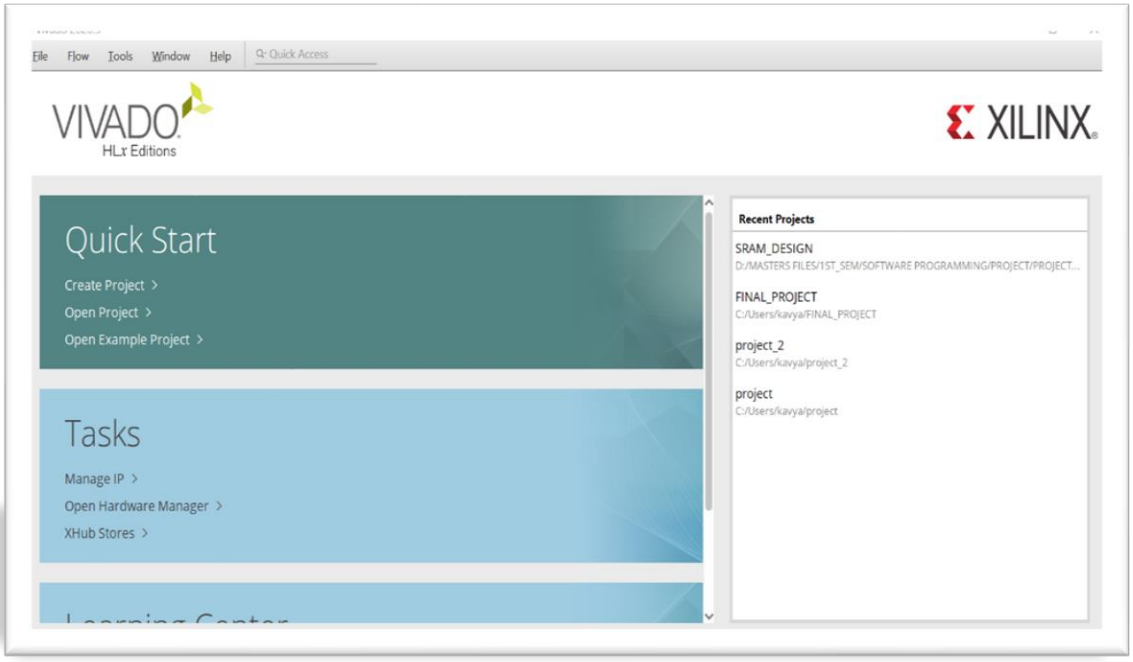
- It is EDA tool developed by mentor graphics.
- It is used for simulation of hardware description languages such as VHDL, Verilog and systemC.
- It simulates behavioral, RTL, and gate-level code.

2. VIVADO:

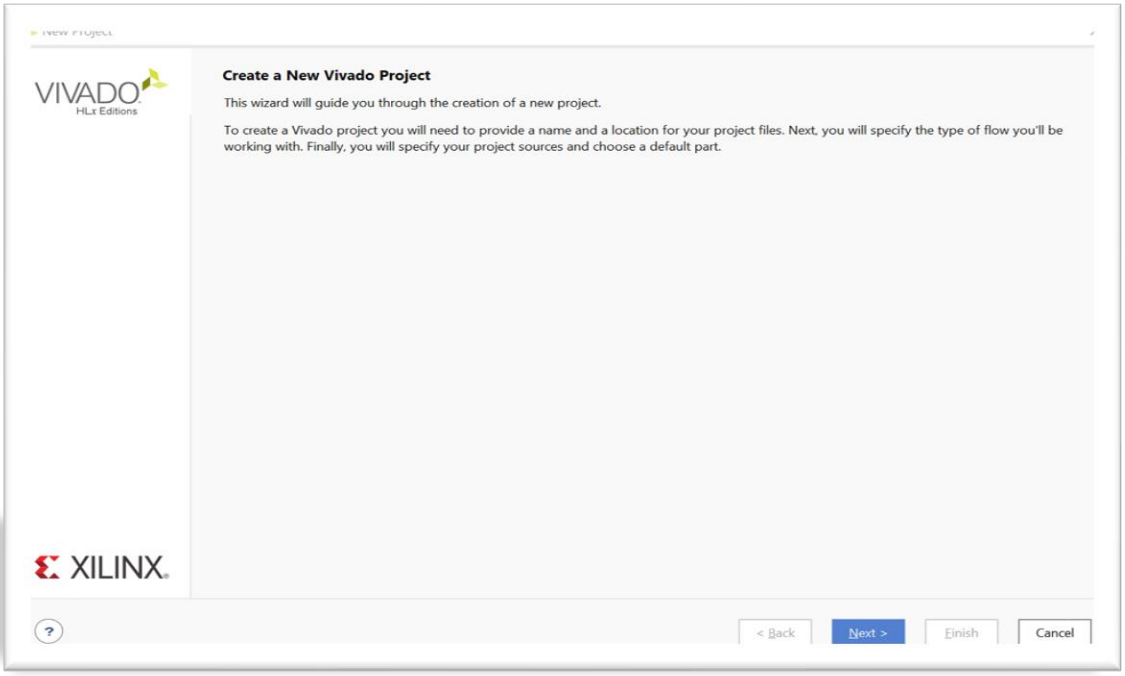
- Vivado is a design tool.
- It is developed by Xilinx.
- It is used for synthesis and analysis of hardware description language (HDL) design.

➢ **User guide to VIVADO:**

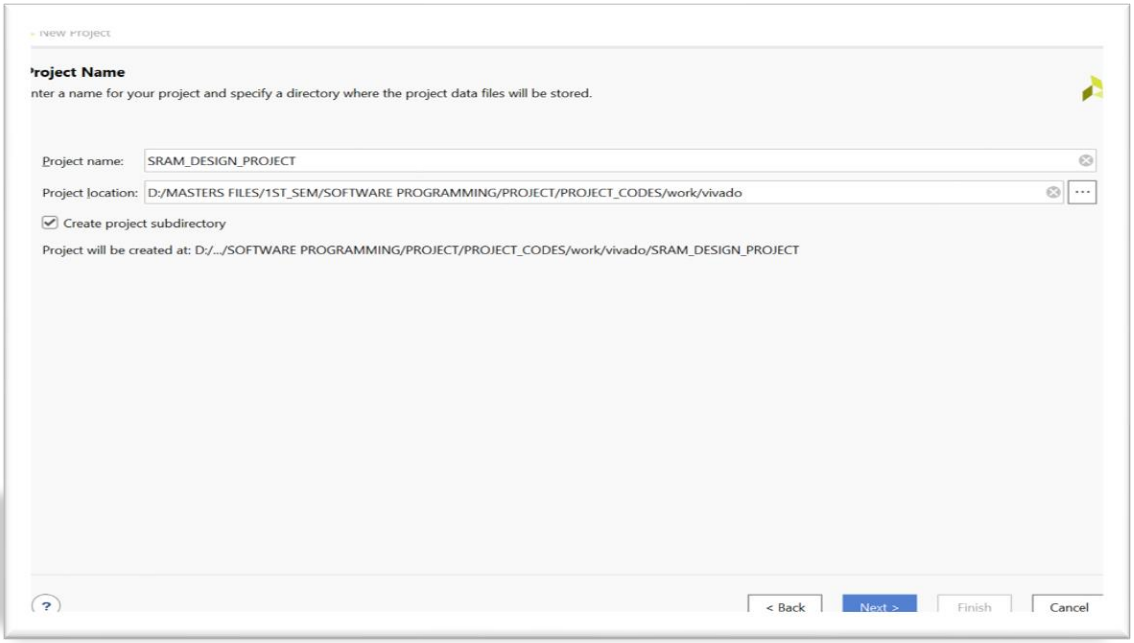
1. Open the vivado software.
    - Click on create project to create new project and give next.
    - Click on open project if the project already exists and give next.



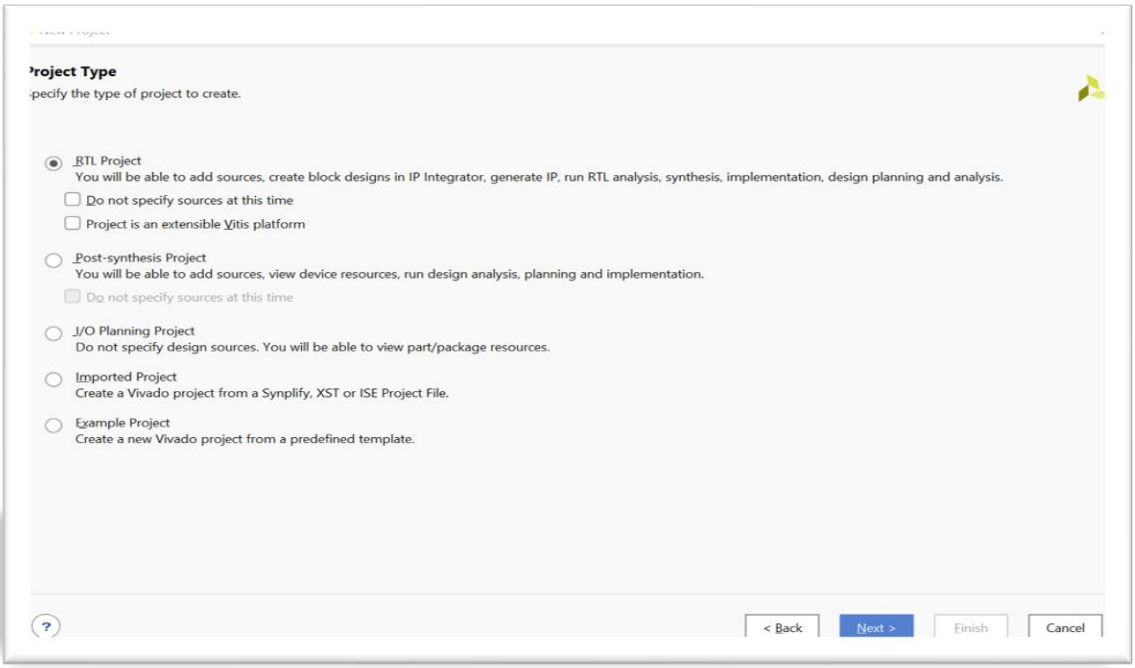
2. Give next at this window.



3. Create project name and choose directory and give next.

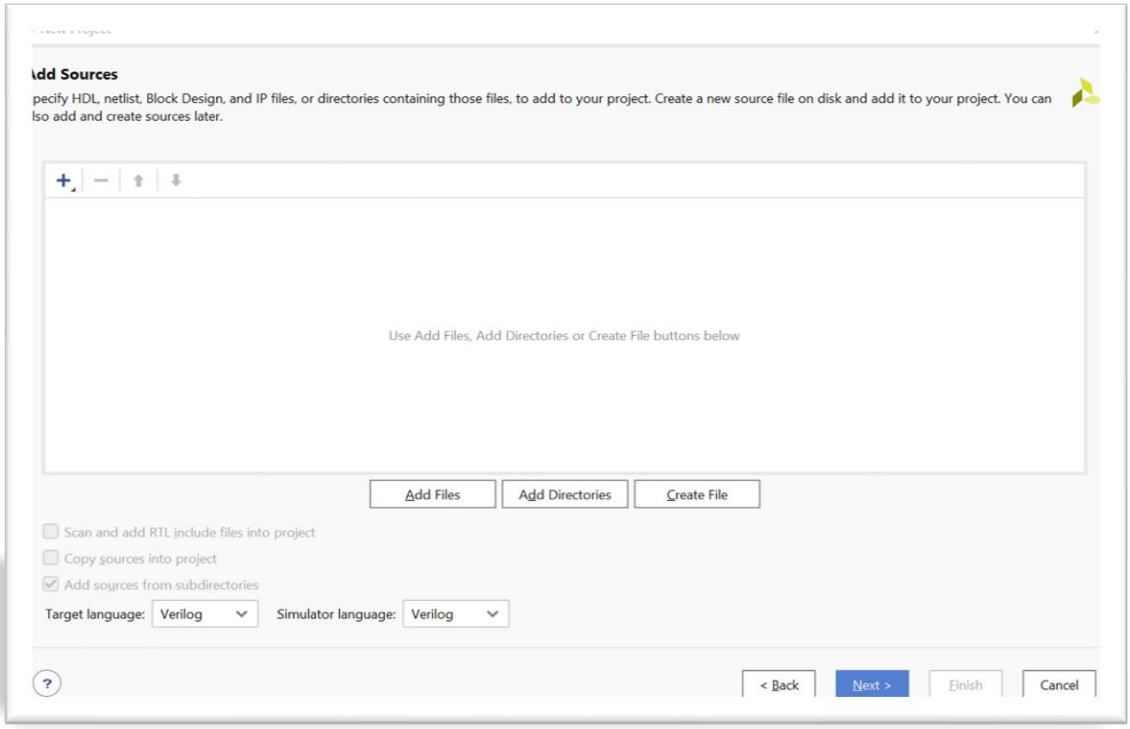


4. Select project type at this window.
    - We are selecting RTL project.
    - We can select other options if necessary but for our project we are not implementing design on board so other options are not required.
    - Give next

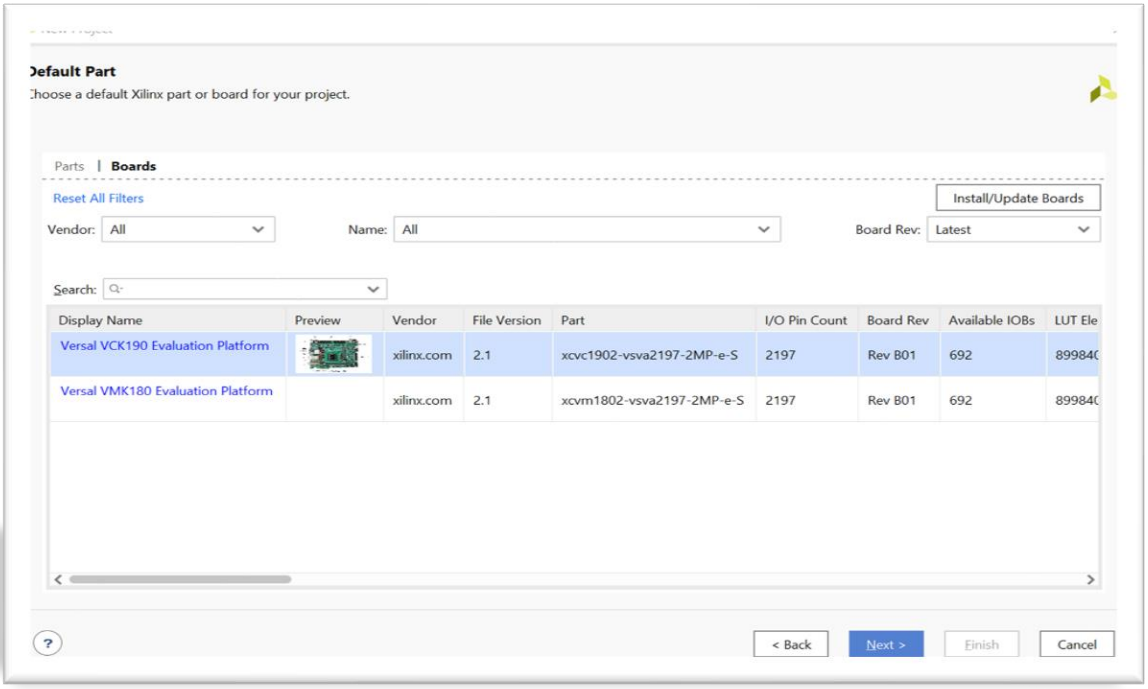


5. We can add source of code at this stage or create source code.

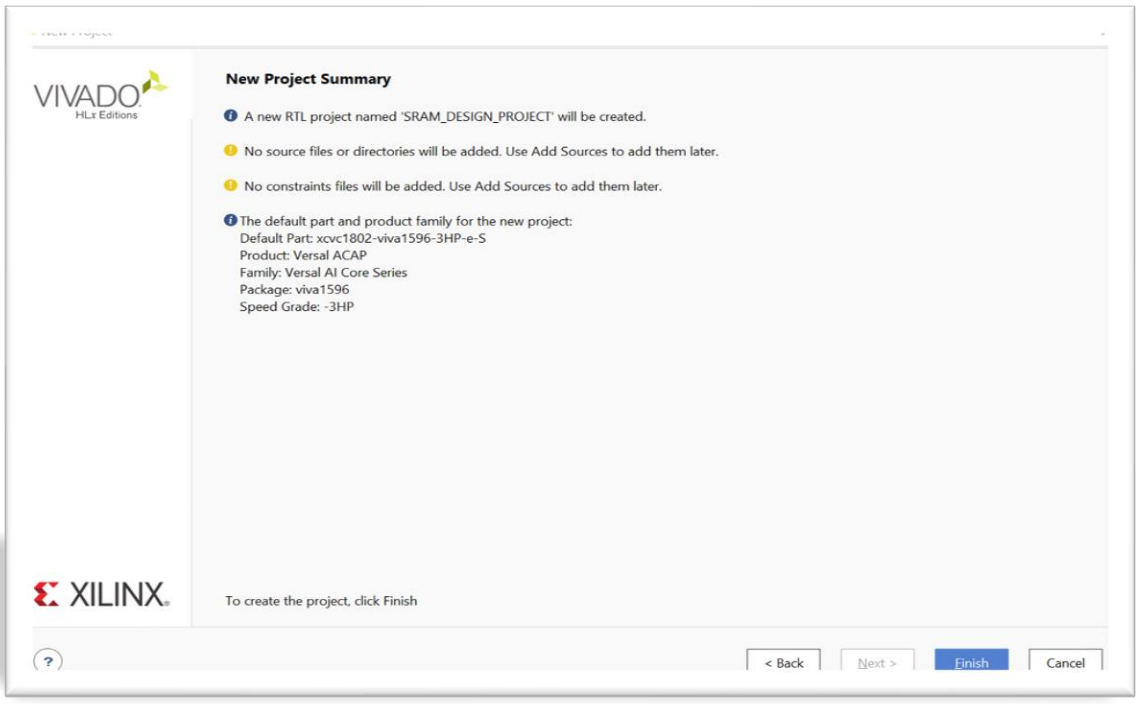
- Target language should be selected as Verilog as we are using Verilog coding for designing the system.
- Simulator type should be given as Verilog as well.
- We have other options like VHDL and systemC.
- Give next



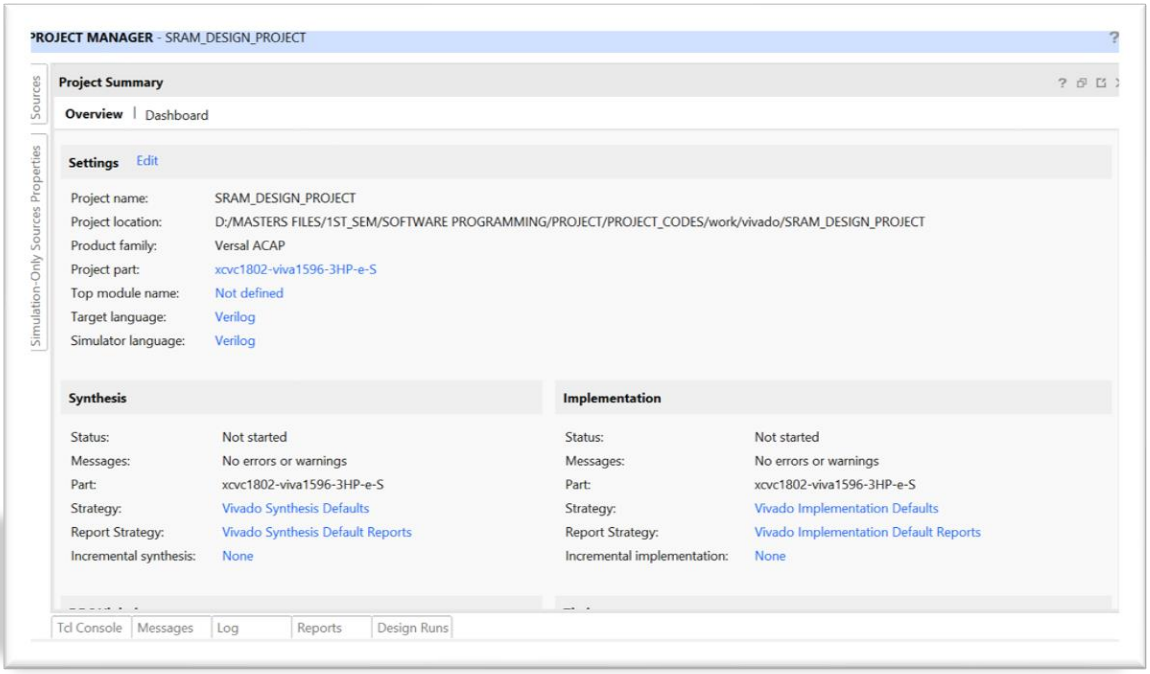
6. Select the required board and give next.



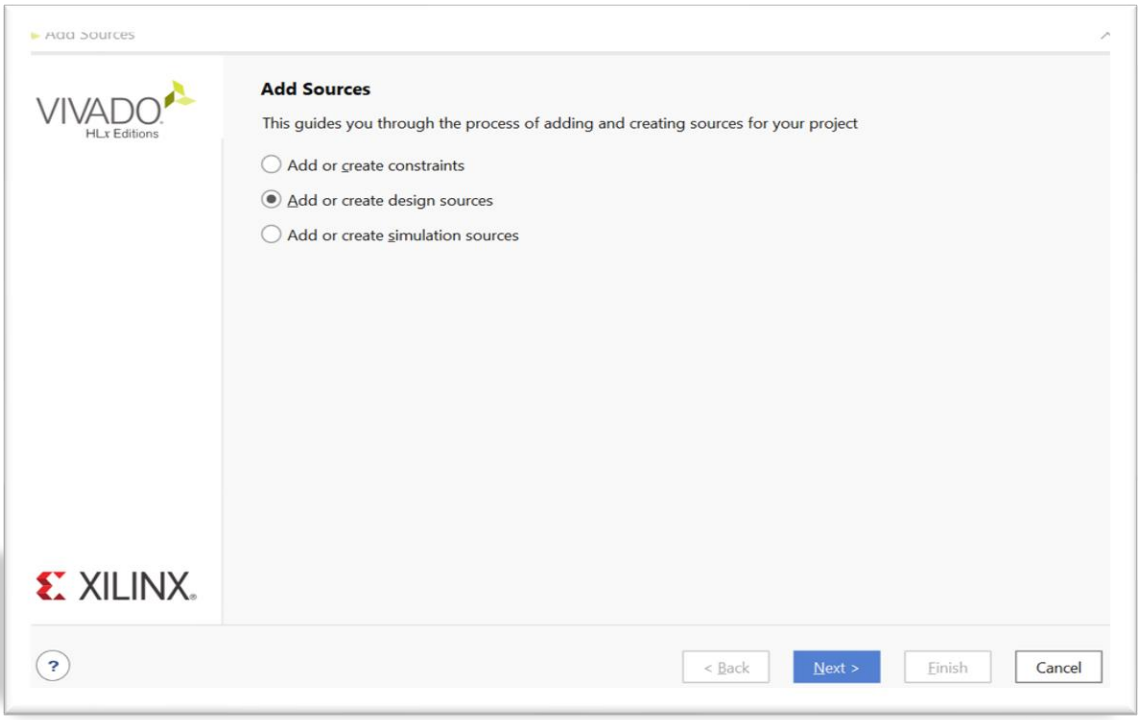
7. We can see project summary i.e., product, family, package, speed grade.
    - Give finish.



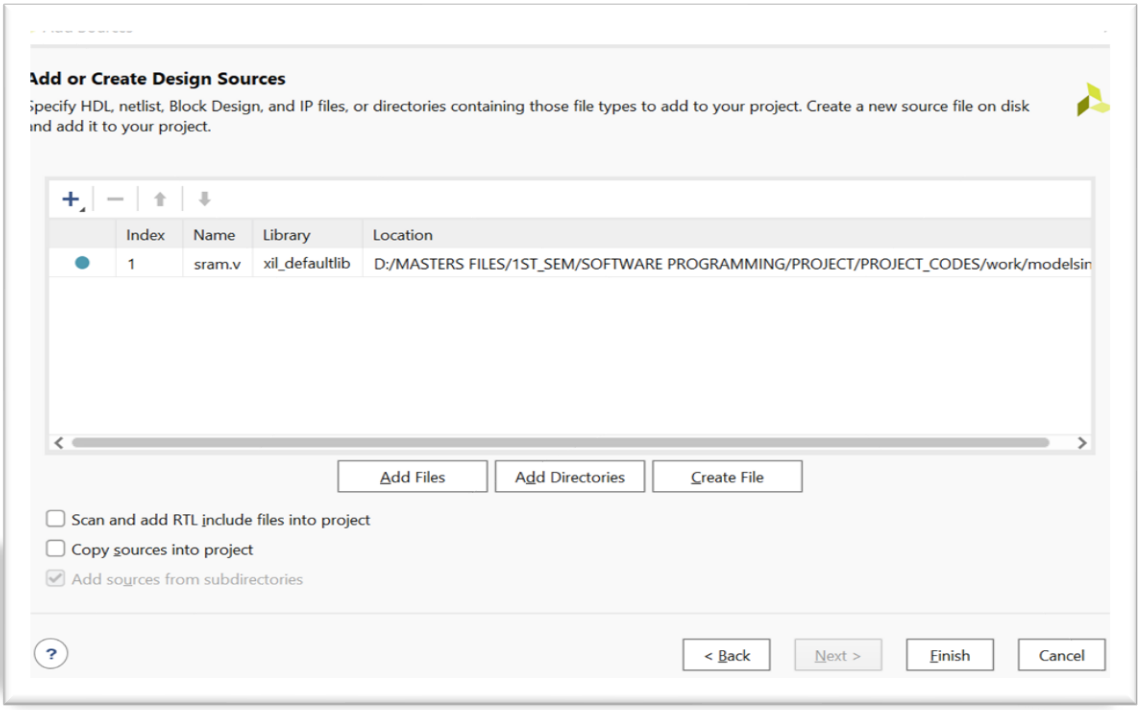
8. Our project will be created. We can see project summary here as well with synthesis and implementation part.



9. We can add or create code source after the project is created.



10. At this window we need to give finish and sources will be created or added to code the design.



11. This is how the window after project is created looks like.
    - We can do behavioral check, RTL analysis can get results.