CSE306: Computer Architecture Sessional

Assignment 1: 4-bit ALU Simulation

Submitted By:

Group No: 05

Sub-Section: A2

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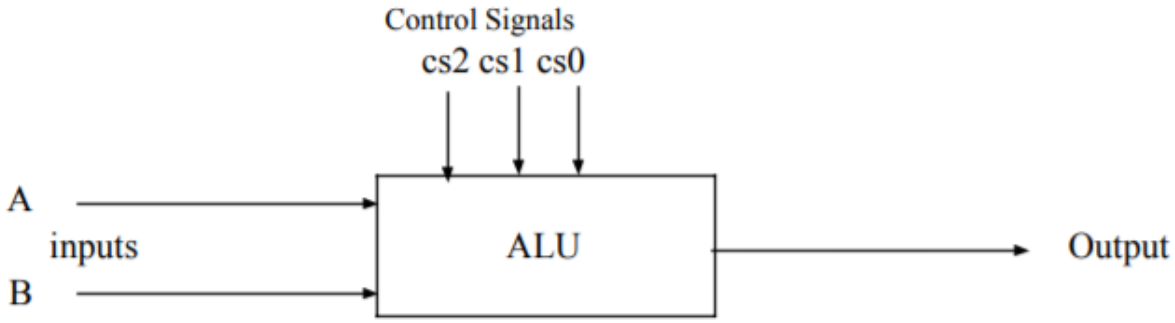
Introduction:

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. The ALU has a number of selection lines to select a particular operation.



Problem Specification:

Here we have two 4 bit inputs and 3 bits to control the operations. We used the control bits to select operations and input carry.

Here we also implemented a status register. The status registers are carry(c), sign(s), overflow(v) and zero(z) flags which indicates

a. Carry: Carry(c) is 1 if output carry is 1 and c is 0 if output carry is 0.

b. Sign: Sign flag (s) is 1 if the leftmost bit is 1 which means the output is negative and s is 0 when answer is positive.

c. Overflow: Overflow flag(v) is 1 if any overflow occurs and 0 if there is no overflow.

d. Zero: Zero flag (z) is 1 if the output value is all zero and z is 0 otherwise.

CS2	CS1	CS0	Function
0	0	0	Subtract with borrow
0	1	0	Transfer A
1	0	0	Subtract
1	1	0	Increment A
X	0	1	Or
X	1	1	And

Truth Table:

CS2	CS1	CS0	Xi	Yi	Zi	Function
0	0	0	A	B’	0	A + B’
0	1	0	A	0	0	A
1	0	0	A	B’	1	A + B’ + 1
1	1	0	A	0	1	A + 1
X	0	1	A + B	0	0	A + B
X	1	1	A + B’	B’	0	A . B

Let,
a = CS1’. CS0
b = CS1 . CS0

Then the inputs in the ADDERS are the following:

Xi = Ai + Bi.a + Bi’.b

Yi = Bi’ (CS1 ⊙ CS0)

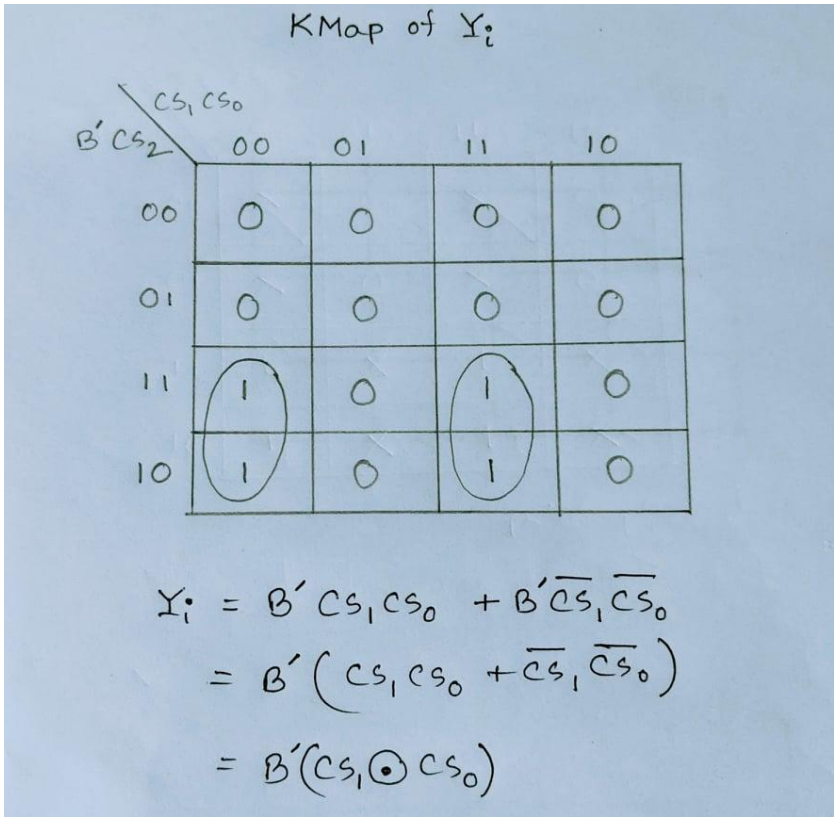
Zi = CS2 . CS0’

Xi:

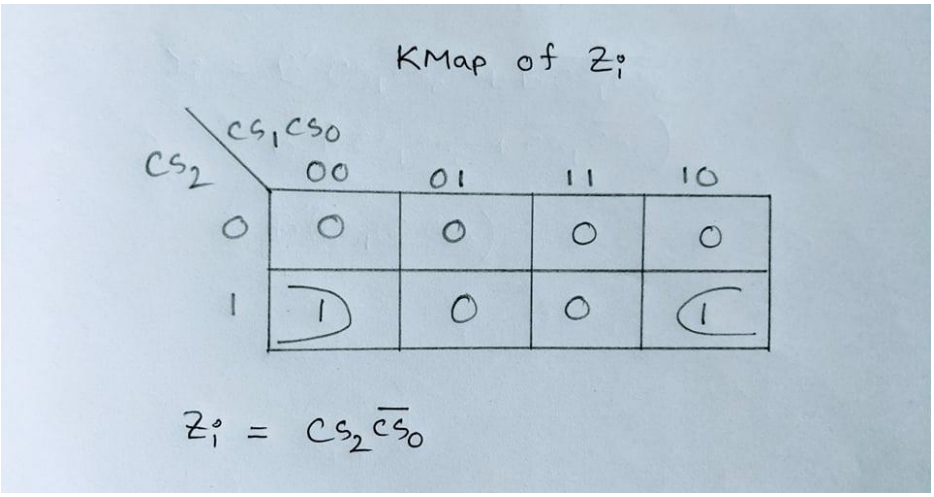
Xi = Ai.a'.b' + (A+B).a + (A+B').b

= Ai + Bi.a + Bi'.b

KMap of Yi:



KMap of Zi:



IC used with count:

IC	Count
7408 (AND)	5
74135 (XOR/XNOR)	1
7404 (NOT)	1
7432 (OR)	2
7433 (NOR)	1
7480 (FULL ADDER)	1

Block Diagram:

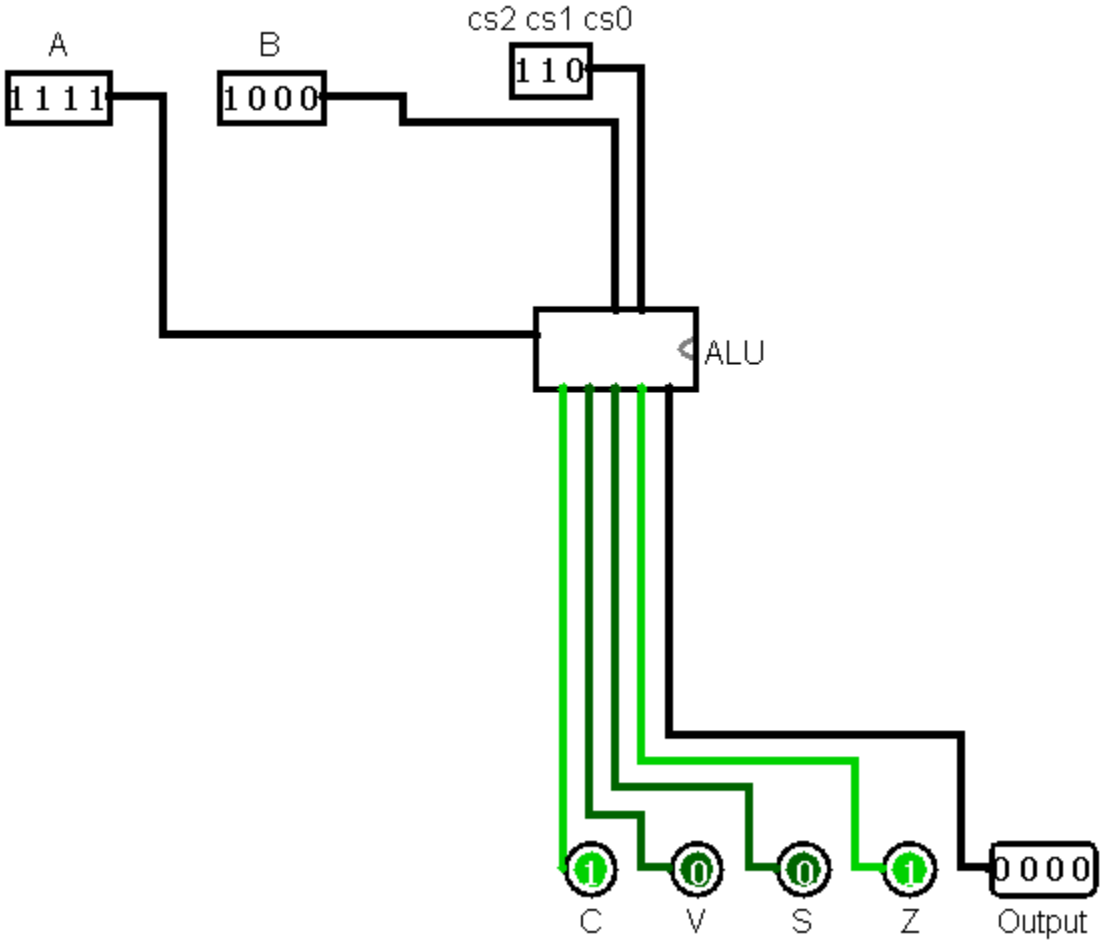


Figure 1: Block Diagram

Circuit Diagram:

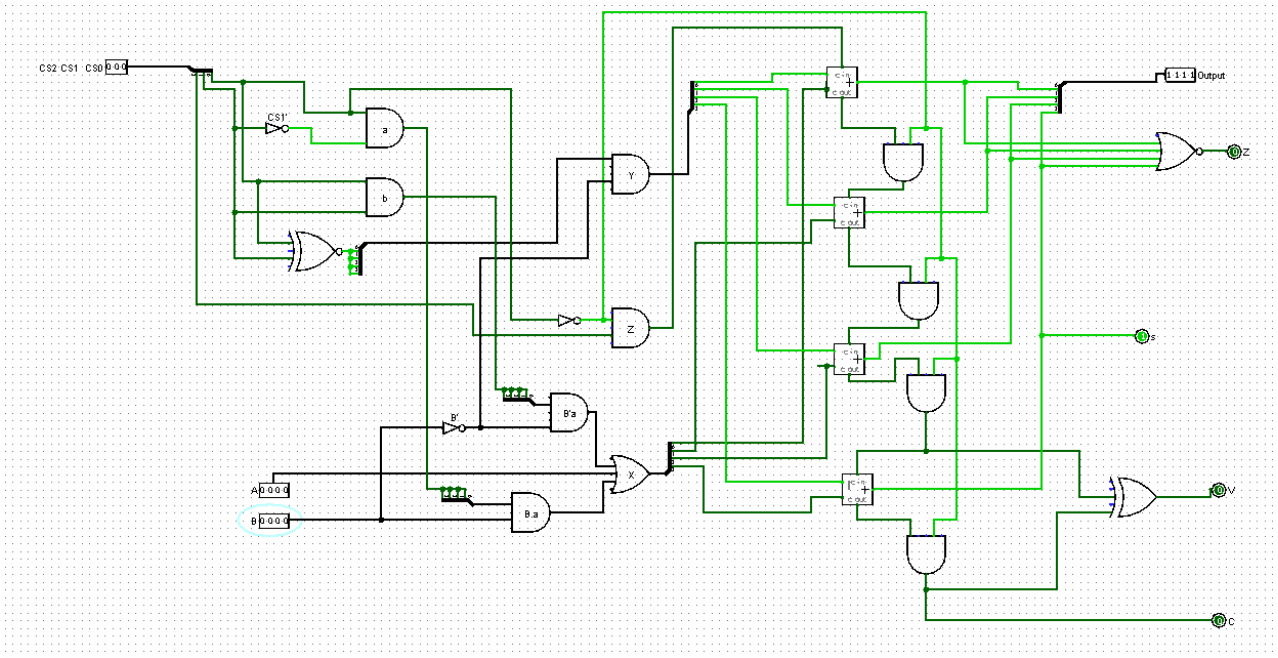


Figure 2: Circuit Diagram

Simulator used along with the version number:

Logisim 2.7.1

Discussion:

In this assignment, we designed an ALU (Arithmetic Logic Unit) which could do some basic operations. For this purpose we used basic gates (AND, OR, NOT, NOR) and universal gates(XOR, XNOR). The inputs in ALU are two 4 bit binary numbers A and B. CS2, CS1 and CS0 are control signals. First four operations are arithmetic and the last two operations are logical operations. Another important part of our design was the status flags. Here CS0 is used as a mode selector in our case (arithmetic/logical). We used the known technique of designing arithmetic units first and incorporating the logic unit. While designing, we put emphasis on minimizing the number of ICs, yet keeping it simple. We asserted our design by testing various inputs and matching the corresponding outputs. On the simulator, alongside the full circuit, we made a block circuit so that all signals can be visualized easily. However, testing the outputs and completing the data table, we successfully finished our simulation.