

EXPERIMENT4 REPORT

BBM233 LOGIC DESIGN LAB

Name and Surname : Meltem Kaya
Student ID : 21827555
Due Date : 05/12/2020



HACETTEPE
University

Department of Computer
Engineering

—

Teaching Assistant
Selma Dilek

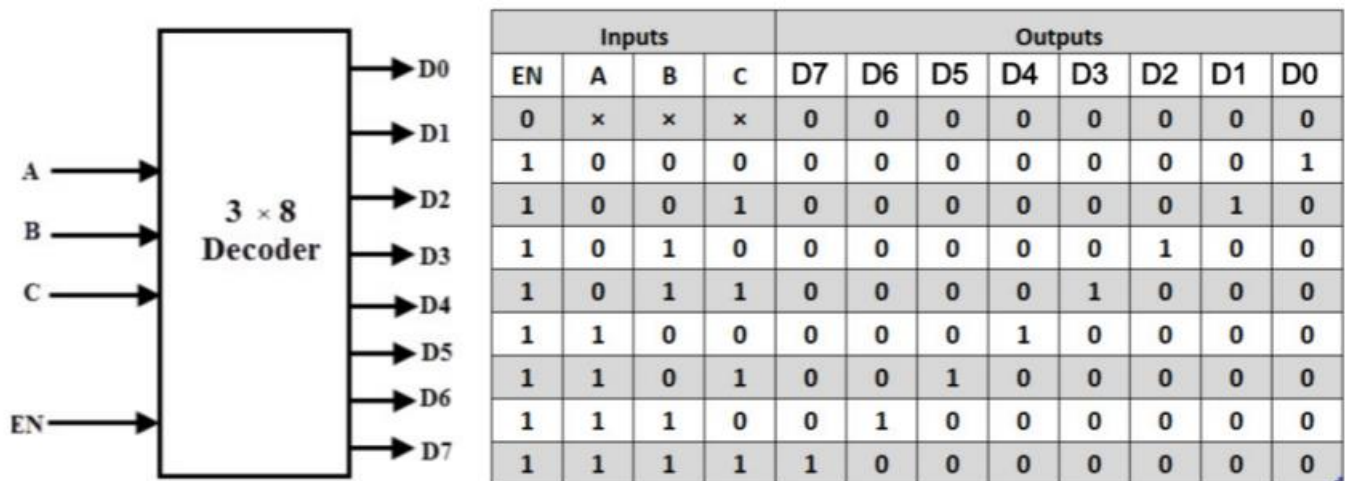
Table of Contents

1. PART0.....	3
1.1 Problem Statement.....	3
1.2 VERILOG CODE SOLUTIONS.....	4
1.2.1 decoder_3x8.v.....	4
1.2.2 decoder_3x8_tb.v.....	4
1.3 Obtained Waveform.....	5
2. PART1.....	6
2.1 Problem Statement.....	6
2.2 VERILOG CODE SOLUTIONS.....	7
2.2.1 decoder_4x16.v.....	7
2.2.2 decoder_4x16_tb.v.....	7
2.3 Obtained Waveform.....	8
3. Resources.....	8

PART 0

PROBLEM STATEMENT

Obtaining Boolean equations for the outputs D_0 through D_7 from the given truth table and implement the 3x8 decoder with enable input using behavioral design approach in Verilog HDL.



VERILOG CODE SOLUTIONS

decoder_3x8.v

```
1  `timescale 1ns / 1ps
2
3  module decoder_3x8(
4
5      input A,B,C,EN, // EN -> enable input
6      output [7:0] D
7
8  );
9      //assigning outputs D0 to D7
10
11      assign D[0] = EN & ~A & ~B & ~C;
12      assign D[1] = EN & ~A & ~B & C;
13      assign D[2] = EN & ~A & B & ~C;
14      assign D[3] = EN & ~A & B & C;
15      assign D[4] = EN & A & ~B & ~C;
16      assign D[5] = EN & A & ~B & C;
17      assign D[6] = EN & A & B & ~C;
18      assign D[7] = EN & A & B & C;
19  endmodule
20
```

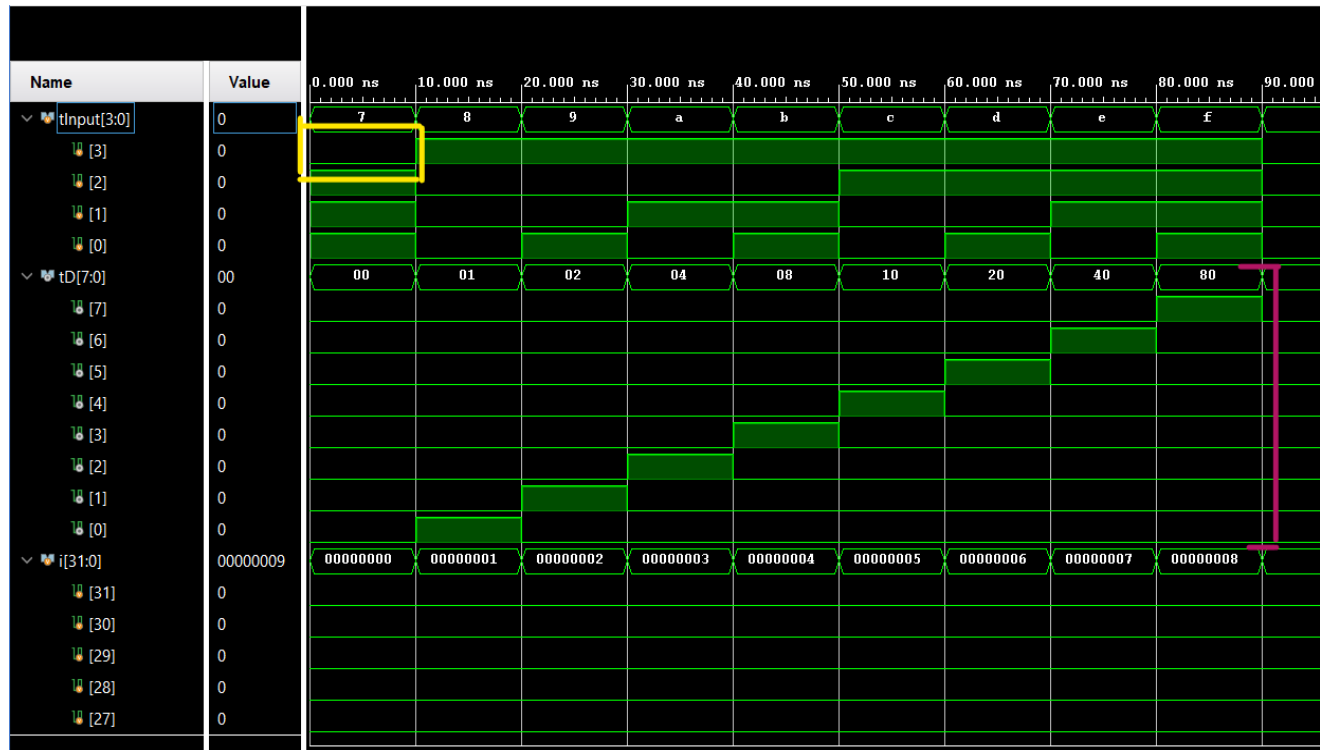
I declared 4 input and 8 output to implement a 3x8 decoder with enable input. Then, I assigned the values of each output from D0 to D7.

decoder_3x8_tb.v

```
1  `timescale 1ns / 1ps
2  `include "decoder_3x8.v"
3
4  module decoder_3x8_tb;
5
6      reg [3:0] tInput;
7      wire [7:0] tD;
8      integer i; //used for iterating for loop.
9      decoder_3x8 UUT(.EN(tInput[3]),.A(tInput[2]),.B(tInput[1]),.C(tInput[0]),.D(tD)); //explicit association
10
11  initial begin
12      tInput = 4'b0111;
13      for(i = 0; i<9; i = i+1) begin //iterates 10 times to produce output
14          #10 //delaying time before testing
15          tInput = tInput + 1; //increasing tInput
16      end
17  end
18  endmodule
19
```

For loop iterates 10 times to testing the decoder. Each time tInputs is increased by 1 to produce to expected results.

WAVEFORM OBTAINED FROM 3X8 DECODER

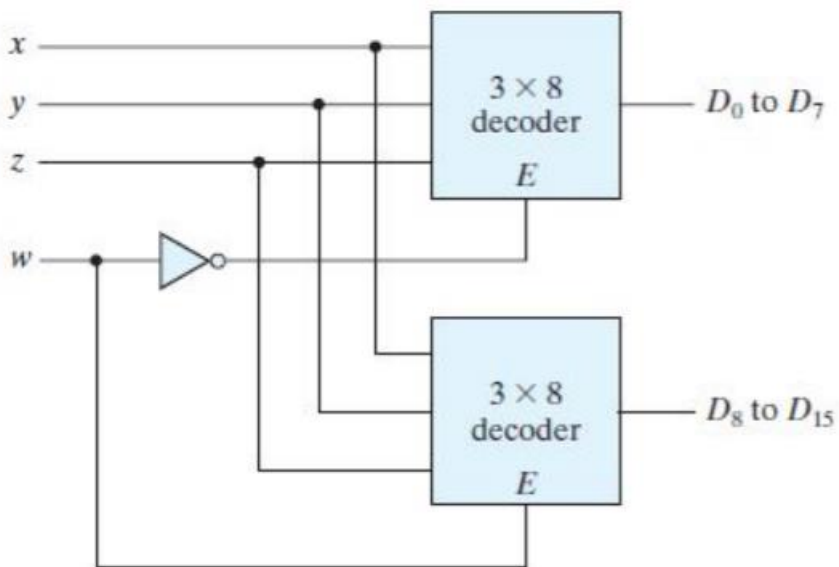


Pointed area with yellow color shows the output equals "0" while Enable Input equals zero. From 10.000 to 80.000ns, waves shows output of D_0 - D_7 which are equal to "1" while enable input equals 1. Also we can check the correctness of obtained waveform by looking the area pointed with pink. D_0 equals "0" within 0-10.000ns, the others are equal "1" within related time scales.

PART1

PROBLEM STATEMENT

Implementing a 4x16 decoder by using two 3x8 decoders with enable input. When $w = 0$, the top decoder is enabled and the other is disabled. When $w = 1$, the enable conditions are reversed.



VERILOG CODE SOLUTIONS

decoder 4x16.v

```
1  `timescale 1ns / 1ps
2  `include "decoder_3x8.v"
3
4  module decoder_4x16(
5      input [3:0] inputs,
6      output [15:0] outputs
7  );
8      //explicit association
9      decoder_3x8 Decoder1(.B(inputs[1]),.D(outputs[15:8]),.C(inputs[0]),.EN(inputs[3]),.A(inputs[2])); // D15-D8
10     decoder_3x8 Decoder2(.B(inputs[1]),.D(outputs[7:0]),.C(inputs[0]),.EN(~inputs[3]),.A(inputs[2])); // D7-D0
11
12
13
14
15     endmodule
16
```

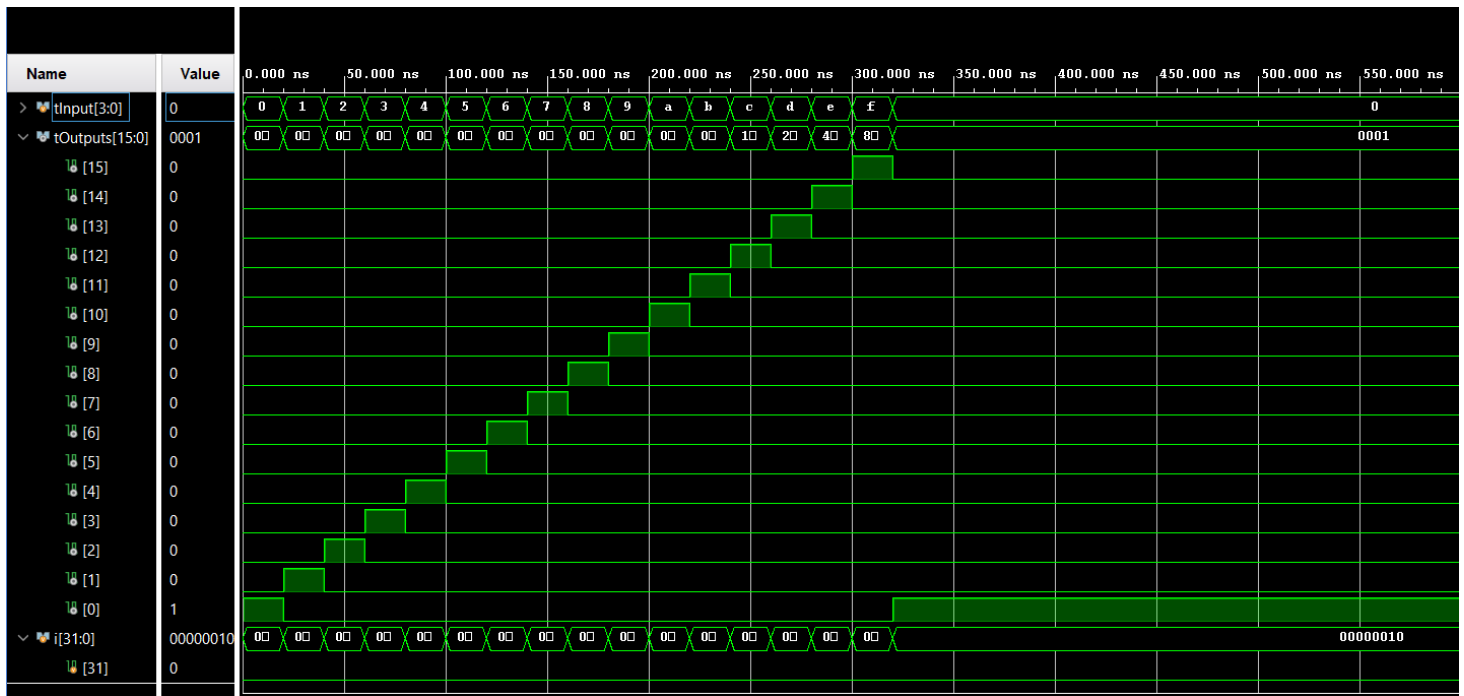
I used Decoder1 with enable input = 1, to declare $outputs_{15}$ - $outputs_8$ and Decoder2 with enable input = 0 to declare $outputs_7$ - $outputs_0$.

decoder 4x16 tb.v

```
1  `timescale 1ns / 1ps
2  `include "decoder_4x16.v"
3
4  module decoder_4x16_tb;
5      reg [3:0] tInput;
6      wire [15:0] tOutputs ;
7      integer i; //needed for iterating for loop
8
9      decoder_4x16 UUT(.outputs(tOutputs),.inputs(tInput));
10
11  initial begin
12      tInput = 4'b0; //initial input
13      for(i = 0;i <16;i = i+1) begin
14          #20
15          tInput = tInput +1; //increasing input by 1
16
17      end
18  end
19  endmodule
```

For loop iterates to test module by increasing input by 1.

WAVEFORM OBTAINED FROM 4X16 DECODER



Signals are easily seen like ladder. $outputs_{15}-outputs_0$ equal “1” within related time scales and there is no signal except $outputs_{15}-outputs_0$.

RESOURCES

BBM233 lecture videos

BBM233 lecture notes

TOBB ETU Computer Engineering lecture records

<https://www.youtube.com/watch?v=Vxvv->

[idOQiU&list=PL36uFMHhtMR5yAVILJw3GRXTh1BDOSB3f&index=8](https://www.youtube.com/watch?v=Vxvv-)

<https://www.youtube.com/watch?v=EDswcCwq014&list=PLvNq8wrSYGAU8Cf3n9rhL-GB4yMNO1-XC&index=4>

<https://www.youtube.com/watch?v=G76Bi0Pr2O4&list=PLvNq8wrSYGAU8Cf3n9rhL-GB4yMNO1-XC&index=6>

<https://www.youtube.com/watch?v=QfrNZQmqLhg>