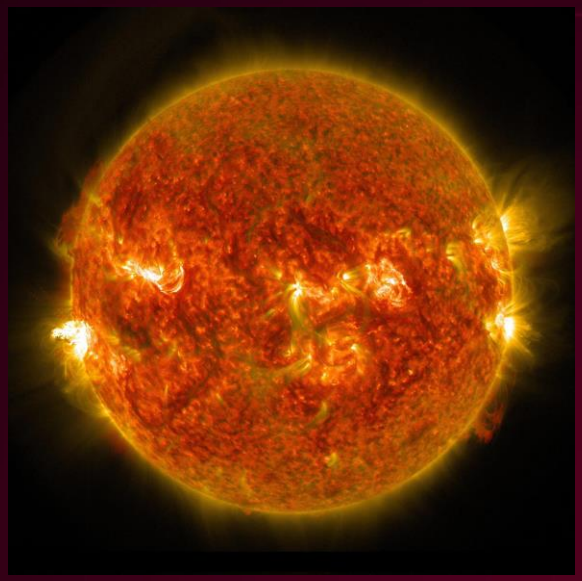


Dwight Look College of ENGINEERING
TEXAS A&M UNIVERSITY

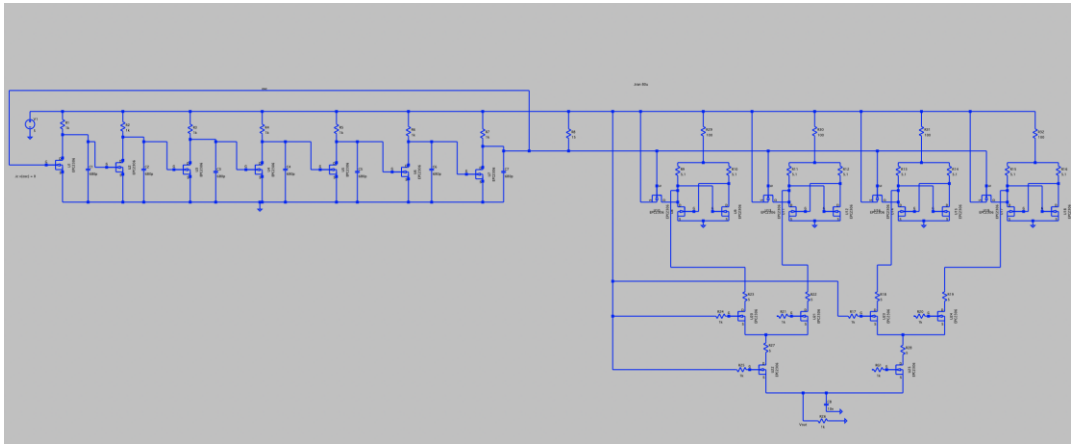
Team 1: Radiation Resilient Logic Circuit Study with WBG Devices Bi-Weekly Update 5

Nia Baireddy, Kaylee Choate, Nomar Lebron
Sponsor: Sandia National Laboratories
TA: Eric Robles

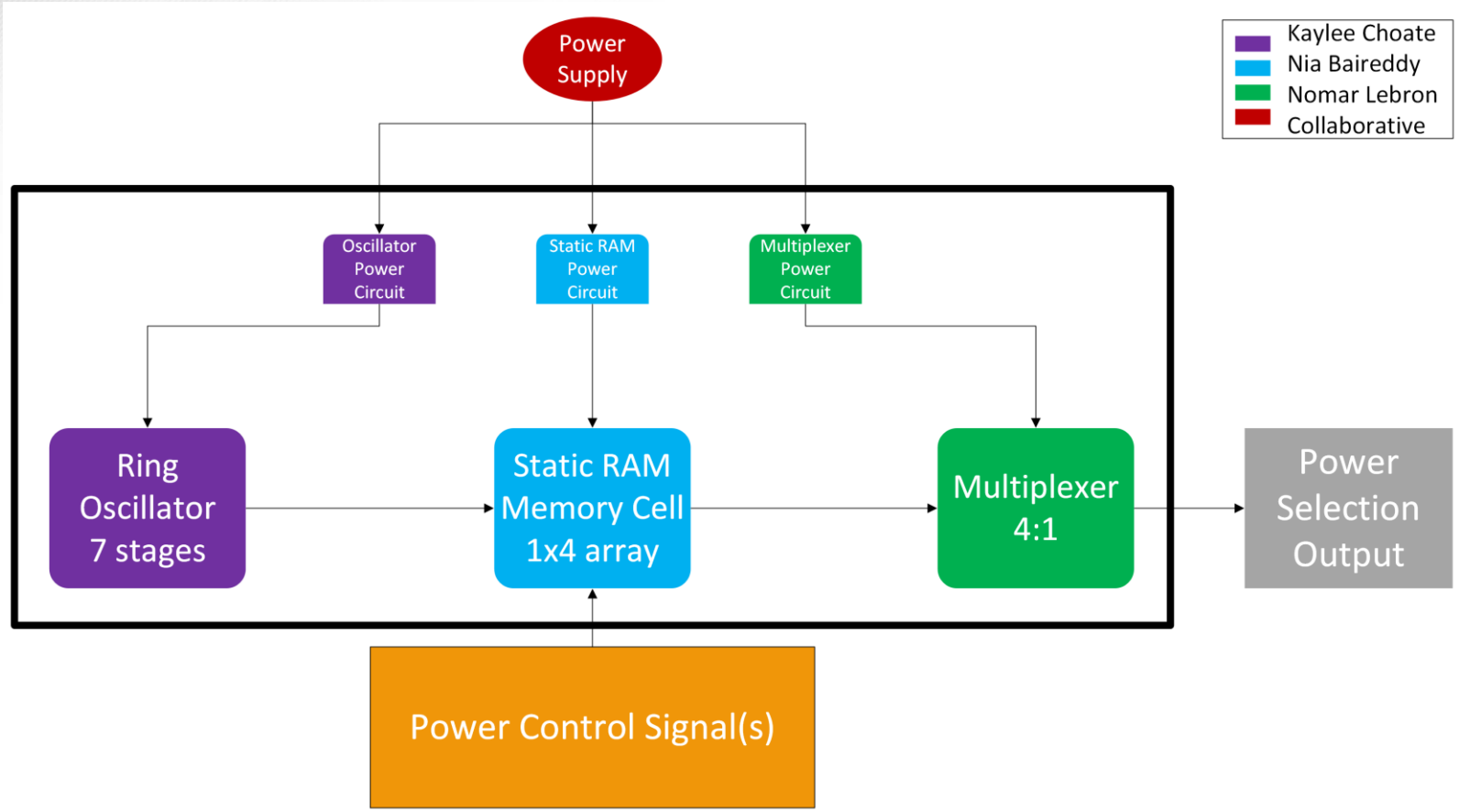
Project Summary and Solution

- Radiation effects on circuits are detrimental and must be mitigated for robust applications in space, military, and nuclear industries.

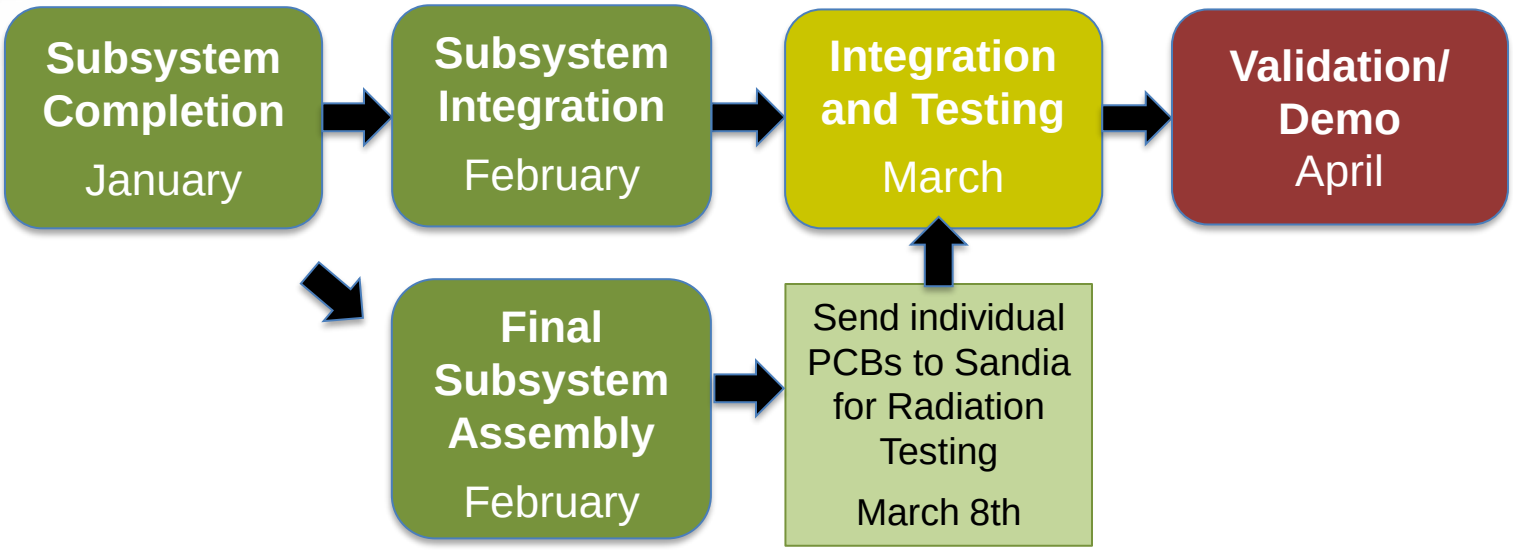
- Use radiation hardening by design techniques to modify various logic circuits for reliable operation in radiation environments.



Integrated System Diagram



Project Timeline



Kaylee Choate

Accomplishments since last update 10 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Sent individual subsystems and user manuals to Sandia • Ordered and received integrated PCB • Began soldering integrated PCB	• Finish soldering integrated PCB • Validation testing on integrated PCB • Receive radiation results from Sandia

Kaylee Choate

7 Stage Ring Oscillator

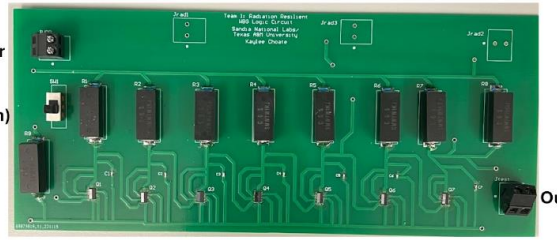
Testing Equipment:

- DC Power Supply
- Oscilloscope
- Set of power supply wires
- Set of oscilloscope wires
- Screwdriver

Board Layout:

Input Power

Switch in downward position (initial condition)



Output

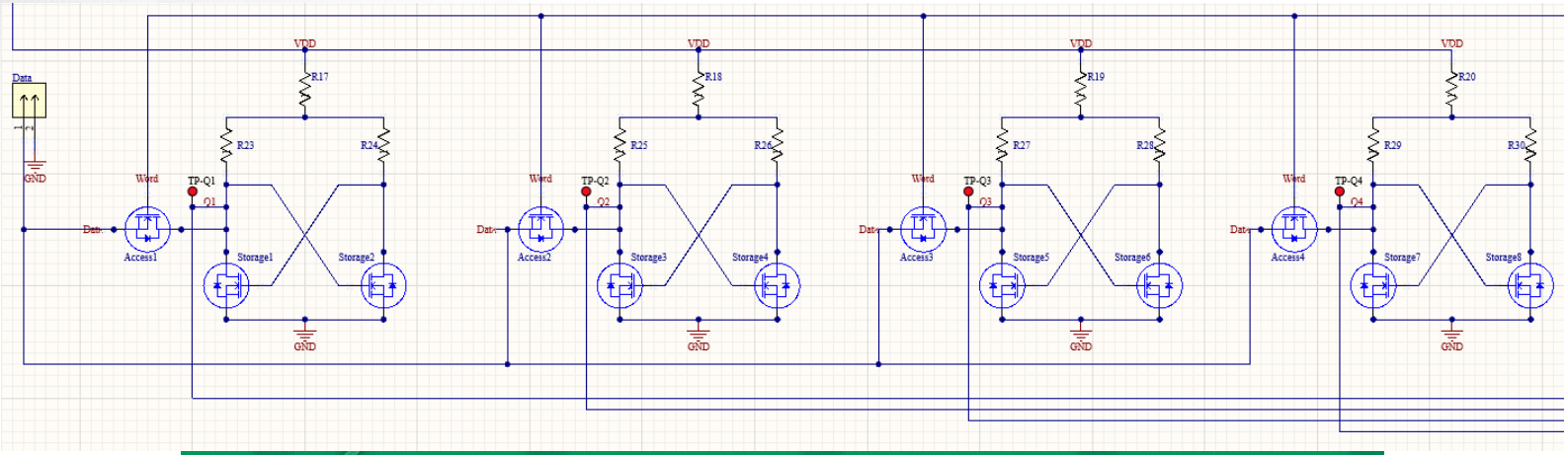
Assembly Procedure:

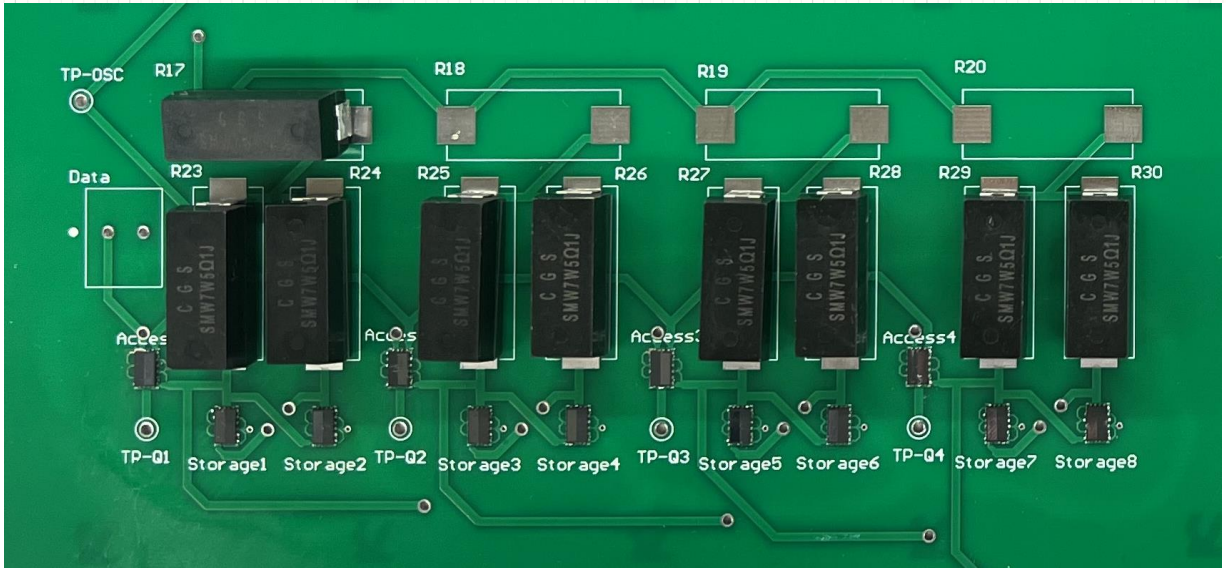
1. Verify that the switch is in the downward position (initial condition).
2. Connect a 5V DC power supply to the input power terminal block. (Dotted side: positive, Non-dotted side: negative)
3. Connect the oscilloscope to the output terminal block. (Dotted side: positive, Non-dotted side: negative)
4. Testing assembly complete.
5. Apply 5V and 0.17A with the DC power supply.
6. Verify that the oscilloscope is reading a constant 5V output.
7. Flip the switch to the upward position to begin oscillations. Expect the oscillation frequency to be in the 90-100kHz range.

Nia Baireddy

Accomplishments since last update 10 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Set dates for radiation testing at Sandia: Apr 8-10 • Ordered and received integrated board • Soldered SRAM array on integrated board	• Finish soldering remainder of board • Specification and scenario validation • Receive radiation testing results from Sandia for report

Nia Baireddy

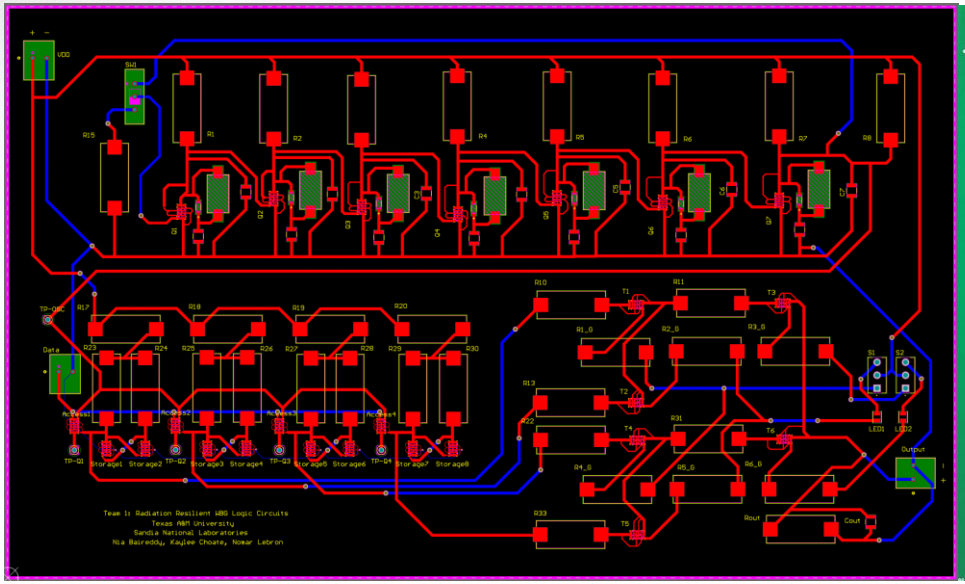


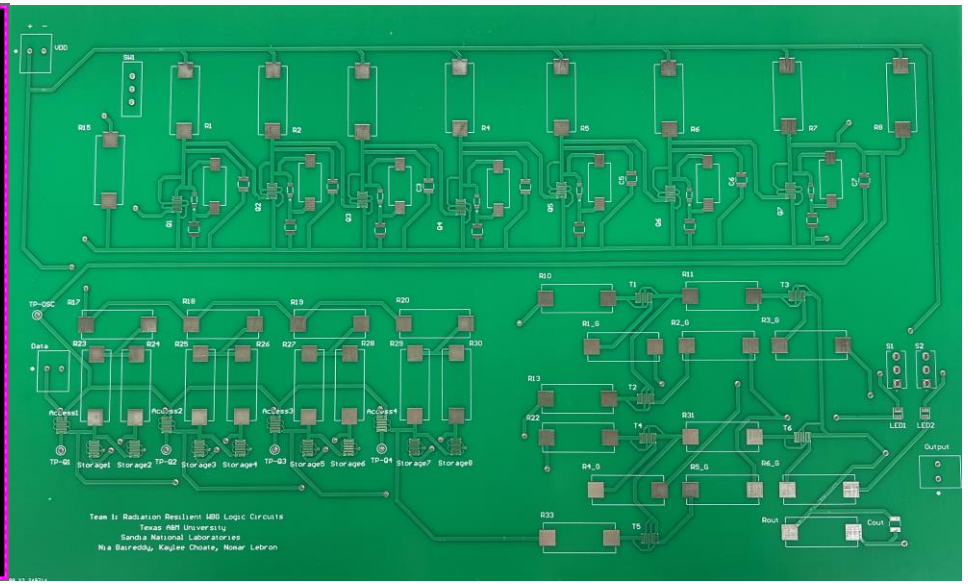


Nomar Lebron

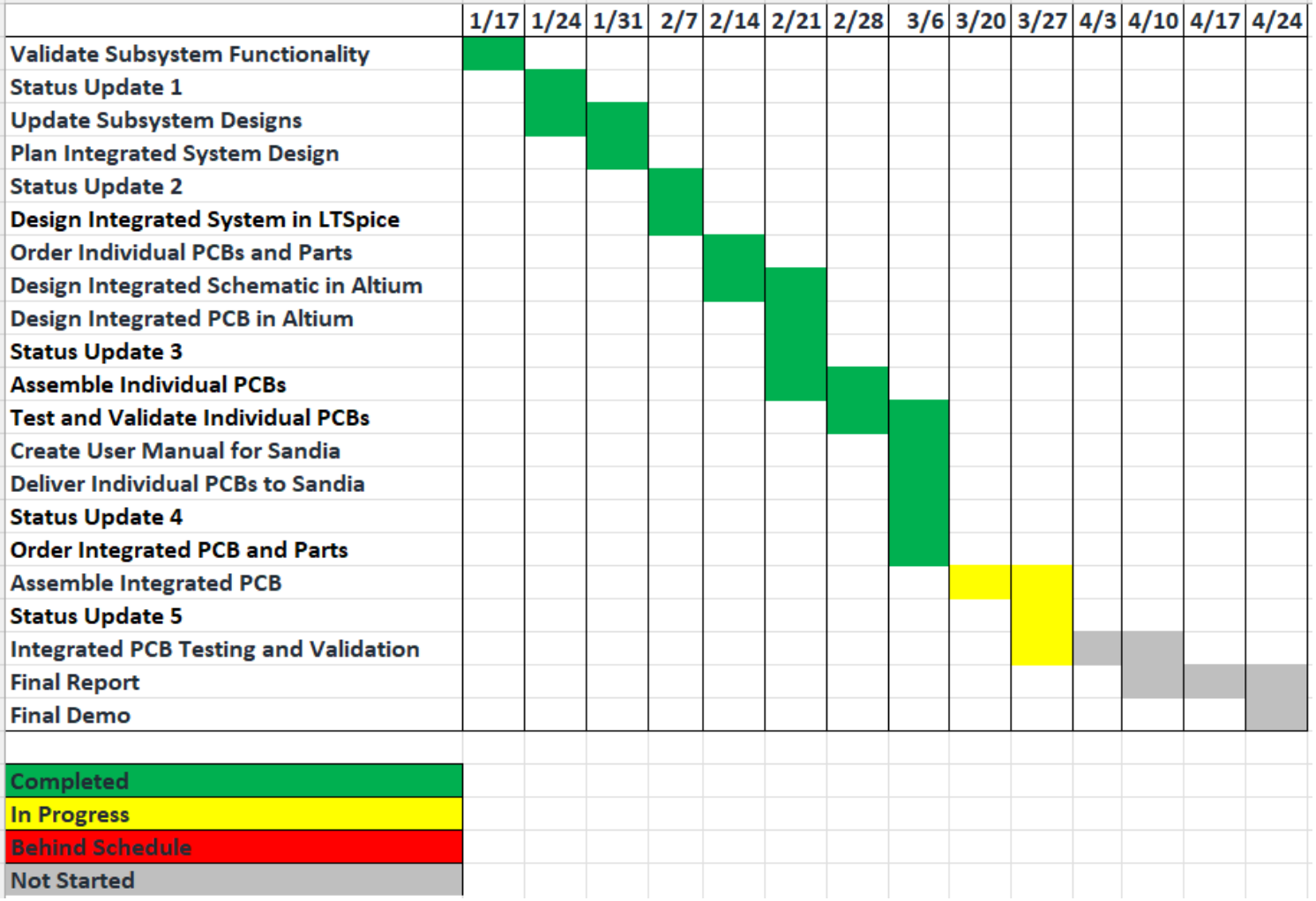
Accomplishments since last update 10 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Sent individual PCB and user manual to Sandia for radiation testing • Ordered and received integrated PCB • Ordered additional parts for integrated PCB • Began soldering integrated PCB	• Finish soldering integrated PCB • Perform validation tests on integrated PCB • Receive radiation test data from Sandia for final report

Nomar Lebron





Execution Plan



Validation Plan - Specifications

Ring Oscillator Task	Specification	Result (Sim)	Result (PCB)	Owner	Date
Voltage Input (max)	5V	Pass		Kaylee	3/27/2024
Square Wave	yes/no	Pass		Kaylee	3/27/2024
Frequency Range	100kHz	Pass		Kaylee	3/27/2024
Magnitude Variation	0-5V	Pass		Kaylee	3/27/2024
Power Consumption	~ 10 mW	Pass		Kaylee	3/27/2024
Supply Voltage Variation Test	Vdd +/- 10%	Pass		Kaylee	3/27/2024
Voltage Spike	50V	Pass		Kaylee	3/27/2024
Voltage Build Up	50V	Pass		Kaylee	3/27/2024
Current Spike	5A	Pass		Kaylee	3/27/2024
Current Build Up	5A	Pass		Kaylee	3/27/2024
1x4 SRAM Memory Cell Array Task	**Specification**	**Result (Sim)**	**Result (PCB)**	**Owner**	**Date**
Voltage Input Max (Vdd)	5V	Pass		Nia	3/27/2024
Read/Write Speed	~ 10 ns	Pass		Nia	3/27/2024
Read/Write Disturb	< 10 cycles	Pass		Nia	3/27/2024
Hold and Setup Time	~ 5 ns	Pass		Nia	3/27/2024
High/Low Voltage	Vdd +/- 10%	Pass		Nia	3/27/2024
Read/Write Stability Margin (Voltage)	Vdd +/- 10%	Pass		Nia	3/27/2024
Power Consumption (active)	~ 10 mW	Pass		Nia	3/27/2024
Power Consumption (idle)	~ 10 uW	Pass		Nia	3/27/2024
Data Recovery Test	~ 10 ms	Pass		Nia	3/27/2024
4:1 Multiplexer Task	**Specification**	**Result (Sim)**	**Result (PCB)**	**Owner**	**Date**
Voltage Input (max)	5V	Pass		Nomar	3/27/2024
Select Line Test	4 inputs	Pass		Nomar	3/27/2024
Data Stability	Vdd +/- 10%	Pass		Nomar	3/27/2024
High/Low Voltage	Vdd +/- 10%	Pass		Nomar	3/27/2024
Power Consumption Test	< 6W	Pass		Nomar	3/27/2024
User Interface Testing	Switches	Pass		Nomar	3/27/2024
User Interface Testing	LEDs on/off	N/A		Nomar	3/27/2024
Supply Voltage Variation Test	Vdd +/- 10%	Pass		Nomar	3/27/2024

Validation Plan - Scenarios

Scenario	Description	Test Procedure	Owner
1: Normal Operation	The circuit controls power distribution to other electronic subsystems (navigation, computing, data collection, etc.) in a low Earth orbit (LEO) satellite.	User will set up and operate the circuit as normal, first supplying VDD, then feeding the input signals to the memory cell array, then selecting one cell's data using the mux selector bits	Kaylee
2: Total Ionizing Dose	The LEO satellite passes through an ozone hole and is exposed to radiation for a significant time (2 min)	User will attempt to disrupt VDD with continuous voltage and current injections significantly higher or lower than rated value and record resulting circuit behavior	Nomar
3: Single Event Upset	The LEO satellite has faulty radiation shielding that allows heavy ions through sporadically	User will attempt to disrupt VDD with voltage and current pulse injections higher or lower than rated value and record resulting circuit behavior	Nia

Thanks and Gig ‘Em!

Questions?