

# Radiation Resilient Logic Circuit Study based on Wide Bandgap Devices

Nia Baireddy, Kaylee Choate, Nomar Lebron

## **CONCEPT OF OPERATIONS**

REVISION – Draft  
5 September 2023

# CONCEPT OF OPERATIONS FOR Radiation Resilient Logic Circuit Study based on WBG Devices

TEAM 1

**APPROVED BY:**

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## 1. Executive Summary

This report details the concept of operations for a study regarding radiation resilient logic circuits using wide-bandgap devices sponsored by Sandia National Laboratories. Radiation has significant effects on the functionality of electronic components and circuits, and it is important to use the various materials and design ideas to try and mitigate those effects in order to create robust circuits that function optimally in radiation environments. Radiation hardening techniques, both by design and by process, are used to make these circuits radiation resilient, though this report only focuses on concepts associated with radiation hardening by design specifically through usage of wide-bandgap materials and modified circuit layouts.

As described in the operation concept section, there are three logic circuits to be designed and tested: a 7 stage ring oscillator, a 4-bit static RAM memory cell array, and a 4:1 multiplexer. These three circuits will use gallium nitride as the wide-bandgap material, and after each individual circuit is built with radiation hardening by design, they will be integrated into a single, large logic circuit system with various applications detailed later in the report. The ring oscillator will provide a clock signal for the 4-bit SRAM array, whose output will feed into the 4:1 multiplexer, resulting in a 1-bit output. The primary application for this single integrated circuit is as control circuitry for power supplies, although there are other uses for it as well as each of the three individual circuits, which are detailed in the scenarios section of the report.

There is also further analysis of the advantages and disadvantages of the proposed improvements, potential limitations, and alternatives regarding the material and design considerations. Finally, the report also considers the project's impact regarding advancements in aerospace applications, environmental efficiency of transistors, and ethical concerns related to radiation testing safety.

## 2. Introduction

Logic circuits must be able to maintain functionality in radiation environments to guarantee reliable performance in critical situations. Logic circuits can be made robust by using radiation hardening techniques, including both radiation hardening by process and radiation hardening by design. These techniques can be used individually or in combination, depending on the type of logic circuit being developed. Materials such as silicon carbide and gallium nitride are often used in the design of circuits that are intended to be radiation resilient. Due to their wide band gap, these materials make the circuit more resistive to ionizing radiation. By collaborating with Sandia National Laboratories, we will utilize radiation hardening by design to create a logic circuit which will be able to function in a radiation environment.

### 2.1. Background

Logic circuits are used for a wide range of applications in modern technology. Employing these circuits is crucial for situations involving digital systems, data processing, automation, and much more. While standard logic circuits may operate effectively in typical environments, they will be insufficient in radiation harsh environments, such as space. Ensuring the dependable performance of these devices in radiation environments is essential for reliability in critical conditions. We will enhance existing logic circuits by implementing radiating hardening by design techniques, therefore allowing these circuits to be functional in the presence of radiation.

### 2.2. Overview

We will construct a radiation resilient logic circuit which will be composed of a ring oscillator, a SRAM, and a multiplexer. Each of these circuits will be made radiation resilient by employing radiation hardening by design techniques. The main application of our project will be for space power systems and logic control systems. The use of ring oscillators, SRAMs, and multiplexers in space power/logic control systems is increasing. By analyzing how these circuits perform in radiation as a whole, it will provide information about how the individual circuits react in a radiation environment when connected to a bigger circuit. The use of wide band-gap devices such as silicon carbide (SiC) and gallium nitride (GaN) in logic circuits enhances their resilience to radiation. Since Silicon carbide has had significantly more research and usage in power electronics, our circuit will employ Gallium nitride as the wide band-gap device to promote further research on this material. By choosing Gallium nitride as our wide band-gap device, the implementation and testing of this project will provide more information on the effects of GaN in a radiation environment.

### 2.3. Referenced Documents and Standards

*Electrical, Electronic, and Electromechanical (EEE) Parts Assurance Standard.* NASA. Accessed: Sep. 12, 2023. [Online]. Available: <https://standards.nasa.gov/sites/default/files/standards/NASA/Baseline/0/nasa-std-873910.pdf>

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R. Baumann and K. Kruckmeyer, *Radiation Handbook for Electronics*. Texas Instruments, 2020. Accessed: Sep. 2023. [Online]. Available:  
<https://www.ti.com/seclit/eb/sgzy002a/sgzy002a.pdf>

Reed, Goetz, Ericson, Sweeney, and Ezell, “Wide Bandgap Semiconductors for Extreme Temperature and Radiation Environments,” *Oak Ridge National Laboratory*, Mar. 2022.

## 3. Operating Concept

### 3.1. Scope

The logic circuit for our project will be composed of three individual logic circuits, which will be integrated to construct the final circuit. The individual circuits will consist of a ring oscillator, a SRAM, and a multiplexer. A seven-stage ring oscillator will produce an oscillating clock signal with a frequency of 100kHz. This signal will be connected to the input of a 4-bit SRAM which will retain data in memory. The SRAM will then provide input to a 4x1 multiplexer which will select the output data from one of the four binary inputs. A DC power supply will provide input power to the circuit, which will be 3V. The three individual circuits will be built on a transistor level, utilizing Gallium nitride (GaN) as the wide band-gap material. The goal of our project is for our final circuit to maintain functionality in a radiation environment. To achieve this, we will focus on implementing radiation hardening by design on the three individual circuits. Radiation hardening by design focuses on the design of the circuit itself, rather than the manufacturing process of the circuit components. Our final circuit will be tested in a radiation environment to observe the effect of radiation on the output data. Our circuit should maintain consistent in a radiation or non-radiation environment.

### 3.2. Operational Description and Constraints

The main application of this logic circuit would be as a control circuit for power supplies. In radiation environments, power electronics are particularly important to radiation harden as they connect to all other parts of an electrical system, so radiation effects in a power circuit could be detrimental to the rest of the system. The entire circuit would yield a single bit output that would be used to switch power on and off to other circuits. Individually, these logic circuits can be used for a variety of applications in radiation environments.

### 3.3. System Description

The proposed system has three major subsystems: a seven-stage ring oscillator, a 4-bit SRAM memory cell array, and a 4-to-1 multiplexer.

#### 3.3.1. 7 Stage Ring Oscillator

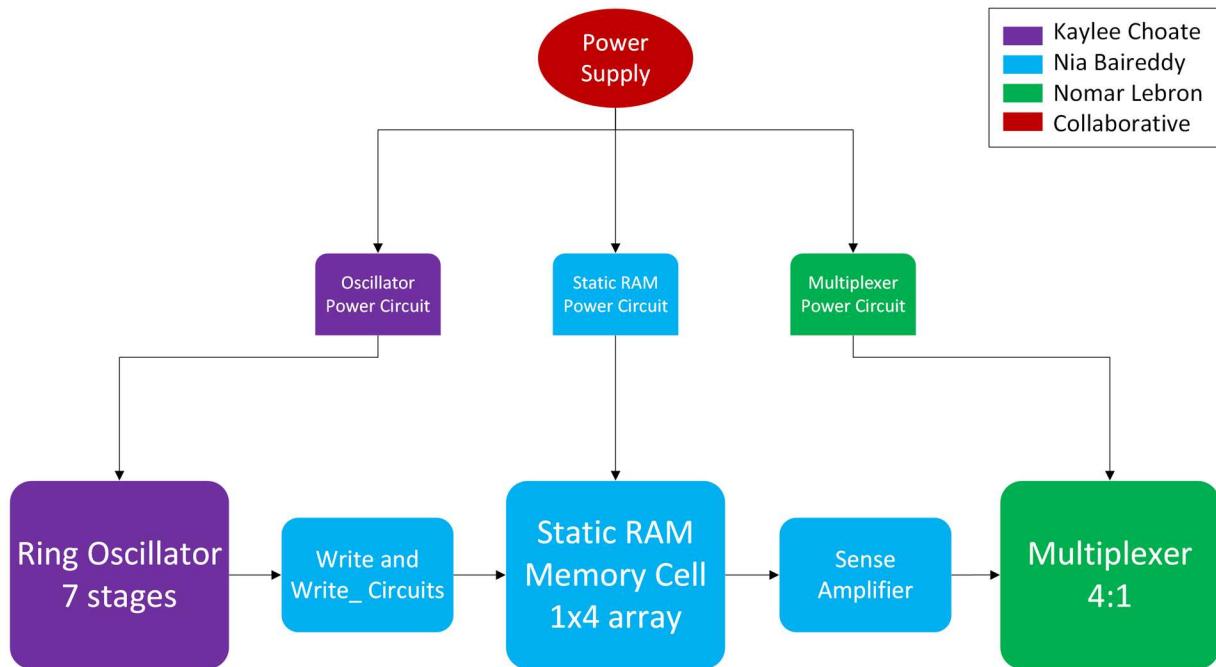
The seven-stage ring oscillator will receive power from a DC power supply and produce an alternating signal output at a desired frequency. It is capable of producing an oscillating output without a connection to an external function generator. The ring oscillator will consist of seven inverters arranged in a ring. The internal design of these inverters will be composed of transistors with a wide band-gap material so that the circuit will be functional in a radiation environment. The design of the ring oscillator will also include a feedback connection from the Vout pin to the first input pin. It will also include capacitors connected in parallel between each inverter. As the signal passes through each inverter, it will be delayed which decreases the frequency. The capacitance of the capacitors between each inverter will be chosen so that the output frequency of the ring oscillator is 100kHz. The output signal produced from the oscillator will serve as the input signal for the 4-bit SRAM.

### **3.3.2. 4-bit SRAM Memory Cell Array**

An SRAM memory cell array is a logic circuit that stores bits of data, 4 bits in this layout. SRAM is a kind of volatile memory that retains data as long as it has a power supply, and it's commonly used in computer systems for its fast access times and simple design. Each cell consists of at least four storage transistors connected in a feedback loop to form a bistable flip flop circuit, and these transistors maintain the stability of the stored data until intentionally changed by a write operation. Two additional access transistors can be added to control read and write operations, and they act as switches that allow or block dataflow between storage nodes and read/write lines. These access transistors allow the cell to be read and written to without affecting the other cells in the array. It consumes little power, so it's powered by a simple, low DC power supply. The cells can be arranged in different configurations, like a 2x2 or a 4x1/1x4 array, and each has its advantages and disadvantages which are detailed in Section 4.2. The behavior of memory cells in radiation environments is important to consider, as total ionizing dosage has significant effects on data storage. Single Event Upsets (SEUs) can flip the state of a memory cell bit, effectively corrupting the data. Radiation can lead to temporary data corruption, soft errors, or even complete data loss, which can be combatted by error detection and correction techniques that add redundancies to stored data and correct errors as they occur. This array will be radiation-hardened by design using wide bandgap transistors, like gallium nitride, and other methods to ensure that the entire circuit is radiation resilient.

### **3.3.3. 4-to-1 Multiplexer**

The 4-to-1 Multiplexer, or 4:1 MUX for short, is a logical circuit that receives four binary values as the input, and outputs one of those four values depending on the state of two additional selection bits. By controlling the selection bits, the user can select which of the four inputs the 4:1 MUX will use as the output. For our system, the 4:1 MUX will be selecting between the four binary values stored in the 4-bit SRAM cell array. This will allow the user to efficiently read out any of the four values stored, to determine whether or not they've been affected by radiation. The logic inside the MUX is conducted using numerous transistors that are themselves susceptible to radiation. Because of this, the use of wide-band gap transistors, namely gallium nitride, will be implemented along with other methods of radiation hardening by design to make the entire system radiation resilient.



**Figure 1: Subsystem Block Diagram**

### 3.4. Modes of Operations

#### Active

The system is in the active mode of operation when power is connected to the system causing the ring oscillator to run and produce an oscillating output signal. This output signal is then routed to the input of the SRAM array where the binary values are stored. Lastly, the 4:1 MUX is connected to the SRAM array to select which of the four SRAM bits to read out as the output. The selecting of values from the SRAM array utilizing the MUX is what constitutes the system as active.

#### Idle

The system is in the idle mode of operation when power is once again connected to the system causing the ring oscillator to oscillate. This output signal will continue to input binary values into the SRAM array. However, in this mode of operation, the 4:1 MUX is not being utilized to select between the four bits of the SRAM array.

#### Off

The system is in the off mode of operation when the system is not connected to the power supply. This means the ring oscillator will not oscillate, the SRAM array will not store values, and the 4:1 MUX will not select values from the array.

### **3.5. Users**

The primary users of the system will be different disciplines of engineers depending on the application. For example, during the testing process, radiation test engineers and radiation hardness assurance engineers would be the primary users of the system. The user manual mentioned in the following section will guide the test engineers through the set up and operation of the system. After testing, the system can be utilized by power or system engineers to help with the control of power circuitry, as mentioned in section 4.

### **3.6. Support**

Support for operating the individual subsystems and the total system will be provided in a detailed user manual. This document will provide support for setting up and running the circuits for both typical and radiation testing, as well as steps for troubleshooting any common problems. The user manual will include the electrical schematics of all three subsystems, as well as how the circuitry integrates together.

## 4. Scenario(s)

### 4.1. Control Circuitry for Power Supply

This comprehensive circuit is best used as a control circuit for a power supply. As the output is 1 bit, it is a simple switch for on/off power control to a load. It can be used to implement control logic in a system where multiple power supplies or voltage sources need to be on or off based on user inputs or certain conditions. The ring oscillator provides a clock signal for the 4-bit SRAM array to store or modify bits related to configuration data or power supply management control signals, which each correspond to one of the four mux inputs. Depending on what the mux selector bit is, a certain power supply configuration from the 4 bit input is chosen. It is important to note that additional circuitry would be needed to translate the selected data configuration into actual control of multiple power supplies.

### 4.2. 7-Stage Ring Oscillator

Ring oscillators have applications which can prove useful in many different scenarios:

- Ring oscillators are most commonly used as clock generators for electronic circuits. The oscillating output signal they produce serves as a clock signal for logic circuits.
- Ring oscillators can be used for timing purposes in a circuit. They can be implemented to produce controlled delays for a signal that is present in a circuit by adjusting resistor and capacitor values.
- In some applications ring oscillators can be used as voltage-controlled oscillators (VCOs) by incorporating a controlled input that will determine the frequency of oscillation. VCOs are commonly used for applications such as phase locked loops and frequency modulation.
- Ring oscillators are sensitive to temperature variations. This makes them suitable for use as temperature sensors since a change in temperature affects the frequency of oscillation.

### 4.3. 4-bit SRAM Memory Cell Array

SRAM memory cell arrays have a multitude of applications for various scenarios:

- Their suitability for harsh environments makes them ideal for navigation, communications, and guidance systems in the military and aerospace industry.
- They're most commonly used as cache memory in computer systems, and a 4-bit SRAM in particular could be used as a small, high-speed cache to store frequently accessed data efficiently.
- They can be used as registers within a CPU or microprocessor to perform arithmetic or logical operations, as well as a temporary storage for data during processing.
- SRAM is used as buffer storage in data communication, networking equipment, and storage devices to help manage data flow and provides temporary storage for smoother data transfer.

The arrangement of cells also determines how effective the SRAM cell array is in certain scenarios:

- A 1x4 or 4x1 array is more space efficient as its just a single row, and it has shorter access time because of the simpler structure and minimal bitline length. It typically consumes less power as it has fewer transistors and shorter bitlines, and it's best suited for size-efficient applications that require a small, efficient memory structure.

- A 2x2 array might require more layout space as it's a square grid, and it would have longer access times because of the additional bitline routing. It would also consume more power than a 4x1 array and it's best suited for applications that require more organization due to the ease of managing a grid layout.

#### **4.4. 4-to-1 Multiplexer**

Multiplexers are an incredibly practical device that can be utilized in many different types of applications. There are many scenarios where multiple input signals enter a device, and the user would like the ability to select which of the inputs should be read out as the output. Because of this, multiplexers are useful in a variety of applications.

- Multiplexers are heavily utilized in communication systems, as they allow for the transmission of multiple different input signals (audio or video) along one singular transmission line. This greatly reduces cost and increases efficiency.
- Considering the radiation environment, multiplexers are utilized in satellite and deep space flight systems to transmit data from the onboard computer systems back to the ground station, using GPS.
- An application similar to the one proposed would be utilizing multiplexers in the memory of a computer. Multiplexers are scattered throughout the architecture of a computer, meaning radiation resilient multiplexers would enhance the overall efficiency of computing in space.

### **5. Analysis**

#### **5.1. Summary of Proposed Improvements**

- Wide-bandgap transistors
  - Greater breakdown voltage
  - Higher current limitations
  - Faster switching speeds
  - Extreme temperatures

- More efficient and power dense
- Radiation hardening by design
  - Radiation resilient transistors
  - Modified layout design may be more compact and less expensive

## 5.2. Disadvantages and Limitations

- Wide-bandgap semiconductor devices are expensive
- Size as a limiting factor
- Availability of parts
- Less research information on Gallium nitride transistors

## 5.3. Alternatives

Below are alternative materials for wide bandgap devices that make up these logic circuits:

- Silicon carbide (*SiC*)
  - SiC transistors would allow for more power to be delivered through the system, however, for the application, the higher switching frequency of GaN proves more beneficial.
- Gallium Oxide (*Ga<sub>2</sub>O<sub>3</sub>*)
  - Gallium Oxide has a high electron/hole mobility, similar to GaN, making it a viable alternative. However, the difficulties of cost and research increase drastically as gallium oxide is the newest and not yet as widely used.
- Radiation Hardening by Process
  - Traditional Silicon transistors could be utilized, with the design adjustments being made in the actual fabrication of the components, such as radiation shielding. This is not a viable alternative for this project since it would not be possible to fabricate custom components.

Below are alternatives for layouts for each of the subsystem circuits:

- >7- Stage Ring Oscillator
  - Adding more stages would yield lower frequency ranges.
- 4-bit SRAM Memory Cell – 4x1 or 2x2 array
  - There are many advantages and disadvantages to either array layout depending on user need and system design, which are detailed in Section 4.3.
- Multiplexers
  - The multiplexer can be edited to contain however many inputs and outputs are required. Alternative designs could have included two 2:1 MUXs or one 4:2 MUX in order to read two outputs at once.

## 5.4. Impact

- Space exploration for the benefit of humankind
- More efficient transistors result in less waste in the environment
- Ethics concerning safety with radiation testing



# Radiation Resilient Logic Circuit Study with Wide Bandgap Devices

## Nia Baireddy, Kaylee Choate, Nomar Lebron

# **INTERFACE CONTROL DOCUMENT**

REVISION – Draft  
25 January 2018

INTERFACE CONTROL DOCUMENT  
FOR  
Radiation Resilient Logic Circuit Study based on WBG  
Devices

PREPARED BY:

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**Author** \_\_\_\_\_ **Date** \_\_\_\_\_

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John Lusher II, P.E. Date

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T/A Date

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## 1. Overview

This document details the scope of how the various subsystems with their respective power circuits and eventually, each other. It lists physical interface details like weight and volume for each of the subsystems and electrical interface details like input/output signals and connections between parts. A description of how each subsystem communicates its results to the user and the interfacing between devices is also detailed.

## 2. References and Definitions

Below are the references and definitions used in this document.

### 2.1. References

#### **MIL-STD-750F**

#### **Test Methods for Semiconductor Devices**

03 Jan 2012

Change Notice 2

30 Nov 2016

#### **SMC-S-008**

#### **Electromagnetic Compatibility Requirements for Space Equipment and Systems**

13 June 2008

#### **SMC-S-010**

#### **Technical Requirements for Electronic Parts, Materials, and Processes Used in Space Vehicles**

01 Apr 2013

### 2.2. Definitions

BIT	Built-In Test
DC	Direct Current
ICD	Interface Control Document
kHz	Kilohertz (1,000 Hz)
krad	Kilorad (1000 rad)
LED	Light-emitting Diode
MHz	Megahertz (1,000,000 Hz)
MUX	Multiplexor
mW	Milliwatt
PCB	Printed Circuit Board
SRAM	Static Random Access Memory
V	Volts
°C	Degrees Celsius

### **3. Physical Interface**

#### ***3.1. Weight***

There are no specific requirements for the weight of the entire system or each of the subsystems. The typical weight of a system like this should not exceed more than 3 lbs, given that it is a set of PCBs.

#### ***3.2. Dimensions***

The dimensions of the system shall be less than or equal to 5 inches in height, 10 inches in width, and 13.25 inches in length.

##### **3.2.1. Dimension of Subsystems**

There are no specific requirements for the dimensions of the subsystems, as long as they all fit in the total system volume without conflict.

## 4. Thermal Interface

While thermal characteristics are important in any system, the thermal interface is not a dominating factor in our system's design criteria. There will be no type of liquid or air cooling necessary, as well as no heat sinks required to better dissipate heat. Whilst the system is being designed for space applications, it is not being designed for vacuum applications where liquid cooling and heat sinks would be necessary due to the lack of convection and conduction. Because of this, the system will not need any active cooling. The system should be able to operate properly at temperatures up to 80 degrees Celsius.

## 5. Electrical Interface

### 5.1. Primary Input Power

The primary input power for the logic circuit system shall be 3VDC. The system shall receive this voltage from a DC power supply.

### 5.2. Signal Interfaces

Signal interfaces for the system will include connectors on the PCB that will supply power from the DC power source to the logic circuit. The system will also contain PCB traces to allow for connection between electrical components on the PCB. The system will have connectors on the PCB to establish connections between subsystems for total system integration.

### 5.3. User Control Interface

There will be a rudimentary user control interface present on the final PCB consisting of LEDs and pushbuttons. Using these components, the user will be able to see the values contained within the SRAM cell array, as well as control and monitor which of the four cells in the 1x4 SRAM array is being read out as the output of the 4:1 MUX. This control interface works by connecting the pushbuttons to the selection bits of the MUX. Using two selection bits, i.e. two pushbuttons and two LEDs, the user can quickly select which of the four cells to read out, and use the LEDs to signify which cell is being read out. The LED on being high or 1, and the LED off being low or 0. Cell 1 would be 00, Cell 2 01, and so on. There will be four LEDs surrounding the 1x4 SRAM array to represent the value in each cell. An LED will flash to represent the rising edge of the clock produced by the ring oscillator. Lastly, there will be an LED to represent the value of the output, to allow for testing without need for the oscilloscope. In total, there will be eight LEDs and two pushbuttons as part of the user control interface.

## 6. Communications / Device Interface Protocols

### 6.1. Subsystem Communication

Since the system is fully hardware based, there is no traditional telecommunication system necessary to communicate between subsystems. However, there is still physical communication required between subsystems due to the outputs of the ring oscillator and SRAM array being the inputs to the subsequent circuits. How these circuits communicate has been outlined in both the Concept of Operations as well as the Functional System Requirements and will be managed via traces and connectors on the PCB.

### 6.2. Oscilloscope

The system will connect to an external oscilloscope during the radiation testing. The final system PCB will include a banana cable connector for easy connection and communication with the oscilloscope.

# Radiation Resilient Logic Circuit Study with Wide Bandgap Devices

## Nia Baireddy, Kaylee Choate, Nomar Lebron

## **FUNCTIONAL SYSTEM REQUIREMENTS**

# FUNCTIONAL SYSTEM REQUIREMENTS FOR Radiation Resilient Logic Circuit Study based on WBG Devices

**PREPARED BY:**

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**Author** \_\_\_\_\_ **Date** \_\_\_\_\_

**APPROVED BY:**

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**Project Leader** \_\_\_\_\_ **Date** \_\_\_\_\_

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John Lusher, P.E. Date

T/A Date

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## 1. Introduction

### 1.1 Purpose and Scope

Radiation has a significant impact on the operation and effectiveness of electronic circuits and systems. It is imperative for logic circuits to maintain their functionality in radiation environments to ensure dependable performance, so mitigation strategies must be implemented in circuits that are expected to be exposed to radiation. Logic circuits can be made radiation resilient by implementing radiation hardening techniques, encompassing both radiation hardening by process and radiation hardening by design. Incorporating wide band-gap materials such as Silicon Carbide and Gallium Nitride into logic circuit design enhances the circuit's resistance to radiation. The wide band-gap of these materials allows the logic circuit to withstand ionizing radiation. We will utilize radiation hardening by design techniques and wide-band gap materials to create a logic circuit that should be able to function in a radiation environment. Following the design phase, our circuit will undergo testing in a radiation environment to observe its response to exposure to radiation. Our goal is to ensure consistent performance of the logic circuit whether in a radiation or non-radiation environment.

### 1.2 Responsibility and Change Authority

The team leader, Nia Baireddy, will be in charge of making sure the system requirements are met, as well as having the authority to make changes to the documentation. All decisions will be discussed with all three team members and the company sponsor before arriving at a final decision, however, the final decision lies with the team leader.

Subsystem	Responsibility
7-Stage Ring Oscillator	Kaylee Choate
1x4 SRAM Memory Cell Array	Nia Baireddy
4-to-1 Multiplexer	Nomar Lebron

## 2. Applicable and Reference Documents

### 2.1 Applicable Documents

The following documents, of the exact issue and revision shown, form a part of this specification to the extent specified herein:

Document Number	Revision/Release Date	Document Title
MIL-STD-750	Revision F = 01/03/2012	Test Methods for Semiconductor Devices
SMC-S-008	06/13/2008	Electromagnetic Compatibility Requirements for Space Equipment and Systems
SMC-S-010	04/01/2013	Technical Requirements for Electronic Parts, Materials, and Processes Used in Space Vehicles

### 2.2 Reference Documents

The following documents are reference documents utilized in the development of this specification. These documents do not form a part of this specification and are not controlled by their reference herein.

Document Number	Revision/Release Date	Document Title
NASA-STD-8739.10	06/13/2017	Electrical, Electronic, and Electromechanical (EEE) Parts Assurance Standard
NASA-HDBK-4002	06/07/2022	Mitigating In-Space Charging Effects – A Guideline
		Radiation Handbook for Electronics
		Wide Bandgap Semiconductors for Extreme Temperature and Radiation Environments

### 2.3 Order of Precedence

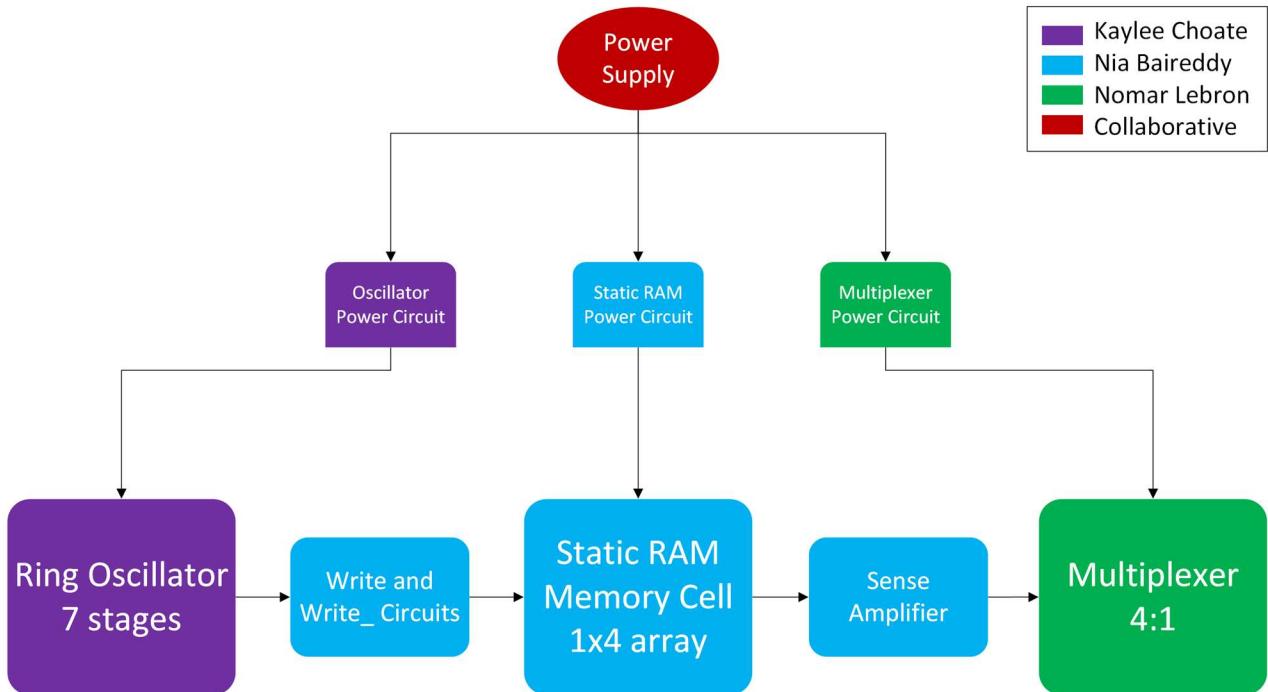
In the event of a conflict between the text of this specification and an applicable document cited herein, the text of this specification takes precedence without any exceptions.

All specifications, standards, exhibits, drawings or other documents that are invoked as “applicable” in this specification are incorporated as cited. All documents that are referred to within an applicable report are considered to be for guidance and information only, except ICDs that have their relevant documents considered to be incorporated as cited.

## 3. Requirements

### 3.1. System Definition

The proposed system is a logic circuit that is expected to withstand exposure to radiation. The main application of the system will be for space power systems and logic control systems. The system will be composed of three distinct logic circuits, which will be integrated to construct the final circuit. The individual circuits will consist of a ring oscillator, a SRAM, and a multiplexer. Each of these individual circuits will be built at a transistor level, employing Gallium Nitride (GaN) as the wide band gap material for the transistors. Additionally, radiation hardening by design techniques such as redundancy, shielding, and spacing of components will be applied to each circuit to improve their resilience to radiation. By analyzing how the final circuit performs when exposed to radiation, information can be gathered about how each individual circuit reacts to radiation when connected to a larger circuit.



**Figure 1. Block Diagram of System**

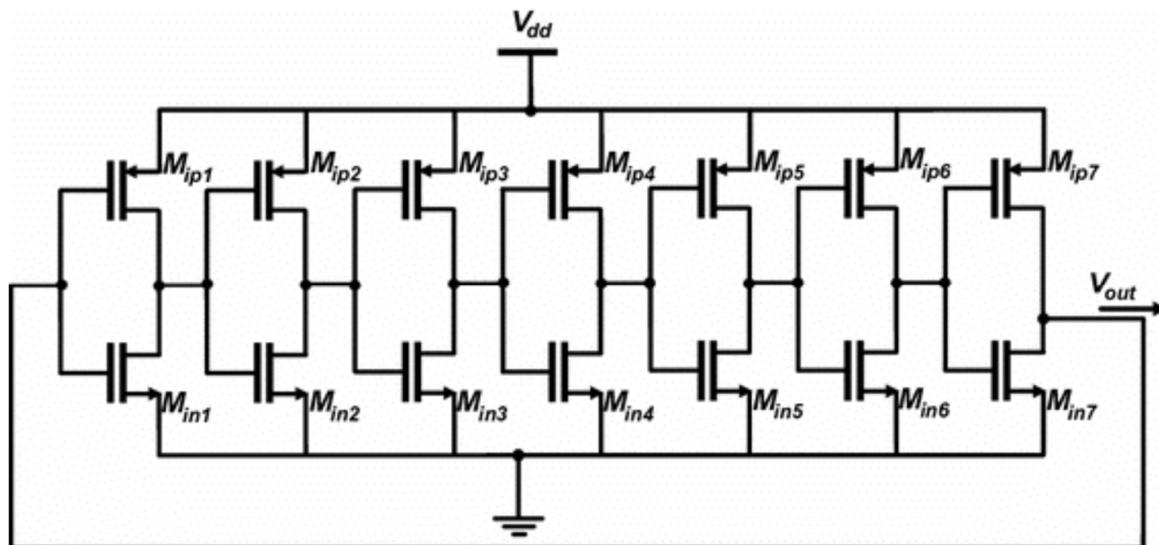
Our system will consist of a seven-stage ring oscillator, a SRAM memory cell 1x4 array, and a 4:1 multiplexor, all of which will receive an input voltage supply of 3V.

The seven-stage ring oscillator will receive power from a DC power supply and shall generate an alternating output signal with a frequency of 100kHz. The oscillator will consist of seven inverters arranged in a ring configuration and will include a feedback connection from the Vout pin to the first input pin. Initially, the nominal output frequency of the ring oscillator is greater than 100kHz, so capacitors will be introduced in parallel with the output of each oscillator stage to decrease the nominal output frequency to the desired output frequency. The resulting oscillating output from the ring oscillator will serve as a clock signal,

which will be directly connected to the wordline and bitlines of the 1x4 SRAM array. Radiation hardening by design techniques will be applied to the ring oscillator to prevent interruptions of the frequency and magnitude of the output signal in the presence of radiation.

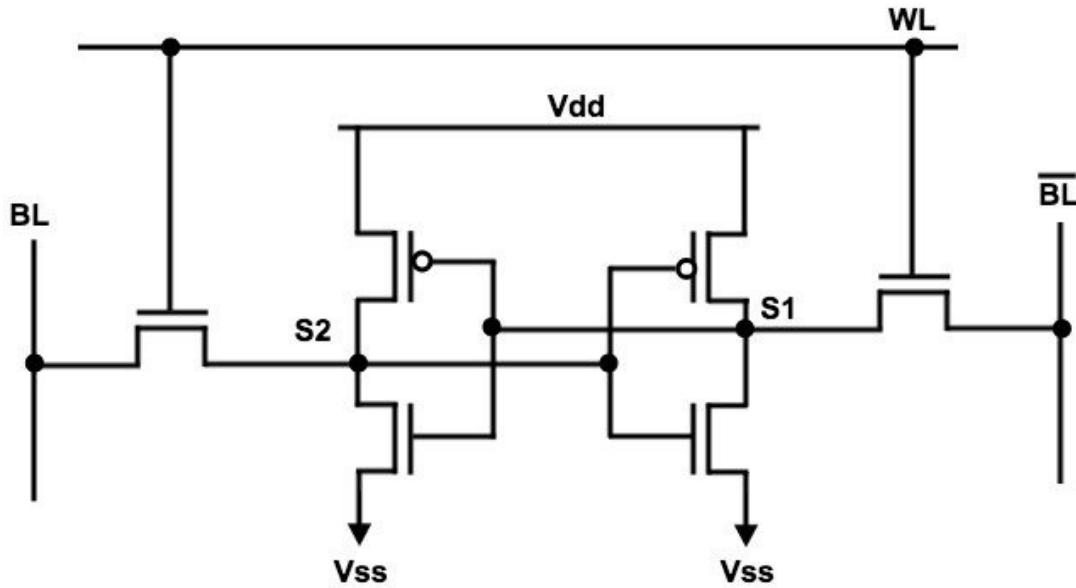
The 1x4 SRAM memory cell array will receive power from an external DC power supply. The read and write operations of the array are synchronized by the clock signal input from the seven stage ring oscillator. The design consists of four cells connected in a row via the wordline, with each cell consisting of six transistors organized in the layout shown in Figure 3. The cell to read from and write to are chosen by the wordline, which indicates the row, and the bitlines, which indicate the column. Each cell has two bitlines that are precharged to a certain voltage level in order to allow access for write operations to occur, and the cross-coupled inverters latch onto the input values and store the written data as long as power is applied. This circuit must be radiation hardened to prevent loss of that stored data when hit with an ionizing dose, which requires the transistors to be radiation hardened as well as the power input interface.

The 4-to-1 Multiplexer will receive power from an external DC power supply and go into a voltage divider to get the desired voltage of 3V DC. The 4:1 MUX input will be connected to the four bitlines of the 1x4 SRAM Cell Array to read the values in the cells. This allows the ability for the 4:1 MUX to select between the four cells in the 1x4 SRAM array and output the desired cell value. The selecting between cells will be done with an external command, utilizing pushbuttons to edit the value of the MUX selection bit. The main purpose of the 4:1 MUX is to read out the values in the SRAM array as the final output of the system to determine whether the values in the SRAM cell array have been altered due to radiation. However, the transistors within the 4:1 MUX themselves are radiation susceptible, meaning radiation hardening by design is required. Because of this, the logic inside the 4:1 MUX will be implemented utilizing Gallium Nitride transistors for radiation hardening.



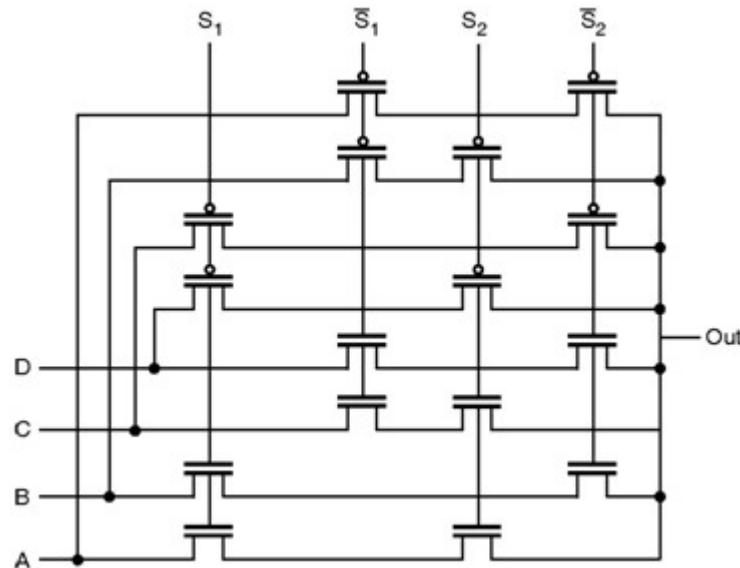
**Figure 2. Seven-Stage Ring Oscillator [1]**

Note: This is a general diagram of a seven-stage ring oscillator which does not include output capacitors.



**Figure 3. Single Cell in the 1x4 SRAM Memory Cell Array [2]**

Note: This is a single cell in the 1x4 array. Four of these cells are consecutively connected via the wordline.



**Figure 4. 4-to-1 Multiplexer [3]**

Note: The system will have a similar topology, however utilizing only NMOS transistors.

## 3.2. Characteristics

### 3.2.1 Functional / Performance Requirements

#### 3.2.1.1 Full System

The functional requirements of the full system include operating a seven-stage ring oscillator to update the binary values in a 1x4 SRAM cell array that can be read out utilizing a 4-to-1 multiplexer. The circuits should be able to perform these tasks whilst being tested in a radiation environment. The functional and performance requirements for each individual subsystem have been outlined below.

*Rationale: This system is meant to be functional in space applications. This requires all the radiation susceptible components, specifically the transistors, to be radiation resilient in order to perform as required.*

#### 3.2.1.2 7-Stage Ring Oscillator

The seven-stage ring oscillator shall receive power from a 3V DC supply and generate an oscillating output signal of 100kHz. The seven-stage ring oscillator shall maintain functionality in a radiation environment.

#### 3.2.1.3 1x4 SRAM Memory Cell Array

The 1x4 SRAM Memory Cell Array receives power and an initial voltage signal from a 3V DC supply that sets the values of the bits in each cell. The clock signal from the seven-stage ring oscillator connects to the word line and bit lines of the array to determine the frequency at which a certain cell changes state. The cell array should be able to maintain storage of data without corruption or loss in radiation environments.

#### 3.2.1.4 4-to-1 Multiplexer

The 4:1 MUX shall take the values from the 1x4 SRAM cell array bit line as the four inputs and read the selected cell out as the output. It should have this functionality in a radiation environment.

## 3.2.2 Physical Characteristics

#### 3.2.2.1 Full System

The volume of the three logic circuits shall be less than or equal to 5 inches in height, 10 inches in width, and 13.25 inches in length. There is no weight requirement.

*Rationale: This is a requirement specified by our customer due to larger circuits being more difficult to test in radiation.*

#### 3.2.2.2 7-Stage Ring Oscillator

The volume of the seven-stage ring oscillator does not need to adhere to any specific dimensions, as long as it fits within the overall system's dimensions, along with the SRAM cell array and the multiplexer.

### **3.2.2.3 1x4 SRAM Cell Array**

The volume of the 1x4 SRAM cell array does not need to adhere to any specific dimensions, as long as it fits within the overall system's dimensions, along with the ring oscillator and the multiplexer.

### **3.2.2.4 4-to-1 Multiplexer**

The volume of the 4:1 multiplexer does not need to adhere to any specific dimensions, as long as it fits within the overall system's dimensions, along with the ring oscillator and the SRAM cell array.

## **3.2.3 Electrical Characteristics**

### **3.2.3.1 Inputs**

- a. The main input into the system is a 3V DC voltage which is connected to the top bus of the 7-stage ring oscillator.
- b. The output of the ring oscillator, the final inverter on the right of the schematic, is the input to the 1x4 SRAM cell array. The ring oscillator output will be connected to the word line of the SRAM array to update the values using the rising clock edge.
- c. The input to the 4:1 MUX is the four values stored inside the 1x4 SRAM cell array. The 4:1 MUX input is connected to the bit line of the SRAM to read out the value in the desired cell based on the MUX selection bits.

*Rationale: The system is three logic circuits combined into one system. Because of this, the output of one circuit is the input of the next circuit in the system.*

#### **3.2.3.1.1 Power Consumption**

- a. The maximum peak power of the full system shall not exceed 6W.
- b. The maximum peak power of the 7-stage ring oscillator shall not exceed 6W.
- c. The maximum peak power of the 1x4 SRAM Cell Array shall not exceed 6W.
- d. The maximum peak power of the 4:1 MUX shall not exceed 6W.

#### **3.2.3.1.2 Input Voltage Level**

The input voltage for the system shall be in the range of +3VDC to +5VDC and shall not exceed +50VDC.

*Rationale: The system is meant to be utilized in space applications, such as control circuitry for power supplies onboard a spacecraft. Most onboard space applications require between 3-5 V DC.*

#### **3.2.3.1.3 External Commands**

The main external command to the system will be the value of the selection bits into the 4:1 MUX. This allows the user the choice of which of the four SRAM cells to read out as the output of the MUX. The command will be implemented using pushbuttons on the PCB.

*Rationale: The external command allows the user to quickly and easily switch between cells within the 1x4 SRAM cell array.*

### **3.2.3.2 Outputs**

- a) The seven-stage ring oscillator will produce an oscillating output signal with a frequency of 100kHz which serve as an input for the SRAM cell array. The magnitude of the output signal will alternate between zero and one.
- b) The output of each cell in the 1x4 SRAM cell array is a binary value depending on the clock signal from the ring oscillator. The output of the SRAM cell array connects to the input of the 4:1 MUX.
- c) The main output of the system is the output of the 4:1 MUX, which will read out the value of the desired cell in the 1x4 SRAM cell array. An oscilloscope will be connected to the output of the system to measure the values of the cells.

*Rationale: The system is three logic circuits combined into one system. Because of this, the output of one circuit is the input of the next circuit in the system.*

#### **3.2.3.2.1 Diagnostic Output**

There will be two main forms of diagnostic outputs, the first being numerous LEDs to represent the value in the 1x4 SRAM cell array, as well as the value of the selection bits to display which of cells is being read out. The second output diagnostic is an oscilloscope placed at the output of the system to determine the value being output by the MUX.

*Rationale: The LEDs provide a quick and easy way to determine the value of each cell, as well as the selected cell, all without the need for an oscilloscope.*

### **3.2.3.3 Connectors**

The system will have connectors on the printed circuit board that establish connections between the ring oscillator and the SRAM, as well as between the SRAM and the multiplexer.

*Rationale: This allows communication between the subsystems.*

### **3.2.3.4 Wiring**

The system will include wiring to supply power from the DC power source to the logic circuit. The system will also contain printed circuit board traces to allow for connection between components.

*Rationale: Provides a way for the logic circuit and its' components to receive electrical power.*

### **3.2.4 Environmental Requirements**

The logic circuit shall be designed to withstand and operate in the environments and laboratory tests specified in the following section.

*Rationale: This is a requirement specified by our customer due to constraints of their system in which the Search and Rescue System is integrating.*

### **3.2.4.1 Radiation**

The logic circuit shall be able to function properly in radiation ranging from 50krad to 100krad.

*Rationale: The logic circuits are required to be radiation resilient for space applications.*

### **3.2.4.2 Thermal**

The logic circuit shall be able to withstand a maximum temperature of 80°C. There will be no heat sink or other type of external liquid cooling.

*Rationale: High temperatures could damage susceptible electronics.*

## **3.2.5 Failure Propagation**

### **3.2.5.1 Failure Detection, Isolation, and Recovery (FDIR)**

A system failure in a non-radiation environment shall be detected by an oscilloscope. A failure in a radiation environment shall be determined by data collected by radiation test engineers.

#### **3.2.5.1.1 Built In Test (BIT)**

The logic circuit will contain LED components which will serve as built-in tests for the system. The LEDs will represent the values inside the cells of the SRAM cell array.

*Rationale: This allows the user to check the values within the SRAM array at a quick glance, as opposed to using the oscilloscope.*

#### **3.2.5.1.1.1 BIT Logic Fault Detection**

BIT shall be able to if the actual value stored in the SRAM array is the same as the expected value. The LEDs will also determine if the value being read out by the multiplexer is the same as the expected value.

#### **3.2.5.1.2 Recovery**

Additional transistor components for the system shall be available to account for minor fault recoveries. The replacement transistors can be soldered onto the PCBs to recover the system.

## 4 Support Requirements

For the operators of the logic circuits, mainly the radiation test engineers, they will be provided with a comprehensive user manual containing all the circuit schematics to explain how the circuits are connected internally. It will also include how to install the circuit for the radiation tests, such as where to put the input voltage and where to connect the oscilloscope to the output. It will address common errors the user can run into during installation.

## Appendix A: Acronyms and Abbreviations

BIT	Built-In Test
DC	Direct Current
ICD	Interface Control Document
kHz	Kilohertz (1,000 Hz)
krad	Kilorad (1000 rad)
LED	Light-emitting Diode
MHz	Megahertz (1,000,000 Hz)
MUX	Multiplexor
mW	Milliwatt
PCB	Printed Circuit Board
SRAM	Static Random Access Memory
V	Volts
°C	Degrees Celsius

## Appendix B: Citations

- [1] Schematic of 7-stage ring oscillator | download ... - researchgate, [https://www.researchgate.net/figure/Schematic-of-7-stage-ring-oscillator\\_fig1\\_318184882](https://www.researchgate.net/figure/Schematic-of-7-stage-ring-oscillator_fig1_318184882) (accessed Sep. 28, 2023).
- [2] AS8-static random access memory (SRAM): Asymmetric SRAM architecture for soft error hardening enhancement - Scientific Figure on ResearchGate. Available from: [https://www.researchgate.net/figure/Standard-6T-SRAM-cell-circuit\\_fig1\\_301740255](https://www.researchgate.net/figure/Standard-6T-SRAM-cell-circuit_fig1_301740255) [accessed 29 Sep, 2023]
- [3] Basic Electronic Tutorials, “4-to-1 Multiplexer,” 4-1-multiplexer-using-CMOS-logic Digital-CMOS-Design || Electronics Tutorial, <https://www.electronics-tutorial.net/Digital-CMOS-Design/Pass-Transistor-Logic/4-1-multiplexer-using-CMOS-logic/> (accessed Sep. 19, 2023).

# Radiation Resilient Logic Circuit Study with Wide Bandgap Devices

## Nia Baireddy, Kaylee Choate, Nomar Lebron

## EXECUTION

	9/5	9/12	9/19	9/26	10/3	10/10	10/17	10/24	10/31	11/7	11/14	11/21	11/28
Define Scope of Project													
Divide Subsystems													
Research Subsystems													
Write Concept of Operations Report													
Write Interface Control Document													
Write Functional System Requirements													
Write Validation Plan													
Write Execution Plan													
Midterm Presentation													
Design Circuit Schematics with CMOS													
Perform Simulations with CMOS													
Research Converting NMOS to PMOS													
Research NMOS Transistor Selection													
Order NMOS Wide Bandgap Transistors													
Download LTSpice and Altium Files													
Design Circuit Schematics with NMOS													
Verify Simulations with NMOS													
Create Circuit Schematic on Altium													
Design Printed Circuit Board on Altium													
Status Update Presentation													
Order Resistors & Capacitors													
Receive Parts													
Assemble Printed Circuit Board													
Prototype/Debug													
Perform Validation Tests on Circuits													
Final Design Presentation													
Final Design Demonstration													
Completed													
In Progress													
Behind Schedule													
Not Started													

## Performance on Execution Plan

The execution plan was completed this semester. Some tasks were done slightly out of order to accommodate team schedules, order arrivals, and class deadlines, but all desired tasks were accomplished. All objectives for this semester outlined by the sponsor, professors, and the team itself were completed thoroughly and effectively.

# Radiation Resilient Logic Circuit Study with Wide Bandgap Devices

## Nia Baireddy, Kaylee Choate, Nomar Lebron

## **VALIDATION**

REVISION – Draft  
25 January 2018

Ring Oscillator Task	Specification	Result (Sim)	Result (PCB)	Owner	Date
Voltage Input (max)	5V	Pass	Pass	Kaylee	10/17/2023
Square Wave	yes/no	Pass	Pass	Kaylee	10/17/2023
Frequency Range	100kHz	Pass	OK	Kaylee	10/24/2023
Magnitude Variation	0-5V	Pass	Pass	Kaylee	10/24/2023
Power Consumption	~ 10 mW	Pass	Pass	Kaylee	11/7/2023
Start Up Time	~ 10 ns	Pass	Pass	Kaylee	10/31/2023
Supply Voltage Variation Test	Vdd +/- 10%	Pass	Pass	Kaylee	10/24/2023
Voltage Spike	50V	Pass	404	Kaylee	10/31/2023
Voltage Build Up	50V	Pass	404	Kaylee	10/31/2023
Current Spike	5A	Pass	404	Kaylee	10/31/2023
Current Build Up	5A	Pass	404	Kaylee	10/31/2023
1x4 SRAM Memory Cell Array Task	Specification	Result (Sim)	Result (PCB)	Owner	Date
Voltage Input Max (Vdd)	5V	Pass	Pass	Nia	10/17/2023
Read/Write Speed	~ 10 ns	Pass	Pass	Nia	10/24/2023
Read/Write Disturb	< 10 cycles	Pass	Pass	Nia	10/24/2023
Hold and Setup Time	~ 5 ns	Pass	Pass	Nia	10/31/2023
High/Low Voltage	Vdd +/- 10%	Pass	Fail	Nia	10/31/2023
Read/Write Stability Margin (Voltage)	Vdd +/- 10%	Pass	Fail	Nia	10/31/2023
Power Consumption (active)	~ 10 mW	Pass	Pass	Nia	11/7/2023
Power Consumption (idle)	~ 10 uW	Pass	Pass	Nia	11/7/2023
Voltage Spike	Vq > 2.5V	OK	404	Nia	11/7/2023
Voltage Buildup	Vq > 2.5V	OK	404	Nia	11/7/2023
Data Recovery Test	~ 10 ms	OK	OK	Nia	11/7/2023
4:1 Multiplexer Task	Specification	Result (Sim)	Result (PCB)	Owner	Date
Voltage Input (max)	5V	Pass	Pass	Nomar	10/17/2023
Select Line Test	4 inputs	Pass	Pass	Nomar	10/31/2023
Data Stability	Vdd +/- 10%	Pass	Pass	Nomar	10/24/2023
High/Low Voltage	Vdd +/- 10%	Pass	Fail	Nomar	10/24/2023
Voltage Spike	10V	Pass	404	Nomar	10/31/2023
Voltage Build Up	50V	Pass	404	Nomar	10/31/2023
Current Spike	1A	Pass	404	Nomar	10/31/2023
Current Build Up	1A	OK	404	Nomar	10/31/2023
Power Consumption Test	< 6W	Pass	Pass	Nomar	11/7/2023
User Interface Testing	Switches	Pass	Pass	Nomar	11/24/2023
User Interface Testing	LEDs on/off	N/A	404	Nomar	10/31/2023
Supply Voltage Variation Test	Vdd +/- 10%	Pass	Pass	Nomar	10/24/2023

## Performance on Validation Plan

The validation plan was mostly completed. The simulations yielded positive results and proved the designs were valid. The PCB tests were somewhat positive, although there were a few failures which are further explained in the subsystem reports. A few validation tests, namely all the radiation ones, will be moved to next semester.

# Radiation Resilient Logic Circuit Study with Wide Bandgap Devices

## Nia Baireddy, Kaylee Choate, Nomar Lebron

## **SUBSYSTEM REPORTS**

REVISION – Draft  
25 January 2018

SUBSYSTEM REPORTS  
FOR  
Radiation Resilient Logic Circuit Study based on WBG  
Devices

**PREPARED BY:**

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**Author** \_\_\_\_\_ **Date** \_\_\_\_\_

**APPROVED BY:**

---

**Project Leader** \_\_\_\_\_ **Date** \_\_\_\_\_

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John Lusher II, P.E. Date

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T/A Date

## Change Record

Rev.	Date	Originator	Approvals	Description
1	12/2/2023	Nia Baireddy, Kaylee Choate, Nomar Lebron		Final Release

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## 1. Introduction

The scope of this project is to design and build a singular logic circuit that will be able to maintain its functionality in the presence of radiation. The logic circuit will consist of three distinct logic circuits – a seven-stage ring oscillator, a 1x4 SRAM array, and a 4:1 multiplexor, which will be interconnected to construct the final circuit. The interconnection of these circuits are as follows: The seven-stage ring oscillator will provide a clock signal to the 1x4 SRAM array. The SRAM uses the clock signal to write data to each of its four cells. Each cell is connected to one of the four inputs of the 4:1 multiplexor, and the multiplexor selects which of the four SRAM array cells to set as the final output of the circuit. In order for this final design to be accomplished, the three individual logic circuits must be designed, built, and tested to ensure functionality, with each circuit focusing on incorporating radiation hardening by design techniques to maximize resiliency to radiation exposure. The three individual logic circuits are the focus of this document, as it is crucial to ensure correct operation as well as radiation resilience of each individual circuit before integrating them to construct the final circuit.

The incorporation of radiation hardening by design choices is crucial to ensuring that the circuits operate properly in a radiation environment. Since these circuits are all at transistor-level, the type of transistor is particularly important for radiation hardening. The main requirement given by our sponsor, Sandia National Laboratories, was that the radiation resilient circuits would use wide-bandgap material, as they are more resilient than typical silicon or metal-oxide transistors. Within the category of wide bandgap, gallium nitride (GaN) is proven to be more radiation resilient than silicon carbide (SiC) due to the higher intrinsic resistance due to the bonding of the GaN atoms. After searching for GaN transistors, the 2306 model from Efficient Power Conversion (EPC) was chosen for its large drain to source voltage of 100V and 197A pulsed drain current. These parameters allow for a larger margin of current or voltage available for the radiation to affect before causing significant damage to the circuit. These transistors are also small surface mount devices which allows for a smaller PCB and reduced area available for radiation to affect. The other circuit elements, resistors and capacitors, were also chosen with radiation hardening in mind. High power wire wound resistors were proven to be radiation resilient over thick and thin film resistors, and they are specifically high power because of the intentionally high current and wide traces included in the circuit design. The capacitors are made of multi-layer ceramic because that material has been proven to be radiation resilient and they are more commercially available. Two circuits use mechanical switches which replace additional transistors and electrical components that would be affected by radiation.

All these radiation hardening by design choices result in circuits that have been significantly altered from their generic counterparts, so it is necessary to simulate radiation effects on these circuits to determine if these changes are effective. Two types of radiation events that could be simulated are Single Event Upsets (SEU) and Total Ionizing Dose (TID). The SEU is equivalent to a voltage or current pulse that mimics a brief pulse of radiation that could disrupt circuit behavior. The TID is equivalent to a buildup of charge, either a prolonged voltage injection or a ramped up current injection, that mimics radiation dosage over a prolonged period. These simulations of radiation provide some insight into the effectiveness of the radiation hardening by design choices implemented in these three circuits.

## 2. Ring Oscillator Subsystem Report

### 2.1. Subsystem Introduction

The primary function of the ring oscillator is to generate an oscillating square wave output signal at a desired frequency and magnitude while being exposed to a radiation environment. The target output frequency for the ring oscillator is 100kHz. The magnitude of the oscillations should have a low value of 0V and a high value that matches the input voltage supply, which is 5V. The operation of this subsystem is crucial, as it provides a clock signal as an input for the SRAM memory cell. Radiation hardening by design techniques are incorporated into the ring oscillator design to ensure performance in a radiation harsh environment.

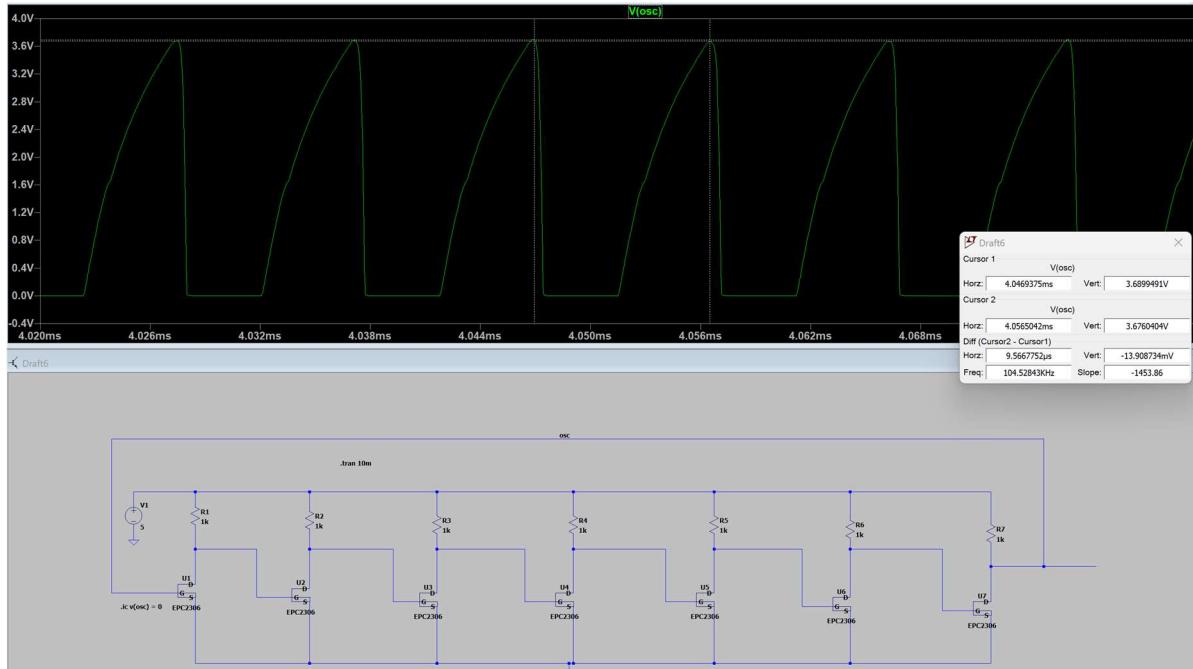
### 2.2. Subsystem Details

The configuration of a ring oscillator requires an odd number of inverters arranged in a ring, with a feedback connection from the output to the first input pin. An odd number of inverters is essential for proper ring oscillator operation. As each inverter inverts its' input signal, an odd number of inverters results in the output of the ring oscillator having a magnitude which is opposite from the oscillator's input. This, when integrated into the feedback loop, provides oscillations. The choice of number of odd inverters can be determined based on the circuit's desired function, as a larger number of inverters provides more delay to the circuit, resulting in lower output frequencies. Since the target output frequency for the ring oscillator is 100kHz, the number of inverters for the ring oscillator subsystem was chosen to be seven. This number provides a balance between a smaller number of stages such as 3 or 5, which would result in excessively high frequencies, and larger stages such as 9 and above, which contribute to a more complex design, requiring more PCB space. Additionally, larger circuits become more difficult to test in radiation environments.

The general design of a seven-stage ring oscillator includes one NMOS and one PMOS transistor per inverter. Initially, this design was simulated in LTspice to obtain baseline output waveforms for the ring oscillator and ensure proper operation. Once the general design was verified, changes to incorporate radiation resilience were made. As mentioned, Gallium Nitride (GaN) was chosen as the material for the transistors because of its wide band gap, which contributes to its enhanced performance in the presence of radiation. However, PMOS transistors made of GaN material are not commercially available, requiring the circuit to be built using only NMOS transistors. To compensate for this, pull-up resistors were used in place of the PMOS transistors for each inverter stage. The value of this resistance is crucial for the design of the inverter. A resistance value that is too small will result in a larger current which will be pulled straight to ground, preventing the signal from being inverted. Before deciding on a specific resistor value, a large resistance was simulated in place of the PMOS transistor to verify that the circuit

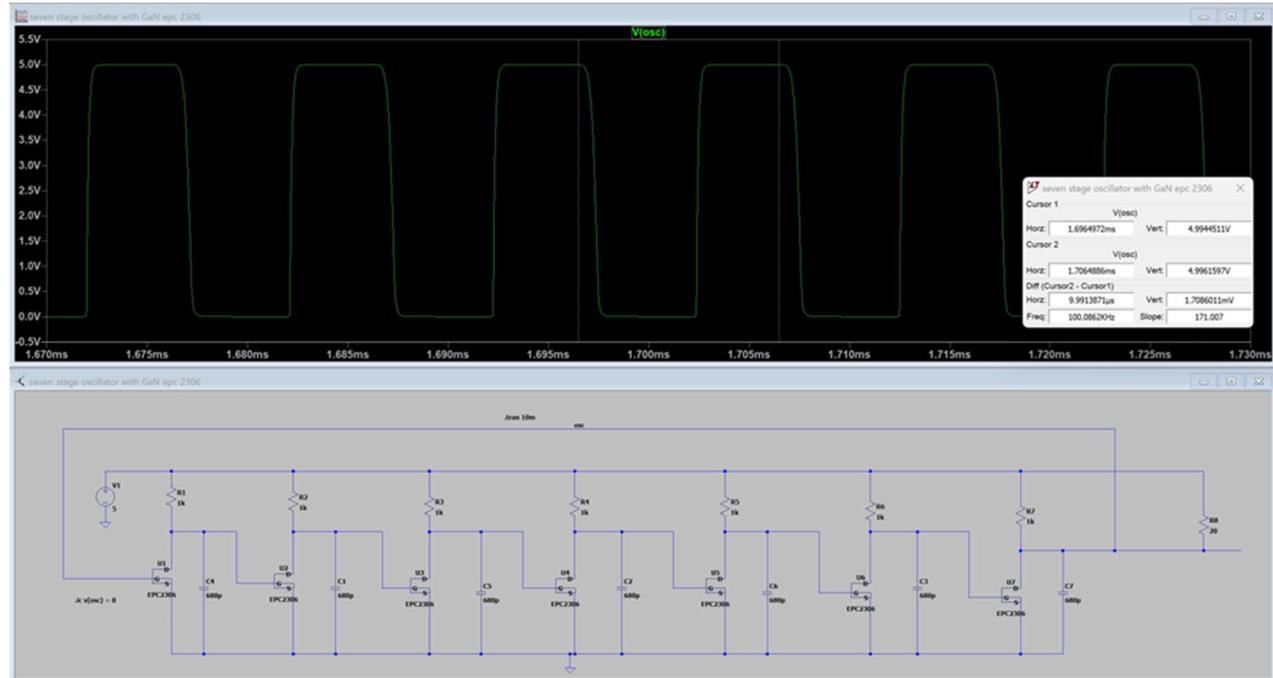
would maintain expected operation following this design change before introducing any further adjustments. Once confirmed that replacing the PMOS transistor with a pull-up resistor was successful, the standard NMOS transistor in the simulation software was replaced with the specific NMOS transistor that was chosen for the project, which was the GaN EPC 2306 transistor. After the addition of this transistor, it was now time to decide the specific value of the pull-up resistors to be used for the circuit. As mentioned previously, it is important that this resistance value is not too small, to allow for signal inversion. It may seem obvious to choose a very large resistance to ensure signal inversion. However, as the value of the resistance increases, the current through the resistor decreases, and smaller values of current are more susceptible to be affected by radiation. Therefore, it is wise to choose a resistance value large enough to allow the signal to be inverted, but not too large to where the current is at risk to be disrupted in the presence of radiation. By testing a single inverter stage in LTspice, it was determined that the minimum resistance value that will allow signal inversion in conjunction with the GaN EPC 2306 transistor was 850 ohms. In the seven-stage circuit design, a 1000 ohm resistance was chosen to provide an adequate threshold for inversion.

The LTspice simulation in Figure 1 shows the output of the seven-stage ring oscillator after the implementation of the pull up resistors and GaN EPC 2306 transistors. The original output frequency was 104.53kHz, which is very close to the target value of 100kHz.



**Figure 1: Output of ring oscillator with pull-up resistor and GaN transistor EPC 2306**

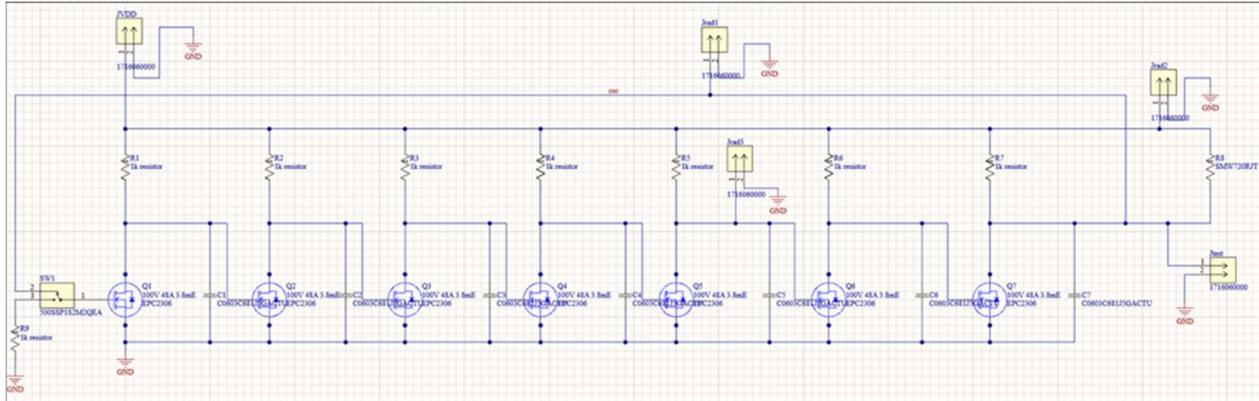
As illustrated above, the initial output waveform exhibits a shape which is more triangular than square, and the voltage high of the output is 3.78V, instead of the desired value of 5V. To address these issues, a 20 ohm resistor was added after the last inverter to serve as a buffer for the circuit. The addition of the buffer resulted in a frequency of 116kHz, so 680pF capacitors were added after the output of each stage to add further delay to the circuit, reducing the output frequency to the desired value of 100kHz. The resulting output after the addition of the buffer and capacitors is shown in Figure 2.



**Figure 2: Output of ring oscillator after addition of buffer and capacitors**

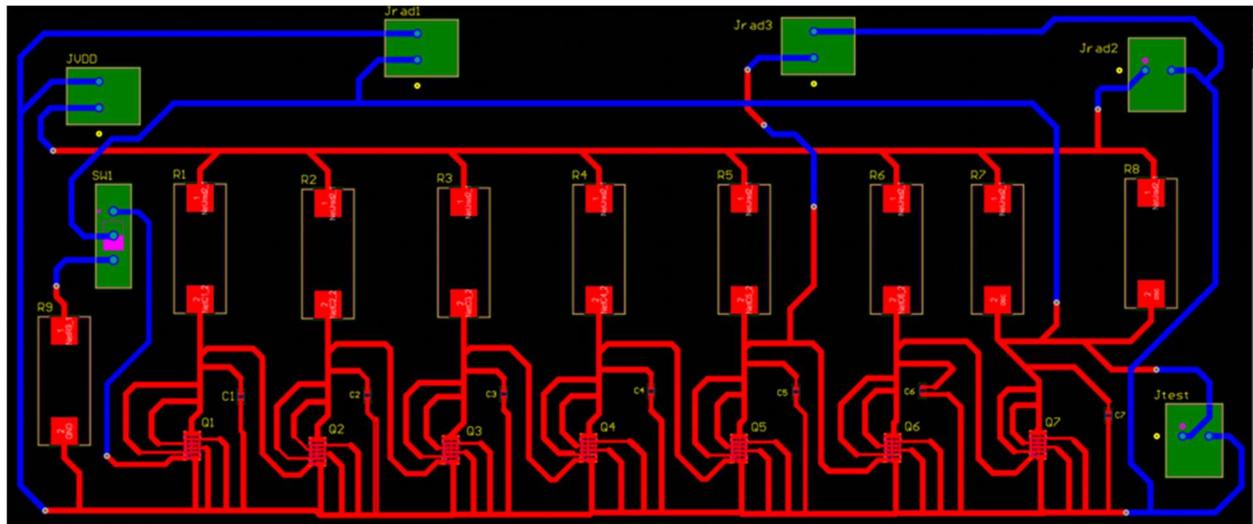
The resulting output waveform is now a square wave, with a voltage low of 0V, a voltage high of 5V, and a frequency of 100.086kHz.

Next, a PCB design was created for the schematic. For the simulations, the initial condition of 0V was able to be provided through a command line in the LTspice software. However, for the PCB design, a pull-down resistor of 1000 ohm was connected to the first input pin to provide the initial condition of 0V. A SPDT switch was added to allow the input pin to switch between initialization and closed loop operation. These changes can be seen in the Altium Designer PCB schematic, shown in Figure 3.



**Figure 3: Ring oscillator Altium Designer PCB schematic**

The ring oscillator PCB design is shown in Figure 4. As mentioned previously, a number of radiation hardening by design choices are incorporated into this design such as GaN transistors, wirewound/high power resistors, ceramic capacitors, large current throughout the circuit, PCB trace width, and spacing between traces. Terminal blocks JVDD and Jtest were added to supply power to the circuit, and to measure the output of the circuit. The terminal blocks labeled Jrad 1,2 and 3 will be used to simulate radiation effects on the circuit in ECEN 404 and analyze how the circuit responds to these effects.



**Figure 4: Ring Oscillator Altium Designer PCB Design**

### 2.3. Subsystem Validation

Upon receiving the physical printed circuit board for the ring oscillator, it was first validated by ensuring that after flipping the switch from initialization to the feedback loop, the circuit would produce square wave oscillations. As seen in Figure 5, the output waveform of the ring oscillator is an oscillating square wave. After validating the general shape of the output waveform, oscilloscope cursors were used to take measurements for the frequency and magnitude of the oscillations, as shown in Figure 6. In the process of adjusting the view

of the oscilloscope to take these measurements, the view of the oscilloscope became less scaled compared to that of Figure 5. However, both of screenshots were taken during the same test period, and both are the exact same output of the ring oscillator, just scaled differently. As seen in the top right corner of Figure 6, the output voltage high of the oscillations was 5.04V, and the output voltage low of the oscillations was 0V, which align with the expected values. The measurement for the output frequency was 89.57kHz, and is shown in the middle/bottom of Figure 6.

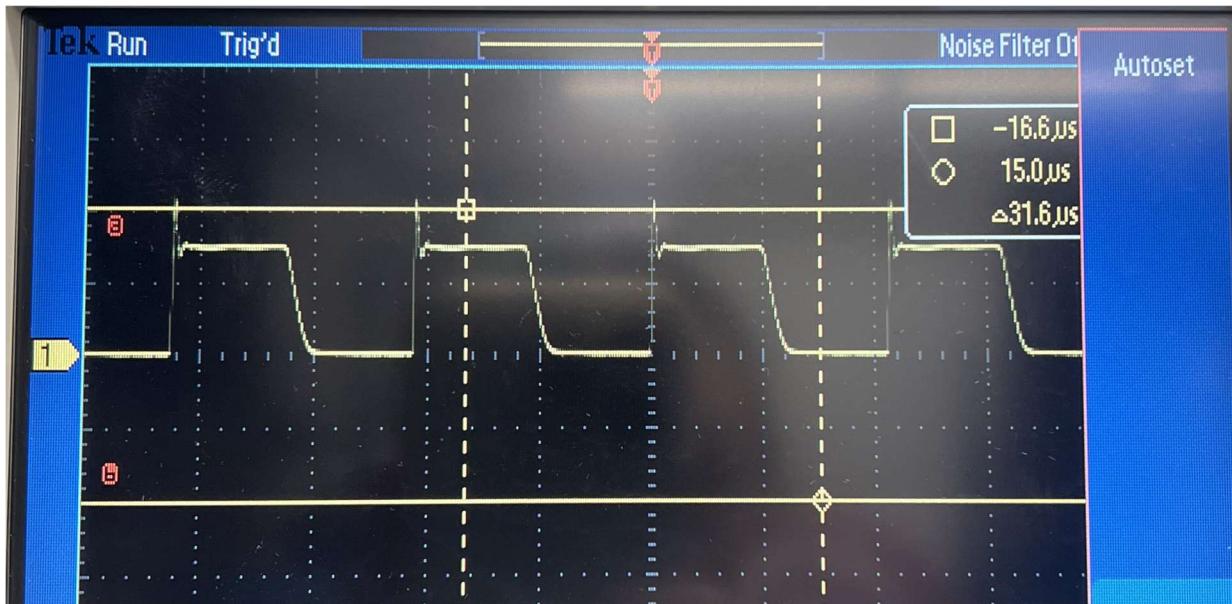


Figure 5: Square Wave Output of Ring Oscillator



**Figure 6: Ring Oscillator Frequency and Magnitude Measurements**

The ring oscillator is expected to be a radiation resilient logic circuit. So testing the circuit's response to radiation exposure is a crucial part of verifying the functionality of the circuit. When simulating radiation on the circuit, we are observing if any discrepancies occur in response to radiation effects, and if so, we will observe whether these discrepancies are detrimental to the functionality of the circuit.

Although the integration of the ring oscillator, SRAM, and multiplexor will be tested in a radiation environment at the end of ECEN 404, it is not feasible to test the individual circuits in a radiation environment prior to this. However, radiation effects were able to be simulated using certain techniques in LTspice. Two types of radiation exposure were simulated on the circuit. The first type of radiation was an instantaneous heavy dose of radiation such as a photon, which was simulated by introducing a large spike of charge into the circuit. A voltage spike of 50V is injected into the circuit in Figure 7, and a current spike of 5A is injected into the in Figure 8. Both of these spikes were introduced to the circuit at a time of 5ms. As seen in Figure 7 and 8, the outputs at 5ms did not have any discrepancies due to the spike in charge.

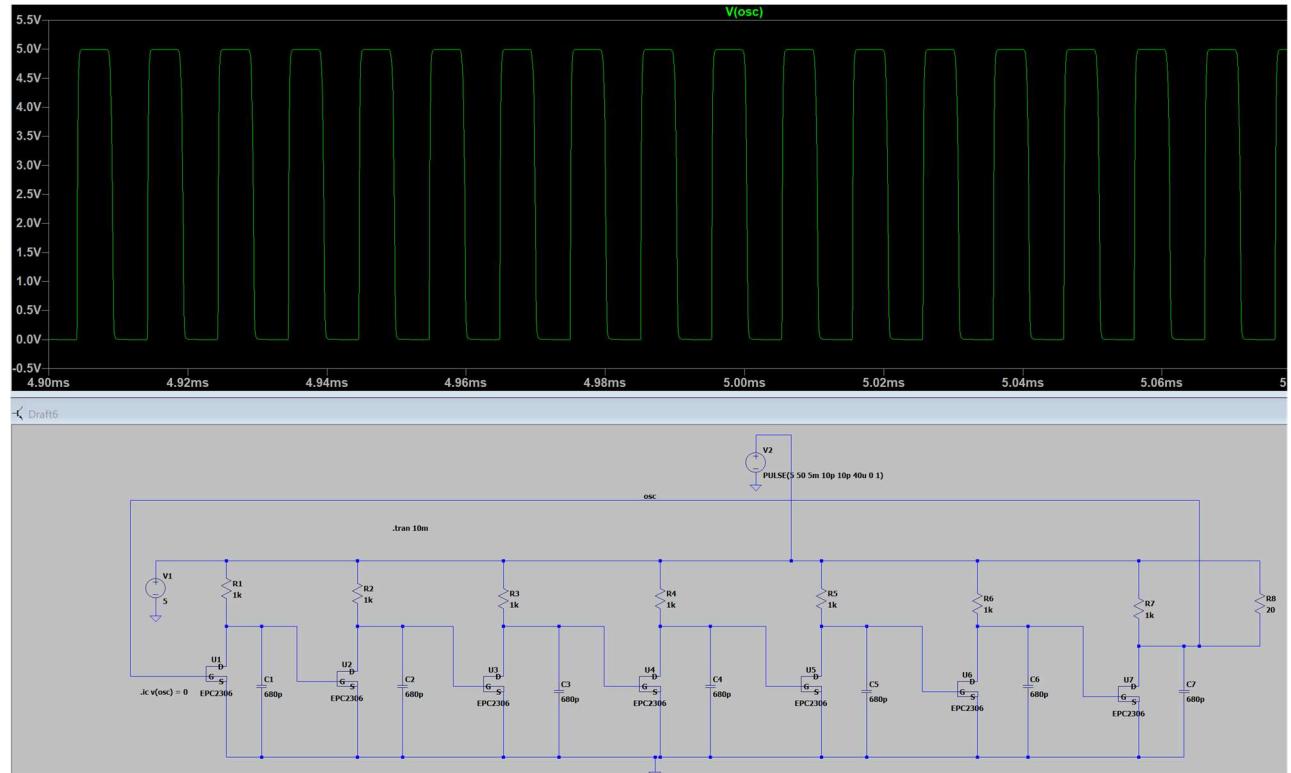


Figure 7: Radiation Simulation with 50V spike

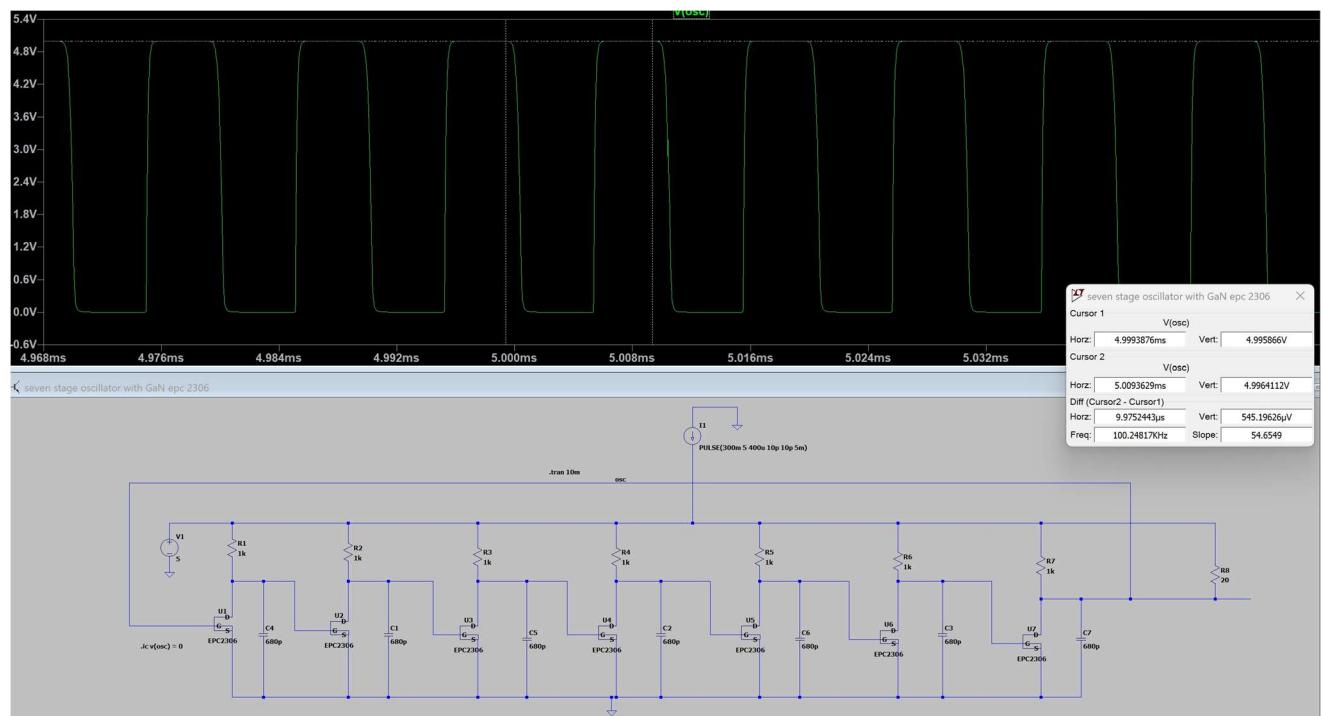
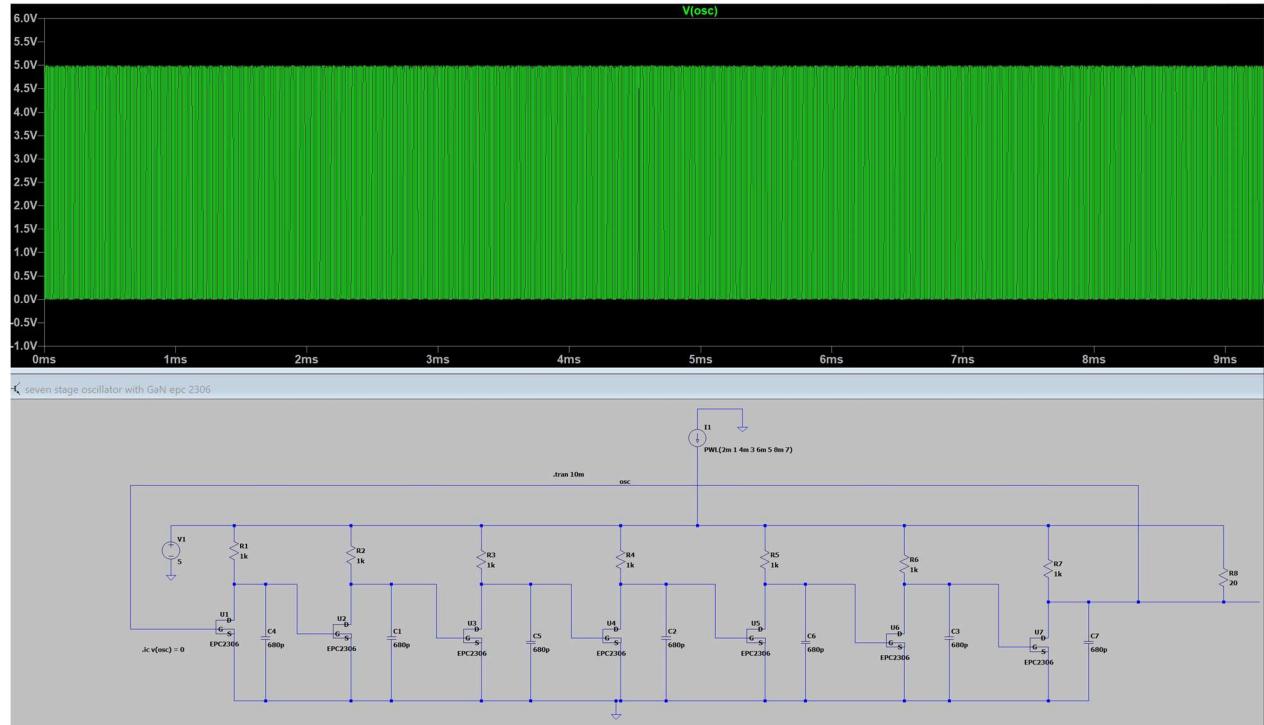
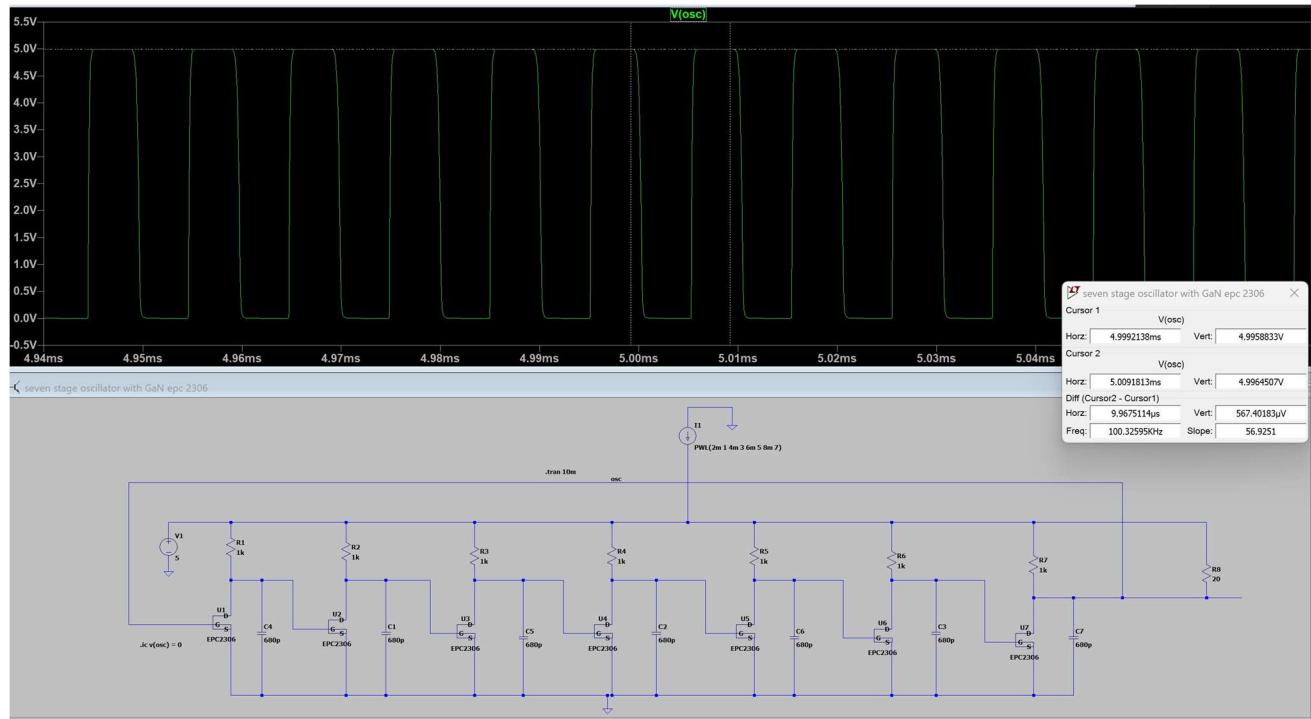


Figure 8: Radiation Simulation with 5A spike

The second type of radiation simulated on the circuit was a buildup of charge over time. This was implemented by gradually increasing the current applied to the circuit in the span of 0-10ms. A current buildup of 500mA-5A was applied to the circuit. Since this buildup occurred over the entire simulation run time, the full output is shown in Figure 9 to illustrate no discrepancies in the magnitude of the output waveform. Furthermore, a zoomed in version of the circuit during the buildup of current is shown in Figure 11. Here it can be seen that no disruptions of frequency occurred due to the buildup of charge.



**Figure 9: Injection of a 500mA-5A charge build up (zoomed out)**



**Figure 10: Injection of a 500mA – 5A charge build up (zoomed in)**

## 2.4. Subsystem Conclusion

In conclusion, a variety of radiation hardening by design techniques were incorporated into the circuit design of the seven-stage ring oscillator to enhance its performance in the presence of radiation. The ring oscillator was designed, simulated, assembled, and tested to ensure proper functionality. It was determined that the seven-stage ring oscillator operates as expected and produces an oscillating square wave output, which will serve as a clock signal for the SRAM memory cell. The output waveform of the ring oscillator also exhibits stability by maintaining a consistent shape, frequency, and magnitude during extensive run time. The magnitude of the output waveforms align with the expected and simulated values, with a voltage high of 5.04V and a voltage low of 0V. The output frequency of the ring oscillator is 89.57kHz, which is slightly lower than the simulated value due to variances between ideal simulations and real-world conditions. This however, is an acceptable frequency, as 100kHz was given as a target value instead of a harsh requirement for functionality. Before integration of subsystems, the frequency can be made closer to the target value by adjusting the value of capacitance. It can also be seen that the output waveform exhibits slight ringing at the beginning of each voltage high. This is due to the presence of impedance in the circuit and can be smoothed by adding an RC snubber to the circuit before integrating the subsystems in the final design.

## 3. SRAM Memory Cell Array Subsystem Report

### 3.1. Subsystem Introduction

The 1x4 SRAM memory cell array is the central subsystem of the project. It uses the output of the seven stage ring oscillator as a clock to write to each of the four cells, and those four cells are connected to the four inputs of the 4:1 multiplexer. This SRAM array is designed to be radiation resilient such that a radiation event would not result in the loss of data stored in the cells, and all design choices were made with that criterion in mind. The typical behavior of the circuit was simulated in LTSpice, with the EPC2306 GaN FET model as the transistor, and any required modifications to resistor and capacitor values were made to ensure the circuit behaved properly according to the desired power and voltage specifications. The entire circuit was then realized on a PCB using Altium Designer and assembled in lab before bench testing was conducted. The SRAM array was operational, although the results of the bench testing did yield some discrepancies with the simulated data. The schematics, PCB design, testing data, and further solutions are all detailed in the following subsections.

### 3.2. Subsystem Details

A 1x4 SRAM cell array was chosen because it was complex enough to truly test the effectiveness of the design, but still simple enough to design, build, and test in the given timeframe. The SRAM memory cell stores data such that the output yields either a logic LOW or a logic HIGH value. Each cell of the SRAM array consists of two cross-coupled inverters with access transistors connected at the drain terminals of each inverter to provide access to the bitlines and wordline. In this particular array of 1x4, four memory cells are connected in a row via the wordline, and they each have their own pair of non-inverting and inverting bitlines that allow read and write access. Non-inverting and inverting write circuits connect to their respective bitlines to allow data to be written to the cell, though only one cell can be written to at a time. The array also requires each cell to be connected to a sense amplifier in order to amplify the output signal of the cell to a value significant enough to be properly read. The final schematic of the SRAM memory cell array, sense amplifiers, and write circuits are shown in the figures below.

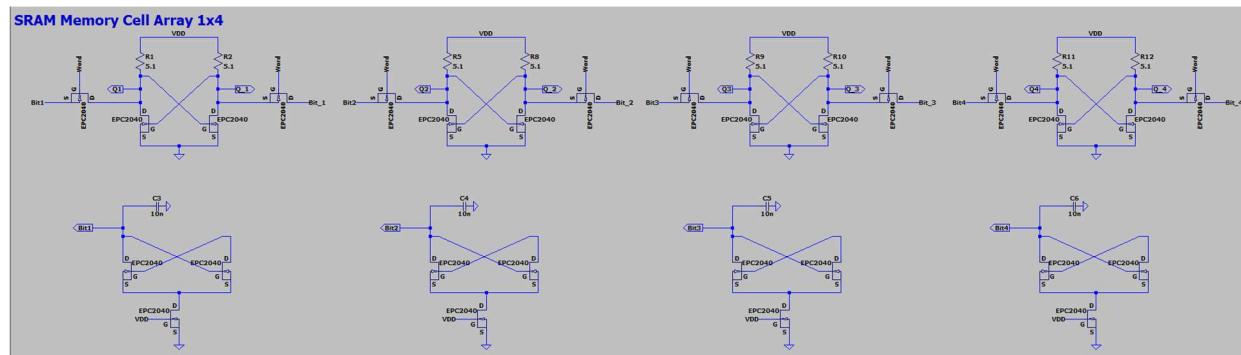
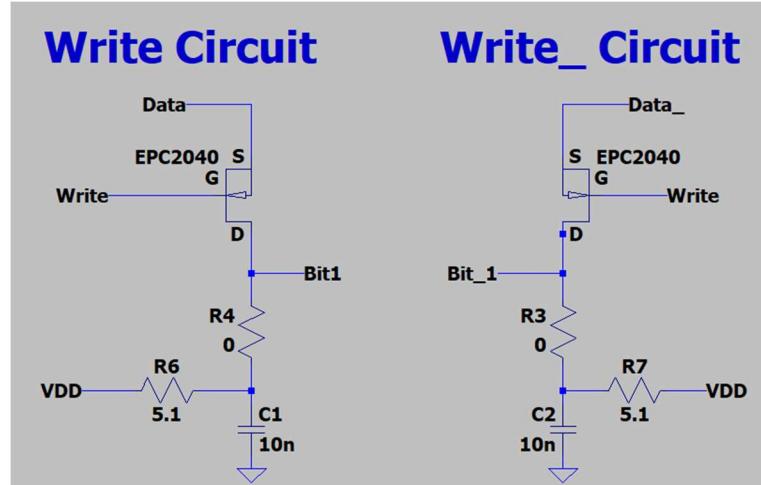


Figure 11: 1x4 SRAM Memory Cell Array with Sense Amplifiers



**Figure 12: Non-Inverting and Inverting Write Circuits**

Typical SRAM cells have a CMOS configuration for their inverters, a PMOS connected to an NMOS via the drain terminals. Their sense amplifiers also use cross-coupled CMOS inverters along with additional NMOS and PMOS transistors. The write circuit pairs use an NMOS for bitline write operations and a PMOS for precharging those bitlines for read operations. However, wide bandgap transistors are only manufactured as NMOS, so the entire circuit had to be realized in NMOS only. As seen in the schematics, only NMOS FETs are used, and where PMOS would typically be, resistors are used instead. The sense amplifiers are the only subcircuits not using resistors, as an alternative NMOS-only configuration with just a capacitor already exists and was deemed effective during simulation.

The radiation resiliency of the SRAM memory cell array was the primary requirement given by our sponsor, Sandia National Laboratories. To accommodate that parameter, radiation hardening by design techniques were implemented. Transistors with wide bandgap materials have proven to be better at handling radiation than traditional silicon, and gallium nitride (GaN) specifically is the most optimal wide bandgap material as opposed to silicon carbide (SiC). As a result, the transistors used in the SRAM memory cell array are EPC2306 GaN FETs. The resistors used in the inverters and write circuits are wire wound high power resistors to achieve the goal of high circuit current, which is another way to resist radiation effects. The capacitors for the sense amplifiers were multi-layer ceramic capacitors, as they are effective enough in radiation and have the most commercially available variety of values. The PCB layout of the final design is shown below.

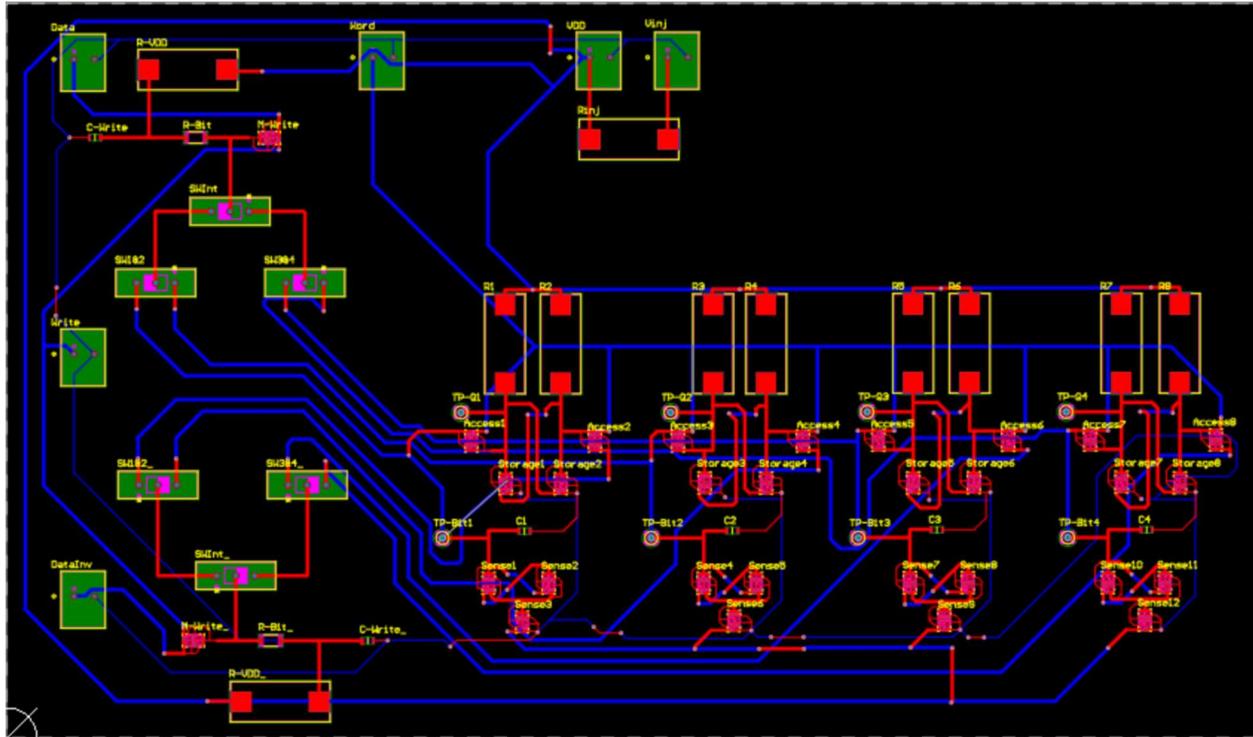


Figure 13: PCB Layout of SRAM Memory Cell Array

The four SRAM cells are clearly shown on the right side of the layout. The write circuits are shown to the left, and each circuit is attached to a set of mechanical switches that allow manual switching between cells during write operations. The terminal blocks shown are for AC and DC voltage signal inputs throughout the circuit. The **VDD** is the DC power supply for the write circuits and the SRAM cells. The **Data** and **DataInv** blocks are the initial DC signals fed to the non-inverting and inverting write circuits respectively. The **Write** and **Word** are AC signals that turn the write circuits and wordline respectively on and off according to a specific frequency and duty cycle. As the seven-stage ring oscillator is the intended clock for this circuit, both AC signal inputs are given a frequency of 100kHz to match the oscillator's expected output and ensure that the SRAM circuit works with said frequency.

### 3.3. Subsystem Validation

Given all the modifications that the circuit went through to become a radiation resilient version of its generic counterpart, various simulations were run in LTSpice to ensure the circuit operated as expected.

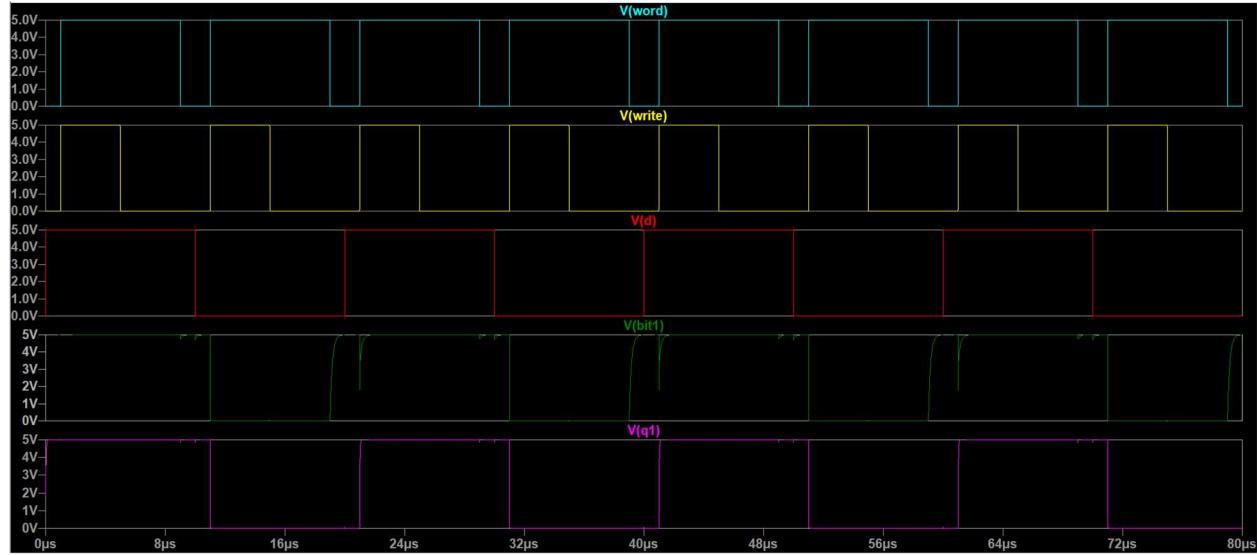


Figure 14: SRAM Array Simulation Output

This simulation shows the typical behavior of the GaN SRAM memory cell array. The Data, Word, and Write signals are such that the data is being written before the wordline turns on, and then the write circuit is turned on then off while the wordline is still on. This ensures that the data is completely written to the cell before access is closed. The output of the cell is Q1, and the connection to the associated sense amplifier is Bit1. Q1 and Bit1 are essentially the same signal, so the inclusion of Bit1 is just a redundant check. If the SRAM cell is working as intended, the Q1 and Data signals should have the same shape and frequency. As seen in the simulation waveform output, that is the case, although Q1 lags behind Data by a few microseconds. This delay is acceptable as it is the delay of the switching, since it cannot be instantaneous due to all the circuit elements requiring time to change states.

Radiation effects were also simulated in LTSpice. Two types of radiation effects were tested, a Single Event Upset (SEU) and a Total Ionizing Dose (TID). The SEU was simulated by adding a pulse to VDD that dropped the overall VDD in an attempt to disrupt the power to the SRAM cells intermittently. The TID, which can be mimicked by a build-up of charge, was caused by introducing a PWL current source to VDD that gradually increased current input over time. The results of both simulations are in the two figures below.

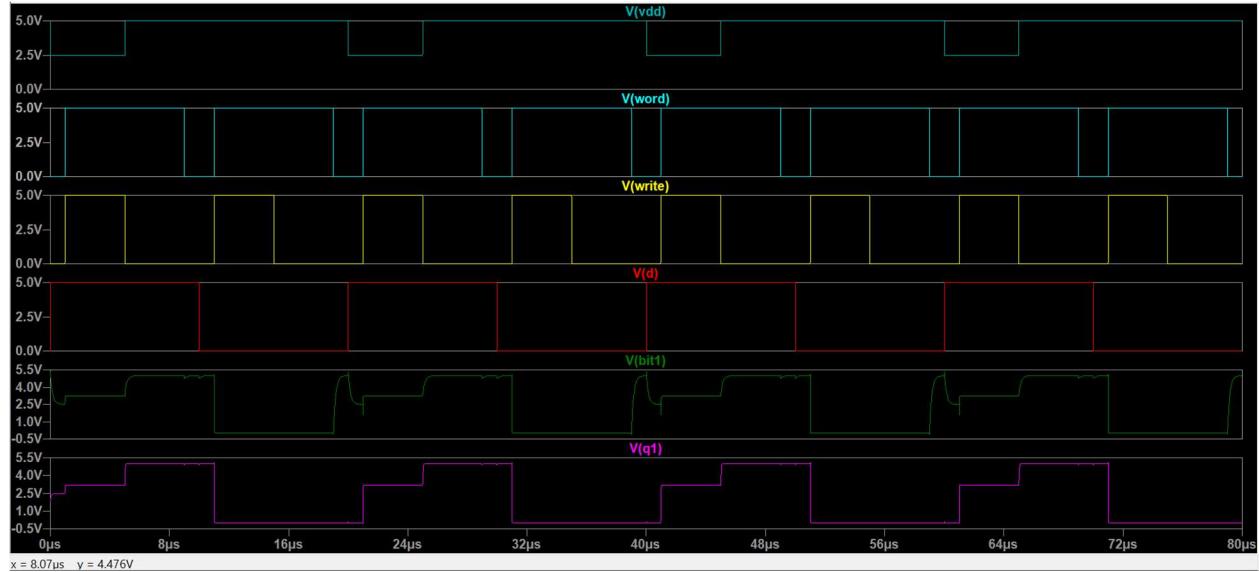


Figure 15: Single Event Upset Simulation

The Q1 signal is seen here to have a slight step at about 3V when switching from a low of 0V to a high of 5V, due to the reduced supply voltage caused by the “SEU”. However, the signal does recover and that lower value in the step could still be considered a logic HIGH. This is because the maximum gate to source voltage of the FET is 2.5V, so the inverter FETs would still conduct. Therefore, with this simulated effect of radiation, the SRAM circuit is expected to still work as intended.

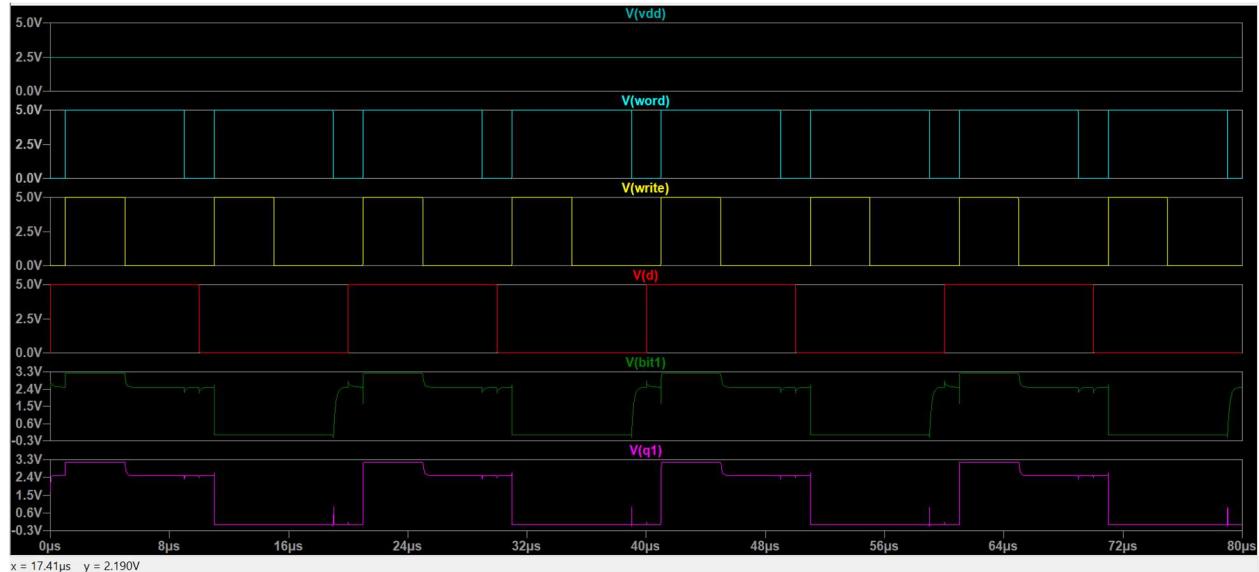


Figure 16: Total Ionizing Dose Simulation

Q1 here is seen to hit a maximum of 3.3V when the supply voltage is indefinitely reduced due to a “TID” charge build-up before stepping down slightly to about 2.5V. However, as mentioned earlier for the SEU simulation, the FET would still conduct and the high voltage here would still be considered a logic HIGH. Therefore, with this simulated effect of radiation, the SRAM circuit is expected to still work as intended.

The simulations above were all run on just one out of the four cells, as the behavior of all cells was the same in simulations.

After the PCB was received, it was assembled and set up for bench testing, as shown below.

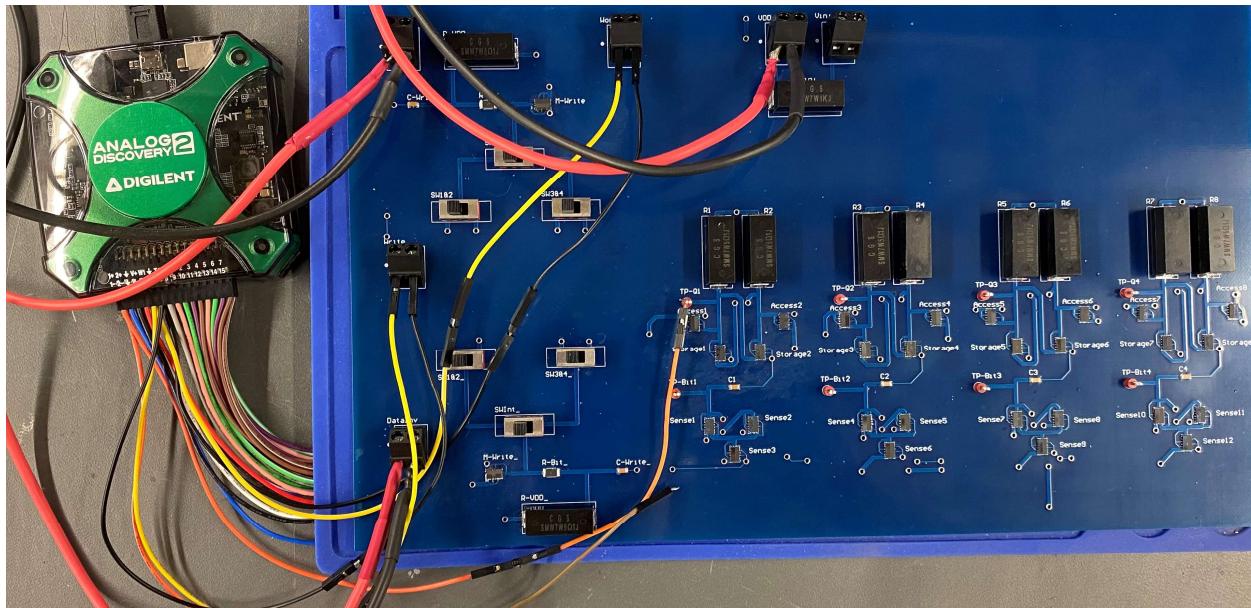


Figure 17: PCB and Bench Setup

The operation of each cell was tested as follows. After the board is powered up, the default value is logic LOW. The **Word** and **Write** signals are turned on, and then the **Data** signal is turned on to supply a high voltage to the cell's non-inverting bitline. The scope shows the output switching from LOW to HIGH, and then the Word and Write signals are turned off. The scope then shows the HIGH value latched in the cell. The **Word** and **Write** signals are turned on again, and then **DataInv** turns on to supply a high voltage to the cell's inverting bitline. That causes a logic LOW to be written to the cell, which is shown in the scope as the output switching from HIGH to LOW. Finally, the **Word** and **Write** signals are turned off and the scope shows the LOW signal latched in the cell. The scope images of these four stages of each of the four cells are shown in the figures below.

# Subsystem Reports

## Radiation Resilient Logic Circuit Study based on WBG Devices

Revision - Final

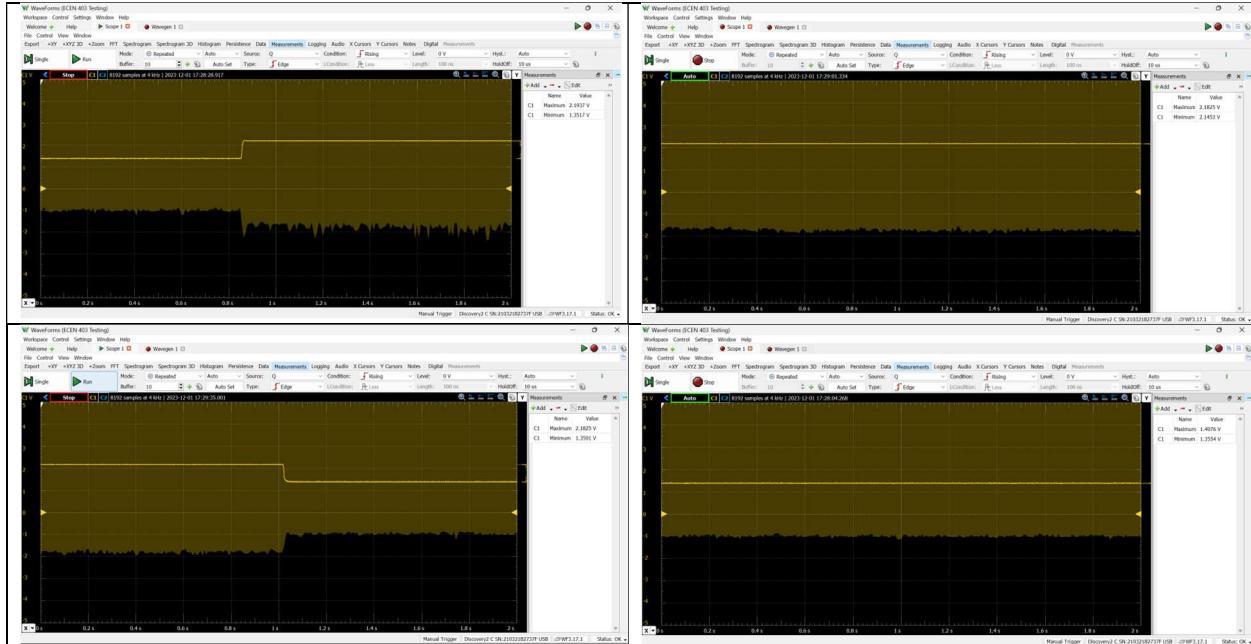


Figure 18: Cell 1 – Low-High Switching, High Latch, High-Low Switching, Low Latch

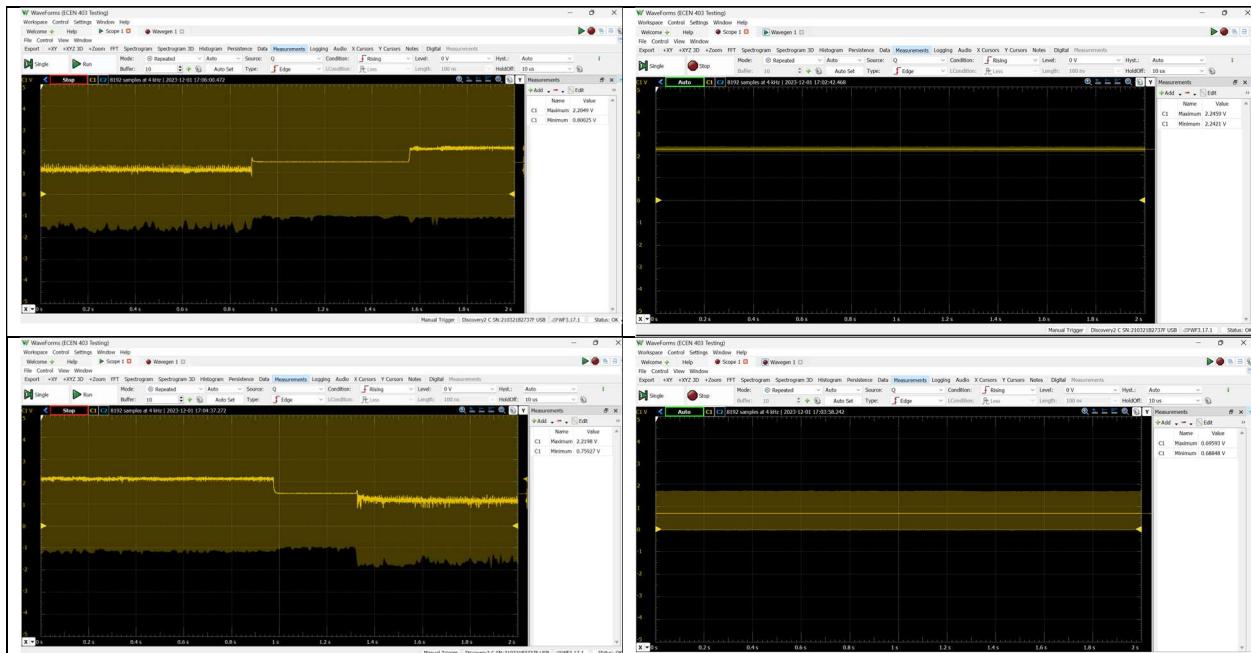
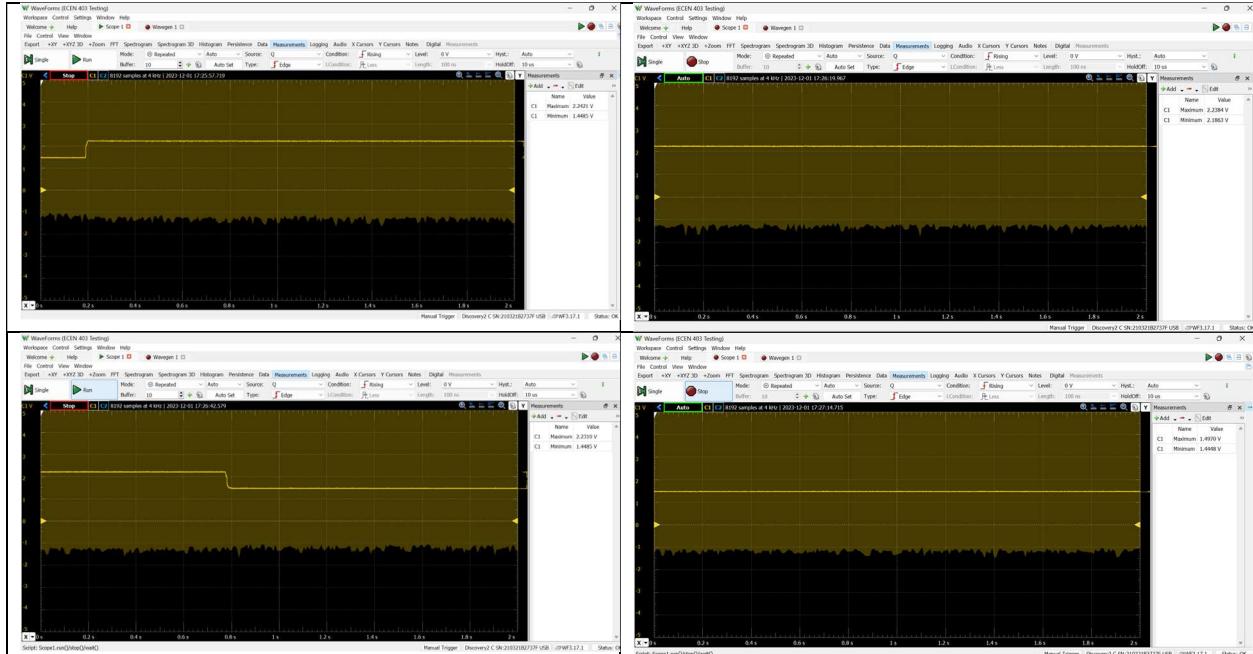


Figure 19: Cell 2 – Low-High Switching, High Latch, High-Low Switching, Low Latch

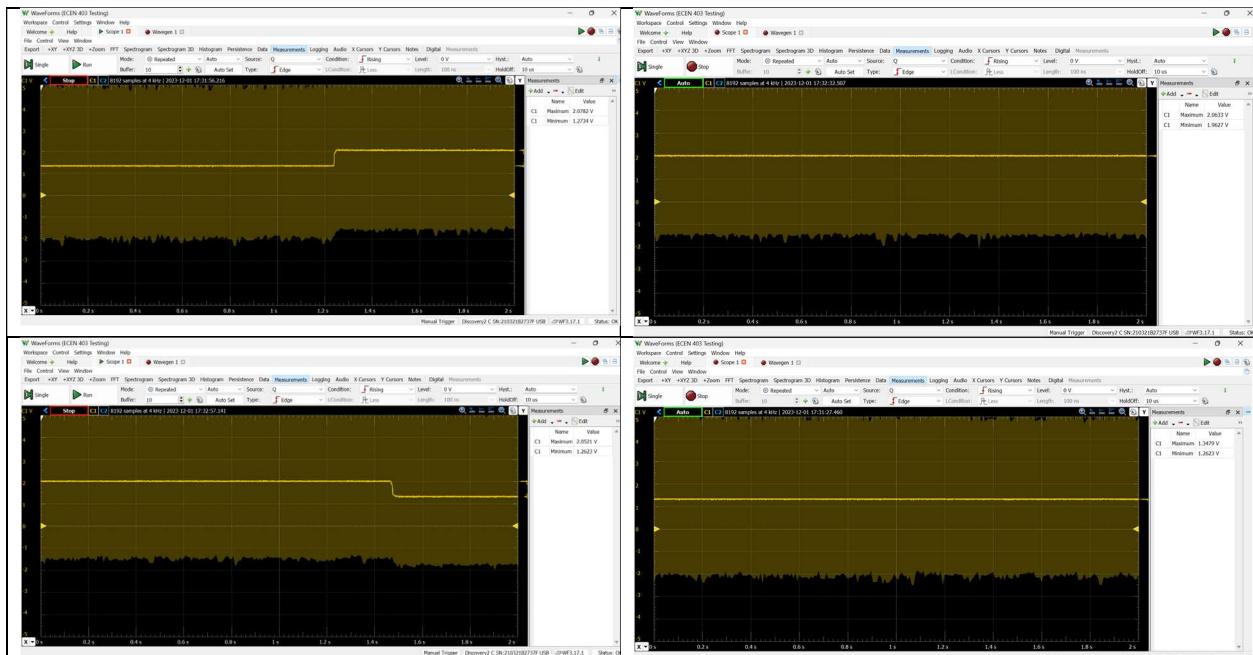
# Subsystem Reports

## Radiation Resilient Logic Circuit Study based on WBG Devices

Revision - Final



**Figure 20: Cell 3 – Low-High Switching, High Latch, High-Low Switching, Low Latch**



**Figure 21: Cell 4 – Low-High Switching, High Latch, High-Low Switching, Low Latch**

Cell	Low (V)	High (V)
1	1.355	2.194
2	0.688	2.246
3	1.444	2.238
4	1.262	2.063

**Table 1: Low and High Latch Values for All Cells**

As seen in the table above, the low and high values of the cells do not match the values from the simulations. The voltage supplied to the cell is 5V, so the assumed values for logic high and low values in the cells would be 5V and 0V respectively. However, a limitation we were given by our sponsor was that the current of the circuits could not exceed 1A, which resulted in the supply voltage being significantly lowered to about 2.5V. Since logic LOW and HIGH are user-defined, the difference between them could be as small as 1V, so this limit by itself was not a problem as HIGH is now redefined as 2.5V. The issue with the lower values not being 0V or somewhat close to it was due to an unforeseen real behavior of the GaN FETs that were not shown in the LTSpice simulations. The source terminals of some FETs in the circuit were not grounded, which can be clearly seen in the schematic. As a result, the source was somewhat “floating” and so the drain was pulled up to a value not 0V. Normally, this issue would be rectified by a PMOS, but since this is an NMOS-only design, a gate-driver or equivalent component/circuit would need to be implemented. The only true requirement for the valid operation of this circuit is that it does switch from low to high and vice versa, and then it does latch that value when access to the wordline has been closed. Therefore, the behavior shown in these simulations and bench measurements proves that the SRAM array is technically working as intended, and there are a few issues with the voltage levels that will be fixed in the next semester before integration.

### **3.4. Subsystem Conclusion**

In conclusion, various radiation hardening by design techniques were implemented in the design of the 1x4 SRAM memory cell array, and it was simulated, assembled, and verified to operate as expected. The use of wide bandgap GaN transistors, multi-layer ceramic capacitors, wire-wound resistors, mechanical switches, and wide traces resulted in a radiation hardened SRAM memory cell array that would theoretically maintain the integrity of its stored data when affected by radiation. There were a few issues encountered during bench testing where the output was not as low as intended, and this was due to the real behavior of the FET that was not shown in the simulations. Further testing showed that the reason may have been because the source of the FETs was not grounded, and there was no PMOS to mitigate the voltage of the drain being pulled up. This will be mitigated in the integrated system design next semester by implementing GaN gate drivers or equivalent circuits. In spite of this issue, the SRAM memory cell array functioned properly and will be the central subsystem of this integrated system.

## 4. 4:1 Multiplexer Subsystem Report

### 4.1. Subsystem Introduction

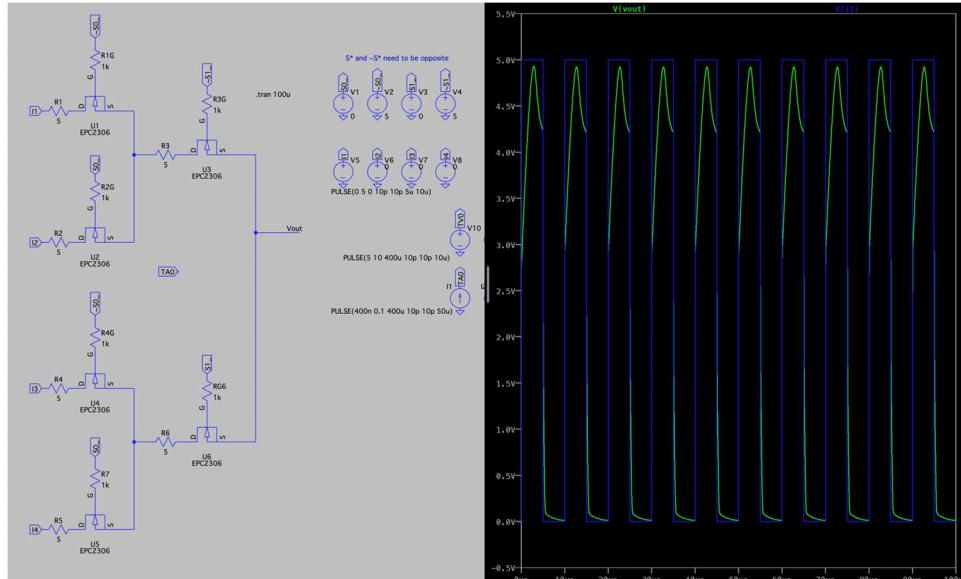
The 4:1 multiplexer has been designed to be the final output of the entire system. The 4:1 MUX has the ability to select between four independent inputs by configuring the two selection bits as necessary. These four inputs will be connected to the four cells of the 1x4 SRAM array in the final design. The 4:1 multiplexer must also be radiation resilient, the main consideration for almost all design choices. Large currents going through wire wound resistors will help mitigate the radiation effects, in addition to the wide bandgap Gallium Nitride transistors implemented in the design. The multiplexer operation and rad hardness were first verified using LTSpice simulations which included the EPC 2306 transistor model, then later realized using an Altium Designer PCB schematic. The 4:1 MUX printed circuit board was tested and verified to be operational, although some discrepancies between the simulations and measurements did emerge. Mainly, the high and low measured voltage values do not align with the simulations and fall short of the specifications. Explanations and potential solutions to this problem and more will be expanded upon in later sections.

### 4.2. Subsystem Details

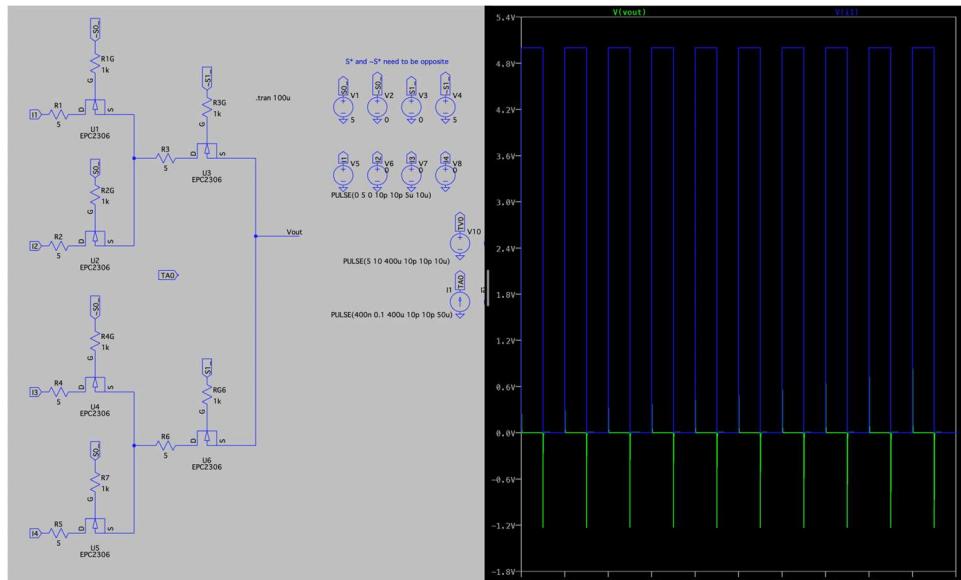
As previously mentioned, designing the 4:1 multiplexer to be as radiation resilient as possible was the main requirement given by the sponsor, Sandia National Labs. In order to accomplish this, we implemented wide bandgap (WBG) transistors which are inherently more resistant to radiation in our logic circuits. They also allow for higher temperatures, voltages, currents, and switching speeds than traditional Silicon. We decided on utilizing Gallium Nitride (GaN) as there is less research using this material than the other main option, Silicon Carbide (SiC). GaN is also better than SiC at higher frequencies which is useful for our application. The main problem with WBG transistors, however, is the inability to acquire commercially available PMOS transistors, therefore requiring us to design our circuits using only NMOS transistors. The 4:1 MUX was first designed and simulated using both NMOS and PMOS transistors to confirm operation. Research was then conducted on converting PMOS to NMOS by cleverly configuring the resistors and transistors to mimic the functionality of a PMOS. The new circuit schematic was once again simulated and tested for operation. The final circuit schematic after converting from NMOS to PMOS can be seen in Figure 22 below.

Once the circuit schematic using only NMOS transistor was complete, it was now time to decide which specific transistors would be used in order to download the LTSpice transistor model to get a more accurate representation of the circuit. We decided on using the EPC 2306 for its large drain to source voltage of 100V and 197A pulsed drain current. This allows for a large current or voltage radiation spike to reach these values before causing significant damage to the circuit. These transistors are also small surface mount devices which allows us to decrease the total size of the PCB. The manufacturer of the transistors, Efficient Power Conversion (EPC), includes both an LTSpice model and Altium Designer footprint, both of which were incredibly helpful throughout the design process. The basic NMOS transistors were replaced by the EPC 2306 transistors in the LTSpice simulation to give more realistic measurements. The values of resistors needed to be slightly adjusted after replacing the transistors, due to the different inherent characteristics. The 4:1 MUX was again tested using both a 5VDC input, as well as a 5VAC 100kHz square wave input to verify the switching operation. The final multiplexer schematic and simulations can be seen in Figures 22-25

below. These waveforms show only when 5VDC is applied to input 1, however, the same trend is followed for the other three inputs.



**Figure 22: LTSpice Simulation w/ 5VAC Applied at Input 1 (Selection Bits: 00)**



**Figure 23: LTSpice Simulation w/ 5VAC Applied at Input 1 (Selection Bits: 10)**

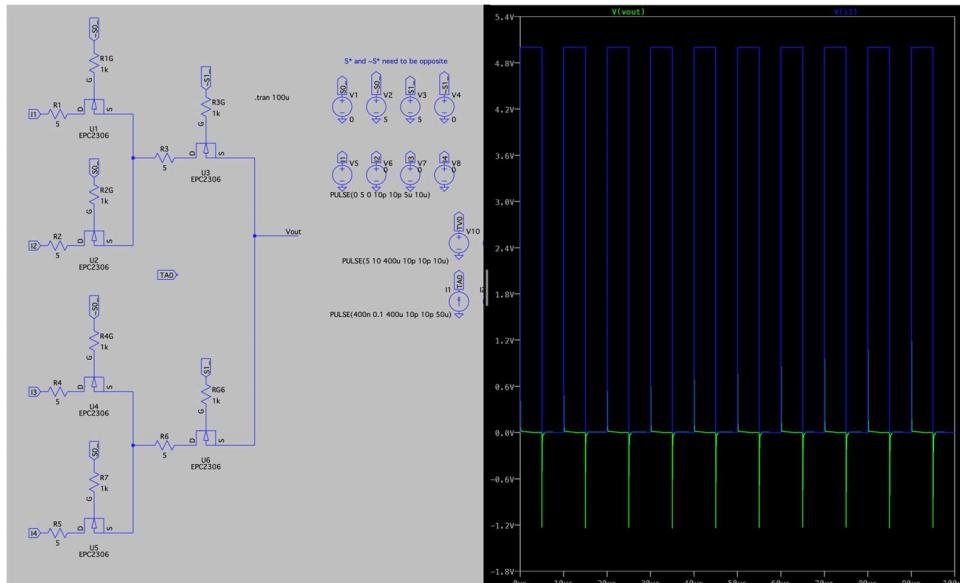


Figure 24: LTSpice Simulation w/ 5VAC Applied at Input 1 (Selection Bits: 01)

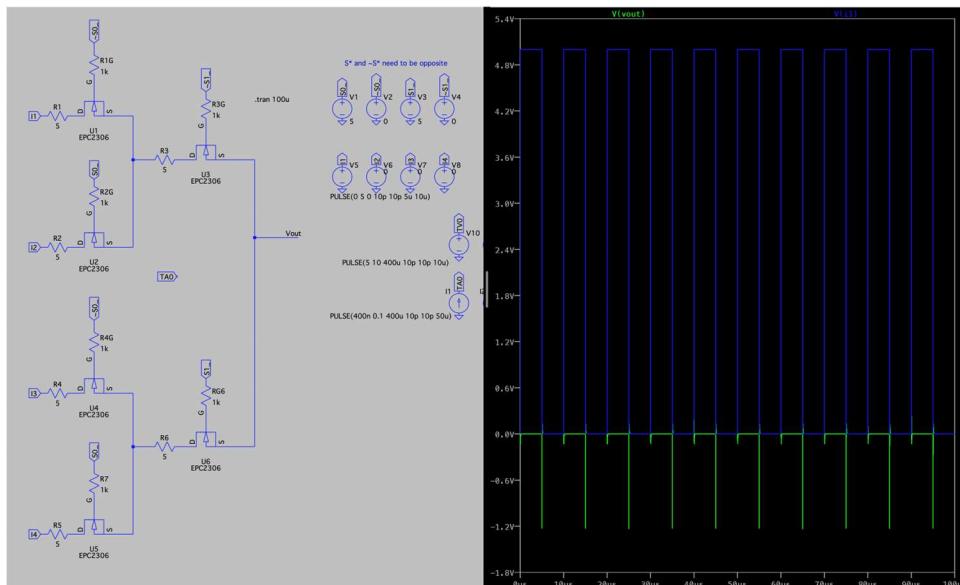
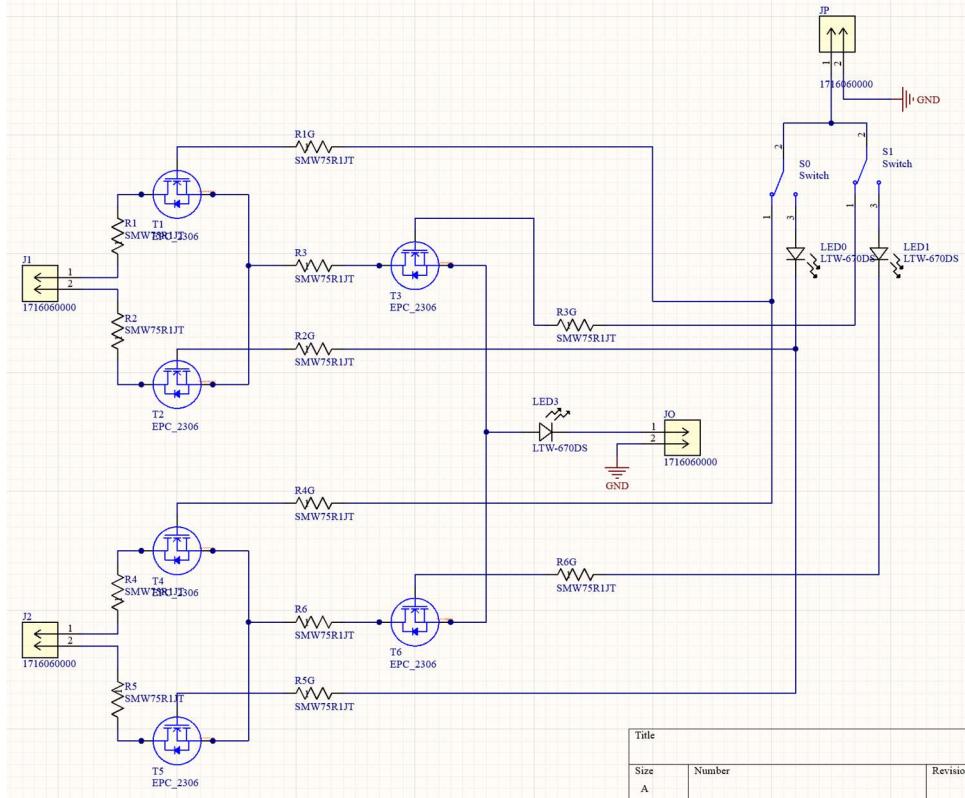


Figure 25: LTSpice Simulation w/ 5VAC Applied at Input 1 (Selection Bits: 11)

After designing and verifying the 4:1 multiplexer operation using LTSpice simulations, the next step was to realize the 4:1 MUX on a printed circuit board using Altium Designer. The conversion from simulation schematic to PCB schematic was fairly straight forward, with the main difference being the implementation of a physical mechanical switch in the PCB schematic instead of changing the selection bit values by hand as done in the simulation, which can be seen in Figure 26. The PCB schematic also includes LEDs for the user interface, however, since this voltage drop was not accounted for in the simulations, these connections have been shorted on the physical PCB and will be revisited in the final design. While making the PCB schematic, design choices such as which resistors and switches must be implemented were decided with radiation resiliency at the forefront of the decision-making process. Wire-wound resistors have been found to be inherently more radiation resilient than

the thick film resistors traditionally used. For this reason, larger wire-wound resistors capable of dissipating 7W of power were chosen for the design. This allows for a large current to flow through the system and makes the entire circuit more rad hard. The Altium footprint of these SWM7XXXJT resistors was initially difficult to solder, leading to the spacing out of the resistor pads for revision 2.



**Figure 26: 4:1 MUX Altium Designer PCB Schematic**

While the resistor pad spacing was a useful addition to revision 2, the main reason for needing a second revision was the orientation of the GaN transistor soldering pads. As can be seen in Figure 27, four out of the six transistors were mirrored in Altium Designer to allow the PCB schematic to have a similar layout to the simulation schematic. While this is possible in Altium, the physical EPC transistors are incapable of being physically mirrored and therefore did not align with the pads on the PCB. This prompted an immediate redesign of the circuit board to align all the transistor pads with the physical EPC transistor pad layout. The redesign also included reducing the spacing between the resistors to allow for a more power dense design. Lastly, revision two included radiation test points to allow for us to inject voltage and current spikes and build-ups to simulate the effects of radiation on the PCB. This radiation injection feature will be utilized for testing next semester before integrating the three systems together for final radiation testing. The changes made to Rev. 2 can be seen in Figure 28 below. This schematic is the final 4:1 MUX PCB design that was tested and verified for functionality in the next section.

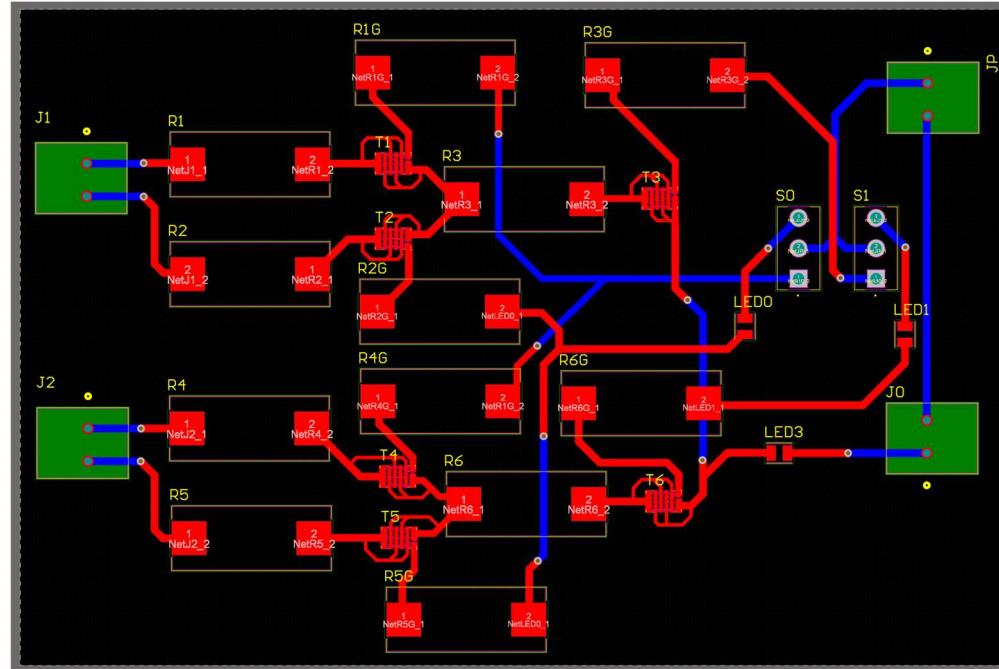


Figure 27: 4:1 MUX Altium Designer PCB Layout Revision 1

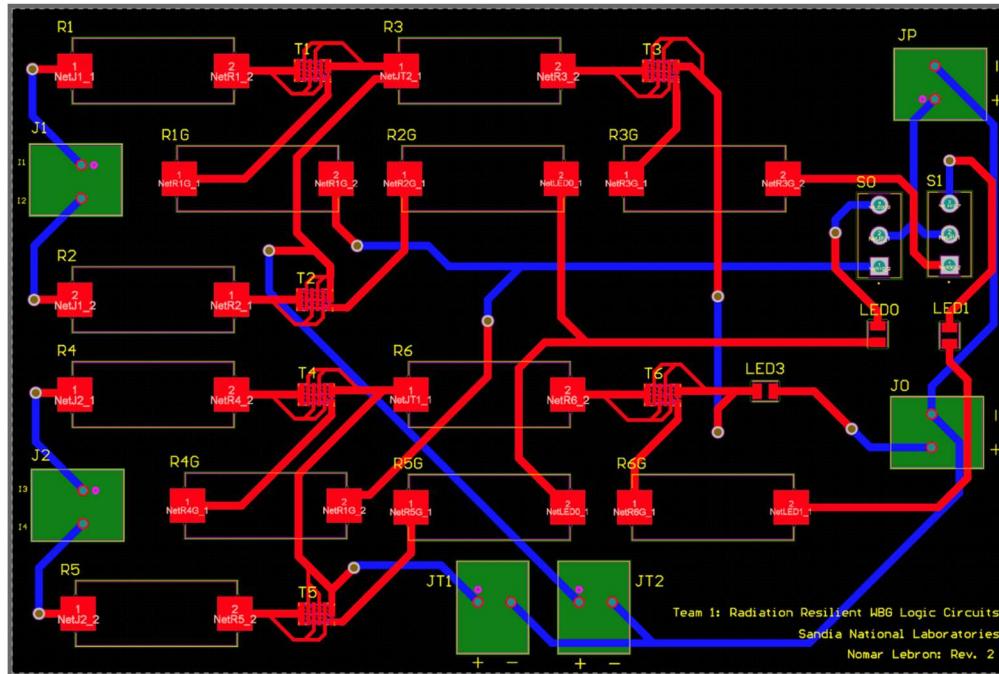


Figure 28: 4:1 MUX Altium Designer PCB Layout Revision 2

### 4.3. Subsystem Validation

Once the simulation and PCB schematics were completed, it was now time to validate the operation of the 4:1 multiplexer. The first validation test was meant to verify the overall functionality of the circuit, mainly the ability for the 4:1 MUX to switch between the four inputs. This test was conducted by inputting 5VDC to each of the inputs individually, then switching between all four selection bit configurations to measure the output voltage value. The data from this experiment can be seen in Tables 2-5 below. The output voltage is the largest when the selection bits are configured to the input that has the 5VDC applied. This data confirms that the 4:1 MUX is operating as intended.

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	5 V	0	0	3.505 V
I2	0 V	1	0	2.968 V
I3	0 V	0	1	1.731 V
I4	0 V	1	1	1.304 V

Table 2: Output Voltages when 5VDC Applied to Input 1

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.011 V
I2	5 V	1	0	3.528 V
I3	0 V	0	1	1.723 V
I4	0 V	1	1	1.305 V

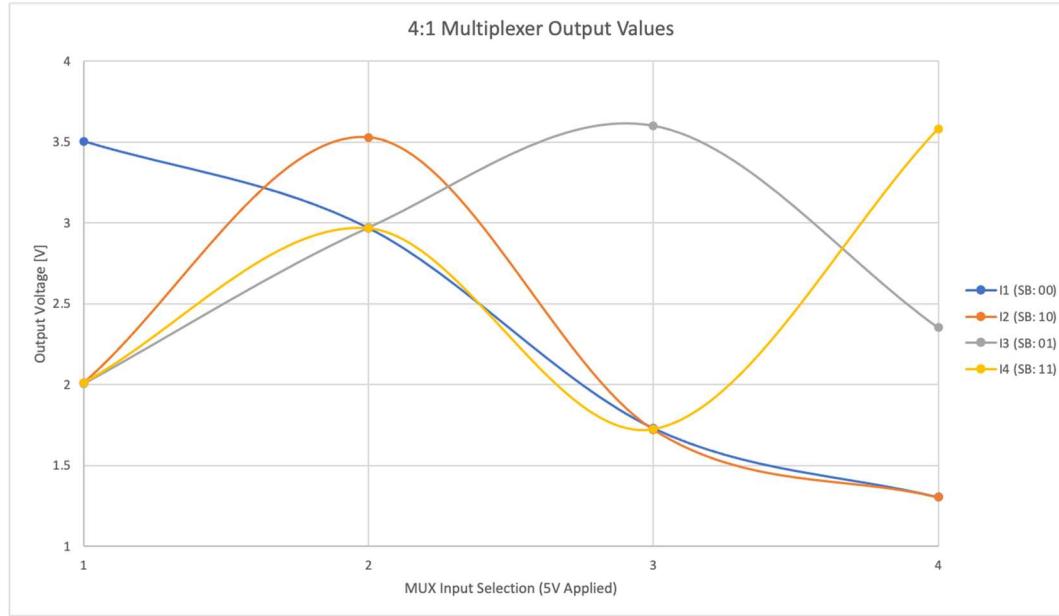
Table 3: Output Voltages when 5VDC Applied to Input 2

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.004 V
I2	0 V	1	0	2.971 V
I3	5 V	0	1	3.602 V
I4	0 V	1	1	2.352 V

Table 4: Output Voltages when 5VDC Applied to Input 3

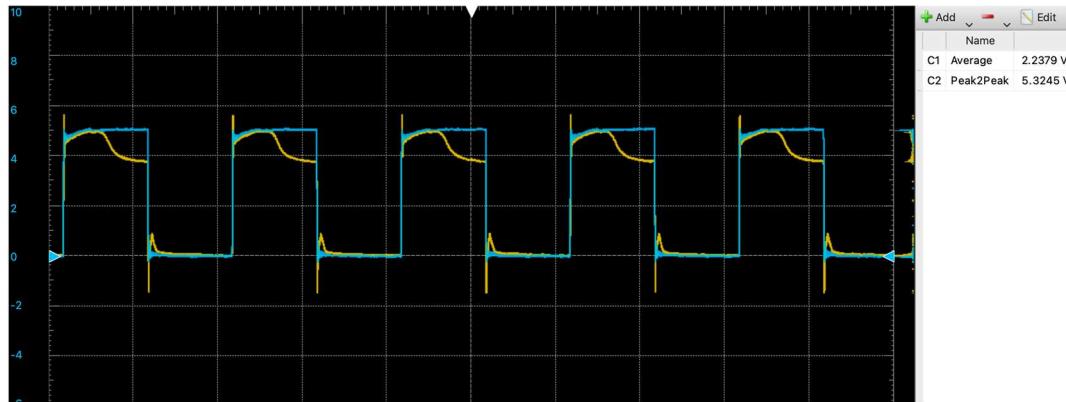
MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.012 V
I2	0 V	1	0	2.966 V
I3	0 V	0	1	1.726 V
I4	5 V	1	1	3.581 V

Table 5: Output Voltages when 5VDC Applied to Input 4



**Figure 29: 4:1 MUX Output Values vs. 4:1 MUX Input Selection**

Once the circuit was verified using 5VDC, the next test used a 5VAC square wave with a frequency of 100kHz as the input to the 4:1 multiplexer. This test was meant to simulate the input signal coming from the 1x4 SRAM array. The results for this test can be found in Figures 30-33 below, although these only illustrate when the 5VAC square wave was applied to input 1. The waveforms and data show the multiplexer operating as intended, outputting a high square wave when the selection bits are configured to 00, and outputting a low square wave for all other configurations. The values when 5VAC was applied to the three other inputs followed the same trend with their respective selection bit configurations. The 4:1 MUX input and output waveforms can be seen below.



**Figure 30: 4:1 MUX Output with 5AVC applied to Input 1 (Selection Bits: 00)**

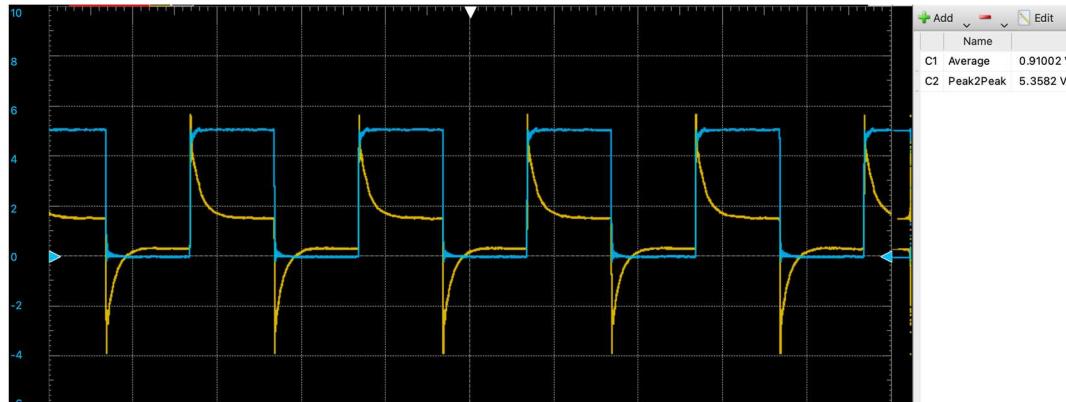


Figure 31: 4:1 MUX Output with 5AVC applied to Input 1 (Selection Bits: 10)

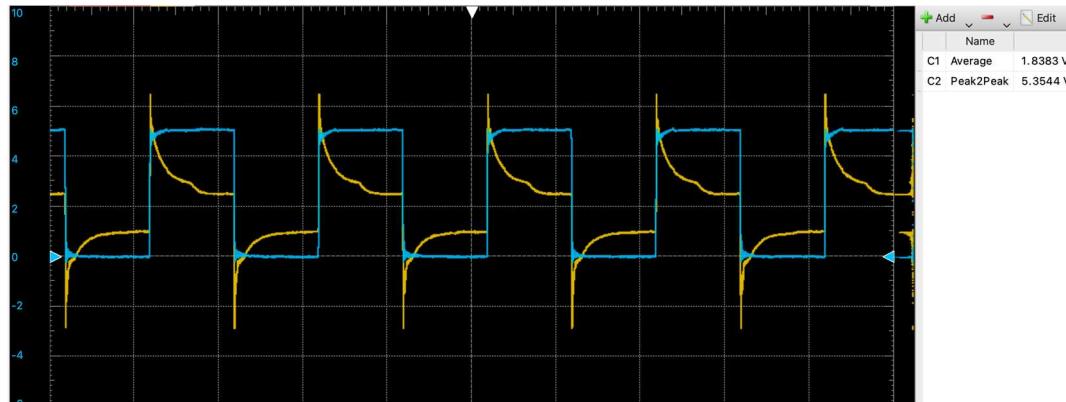


Figure 32: 4:1 MUX Output with 5AVC applied to Input 1 (Selection Bits: 01)

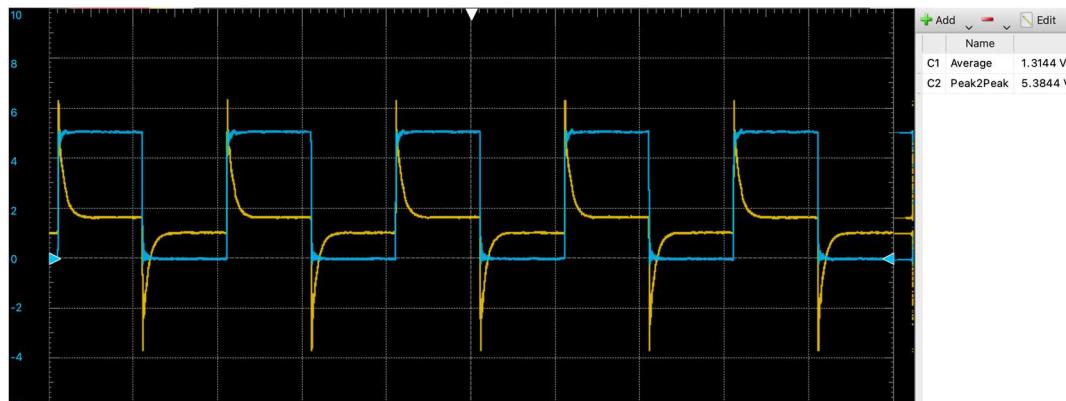


Figure 33: 4:1 MUX Output with 5AVC applied to Input 1 (Selection Bits: 11)

Lastly, some type of validation for the radiational resilient design choices of the 4:1 multiplexer would be incredibly useful. Therefore, we attempted to simulate the effects of radiation on the 4:1 MUX using both voltage and current spikes as well as charge build-up. The circuit was tested for currents spikes of up to 1A, and a charge build-up of up to 50V. The rad-hard design choices allowed for the simulation to remain generally unaffected by the radiation injections. The results for this rad test can be seen in Figures 34 & 35 below.

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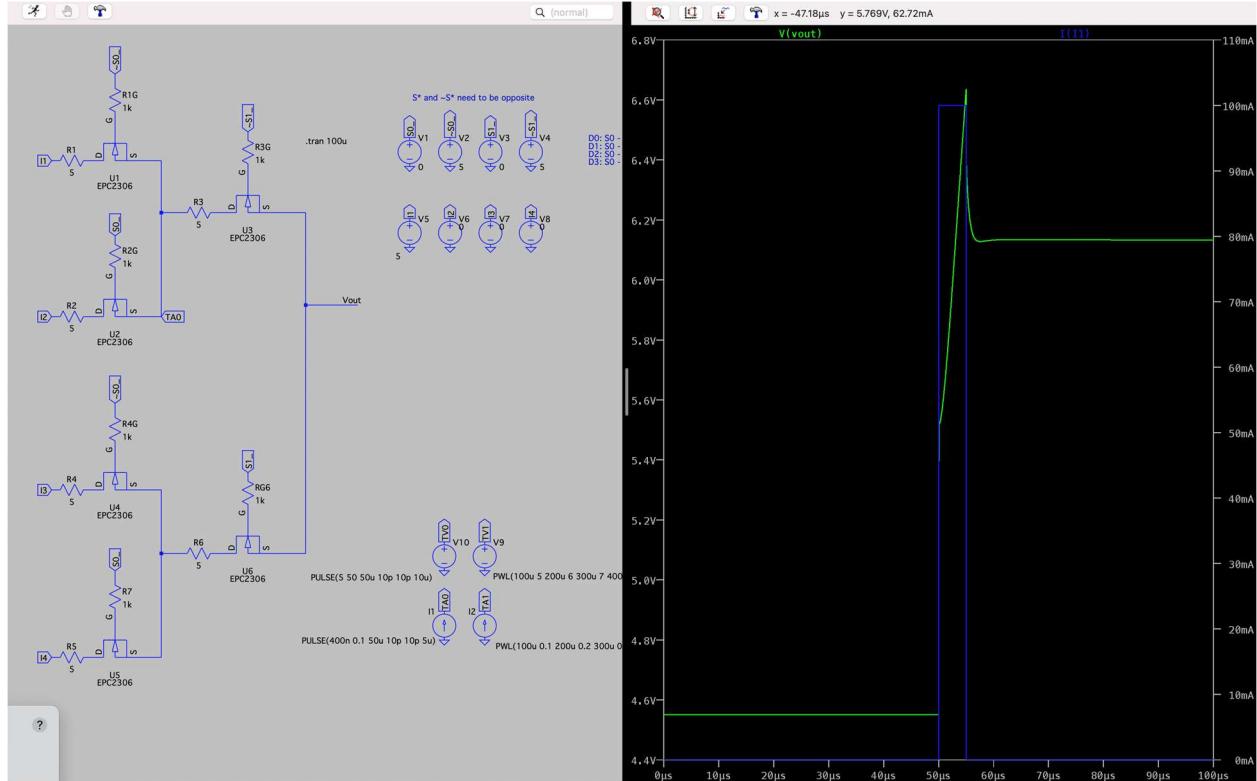


Figure 34: Radiation Simulation w/ Current Spike

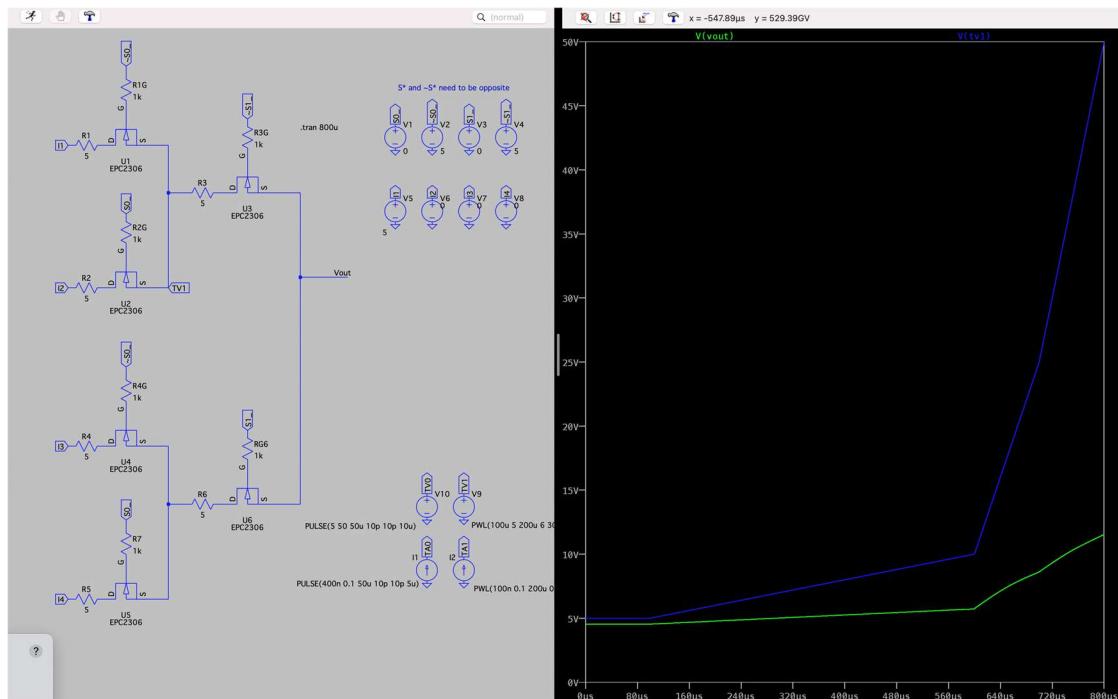


Figure 35: Radiation Simulation w/ Voltage Build-Up

#### **4.4. Subsystem Conclusion**

In conclusion, the design of the radiation-resilient 4:1 multiplexer was described, simulated, assembled, and verified to operate correctly. The implementation of wide bandgap GaN transistors, wire-wound resistors, and mechanical switches allowed for the operation of a rad-hardened 4:1 MUX. There were some issues, however, such as the output voltage value only being 3.5V when high as opposed to the 4.5V seen in the simulations. The low value was also causing problems, reading between ~1.5V-3V for low instead of close to 0V as seen in the simulations. While a high and low can be identified, therefore verifying the circuit, more research is required to understand why the high and low values do not align with the simulations. After preliminary research, we believe these issues could arise due to the source of the transistor not being directly connected to ground, as seen in the seven stage ring oscillator. By setting the source to ground, we can verify that when 5V is applied to the gate, it is indeed 5V from gate to source, not just 5V to the gate as it is currently configured. Potential solutions include changing the design where all the sources are connected directly to ground, or implementing GaN gate drivers to ensure 5V is being applied from gate to source and fully opening the transistor. Besides this issue, the 4:1 MUX was operating as expected and will function as the final output of the system.

## 5. Next Steps

This section highlights the plans for the next semester of senior design, covering the integration of the subsystems as well as the testing and validation for the full integrated system.

### 5.1. Integration

The final system design requires the combination of the three subsystems outlined in the report: the seven-stage ring oscillator, the 1x4 SRAM array, and the 4:1 multiplexer. As previously outlined, the seven-stage ring oscillator is the input clock signal for the SRAM array, the SRAM stores the value from the clock, and the MUX selects which of the array cells to set as the output. In order to integrate these systems, constant communication between subsystems is required. The best way to guarantee this integral communication is by placing all three subsystems on one large PCB, as opposed to the three individual PCBs we made this semester. This would allow us to communicate between subsystems via traces on the PCB, not external wires, ensuring a steadier form of signal transmission. This also prevents the possibility of wires connecting the subsystems from falling out of terminal blocks during radiation testing, a catastrophic failure that would conclude the test. Another integration obstacle is combining our three individual power circuits into one large power system. This could lead to complications in the system as we analyze how the voltage of one subsystem affects the others. The three individual PCBs can be seen in Figures 36-38 below. We will soon begin researching the best way to place all three subsystems on one large PCB, while not exceeding the dimension requirements.

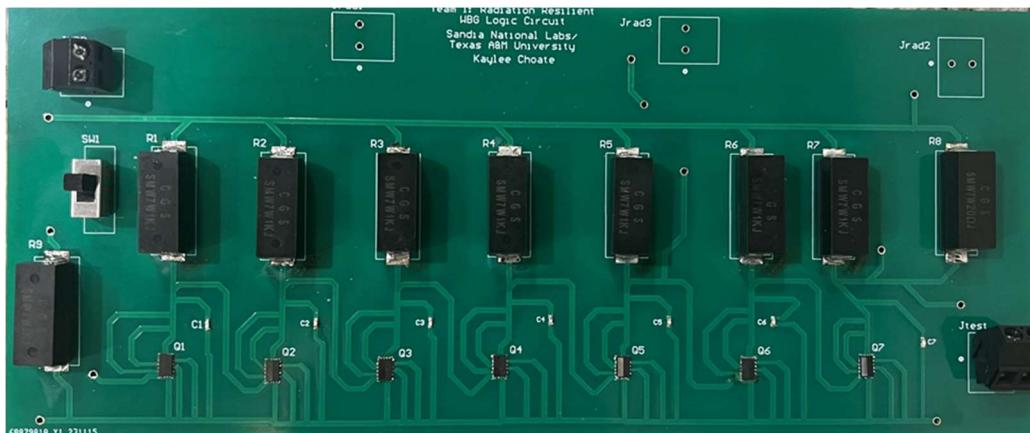


Figure 36: Seven-Stage Ring Oscillator Physical PCB

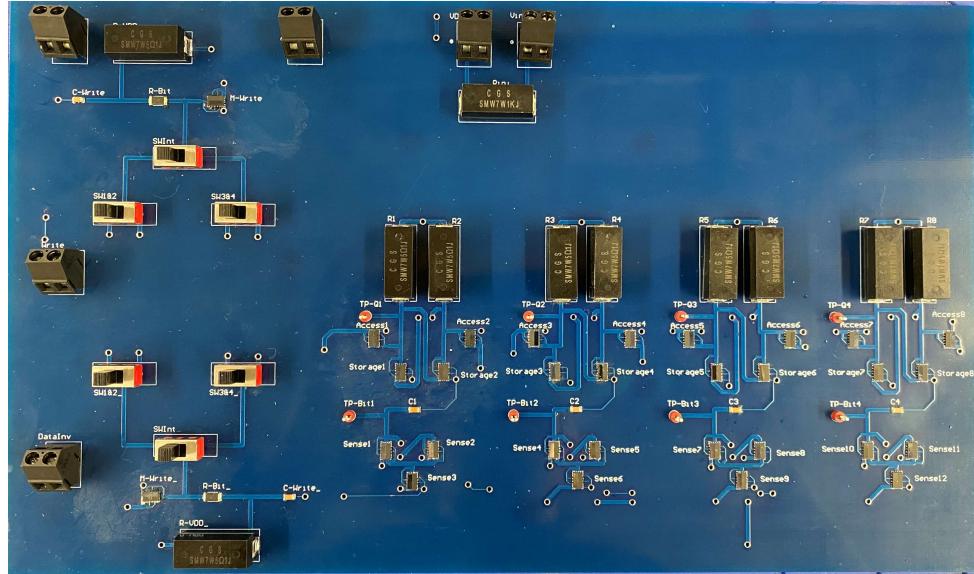


Figure 37: 1x4 SRAM Cell Array Physical PCB

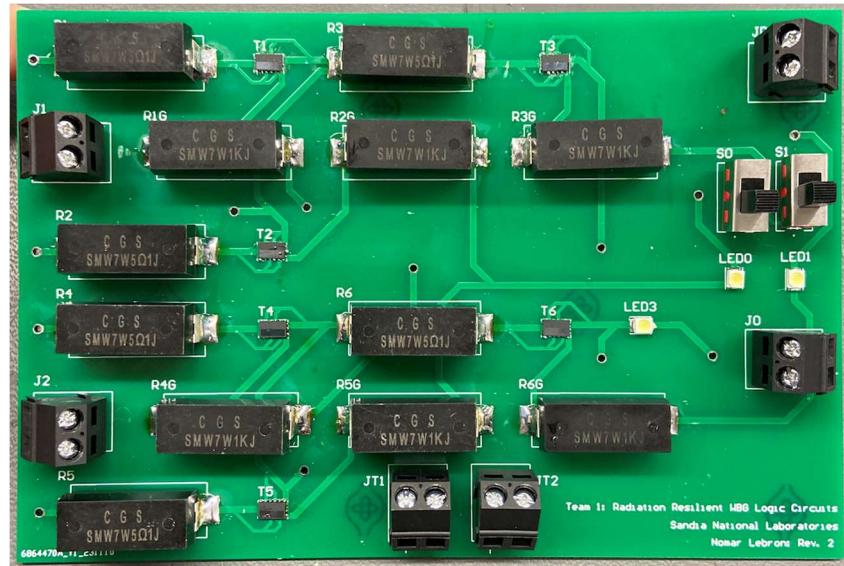


Figure 38: 4:1 Multiplexer Physical PCB

## **5.2. Testing and Validation**

For the full system testing and validation, many of the validation tests performed on the individual subsystems will be repeated. This time, however, we will be testing the individual subsystems to see how they perform when connected to the full system. Tests such as data line selection for the MUX and data stability for the SRAM will be repeated, this time as part of the system. The combined data will then be compared to the individual data acquired in this report. If the systems work as expected few discrepancies between the combined and individual data should be found. Full system tests will be conducted as well, such as measuring the total current through the system and measuring the output voltage waveform. These full systems tests will allow us to verify the entire system before sending the PCB off for radiation testing. Before real full system radiation testing, we plan on conducting the individual simulated radiation tests outlined on the validation plan on our individual PCBs. We decided to wait until after the final demonstration to inject the voltage and current spikes so as not to destroy our working PCBs before being able to demonstrate them. Now that the demonstration is complete, we will begin trying to replicate the results seen in the radiation simulations shown above. We will mimic the effects of radiation by exposing the circuits to a spike and build-up of charge. According to the simulations, the circuits should be resistant to these injections, and continue operating as intended. Once the preliminary individual and full system testing is complete, the circuits will be sent to Sandia National Labs to be tested in a radiation environment.