Dwight Look College of ENGINEERING
TEXAS A&M UNIVERSITY

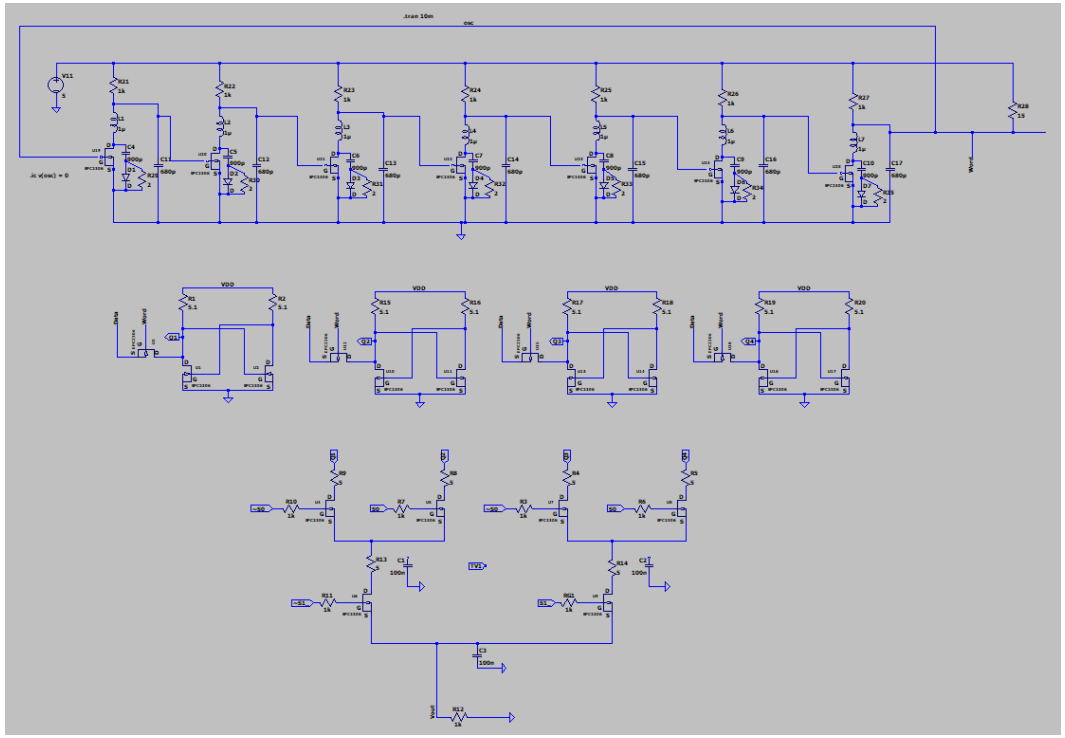
Team 1: Radiation Resilient Logic Circuit Study with WBG Devices
Bi-Weekly Update 3

Nia Baireddy, Kaylee Choate, Nomar Lebron
Sponsor: Sandia National Laboratories
TA: Eric Robles

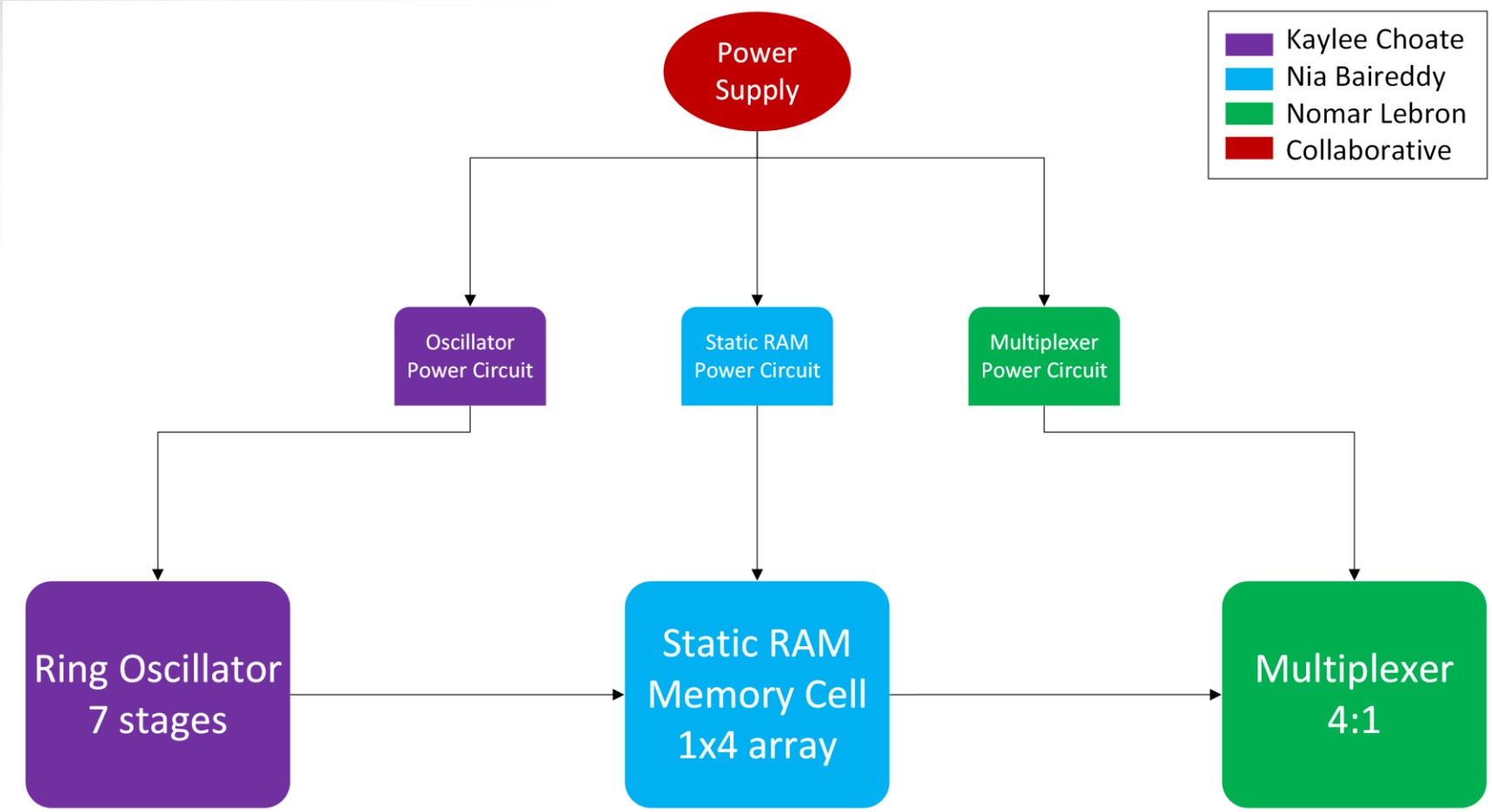
Project Summary and Solution

- Radiation effects on circuits are detrimental and must be mitigated for robust applications in space, military, and nuclear industries.

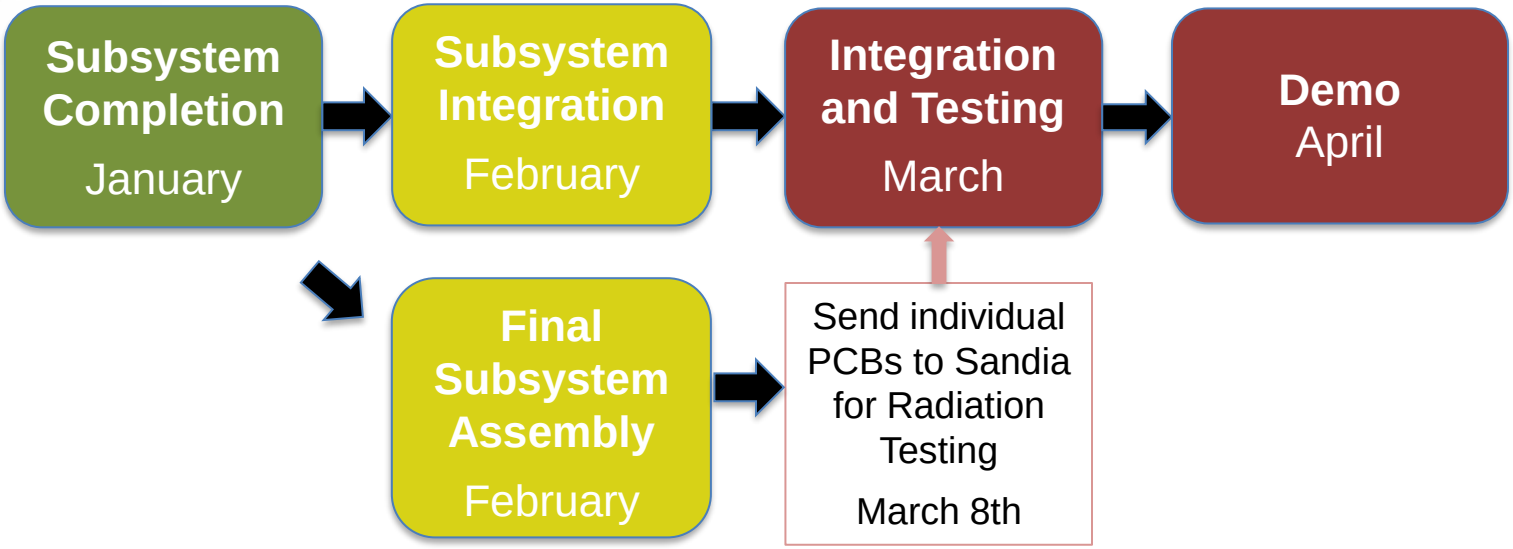
- Use radiation hardening by design techniques to modify various logic circuits for reliable operation in radiation environments.



Project Subsystem Overview



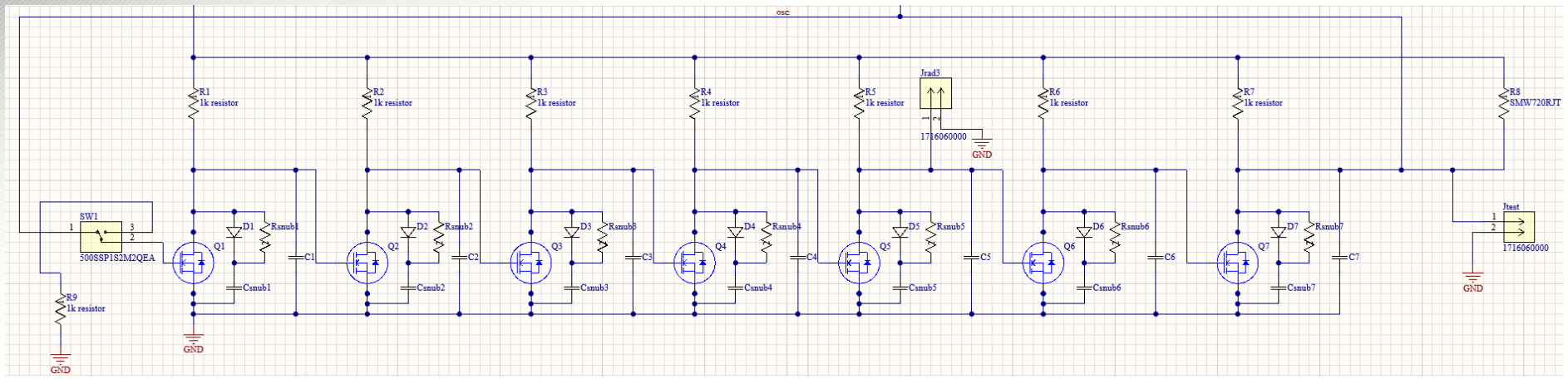
Project Timeline

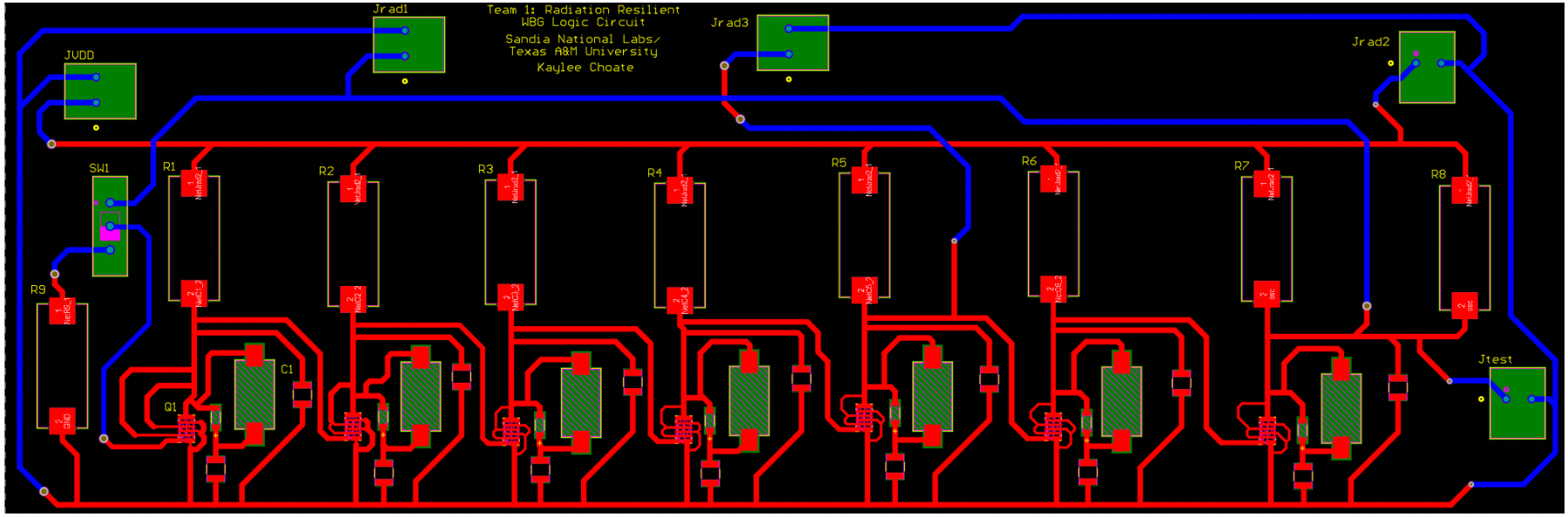


Kaylee Choate

Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Assembling subsystem PCB • Completed integrated system design and testing in LTspice • Began integrated system design in Altium	• Finish assembling/test subsystem PCB • Finalize Altium design and order integrated PCB

Kaylee Choate

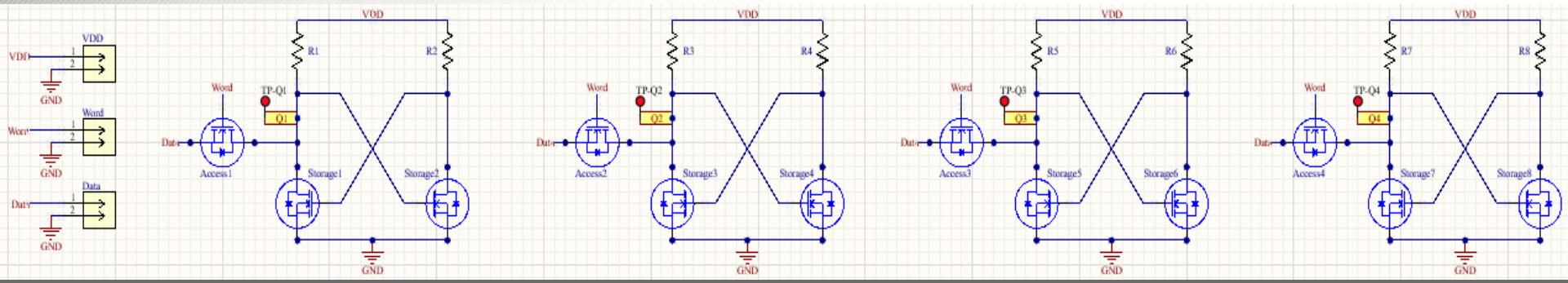


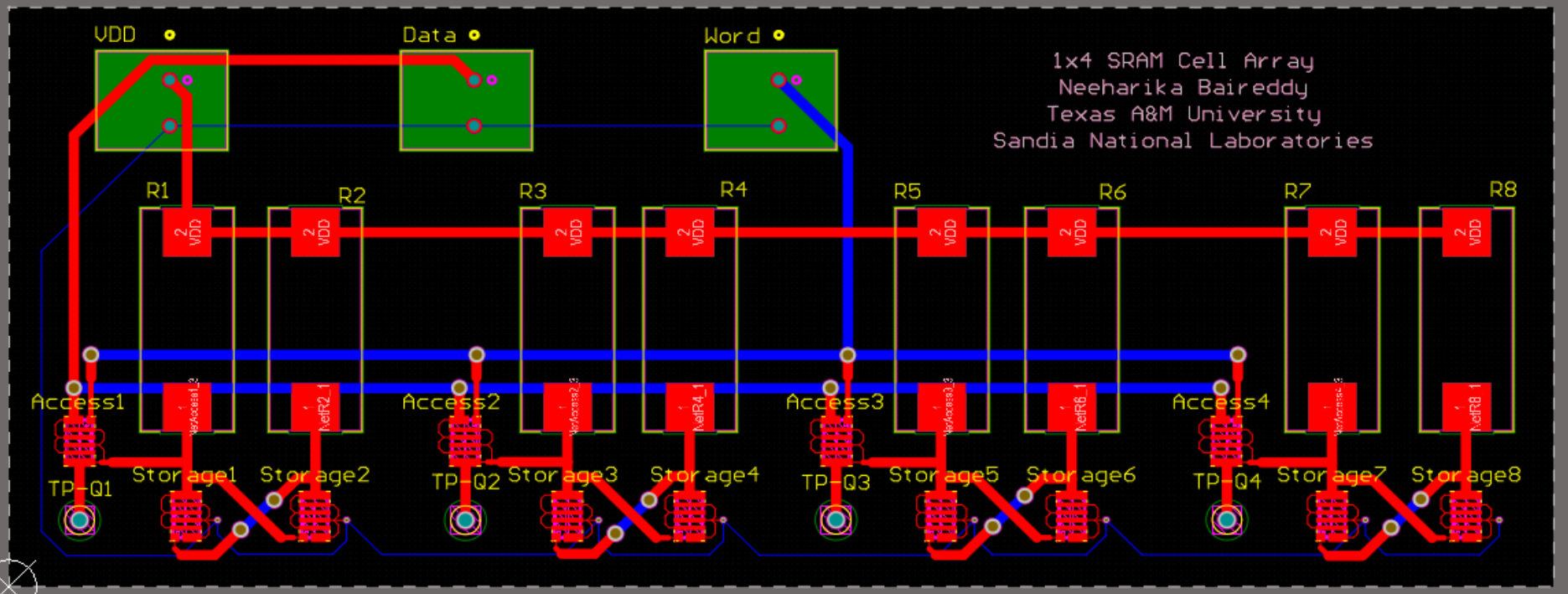


Nia Baireddy

Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Finalized and ordered improved subsystem PCB • Integrated improved subsystem with others for LTSpice simulations • Began integrated system design in Altium	• Assemble individual PCB and test/validate for Sandia • Complete integrated system in Altium • Order integrated PCB or PCBs

Nia Baireddy

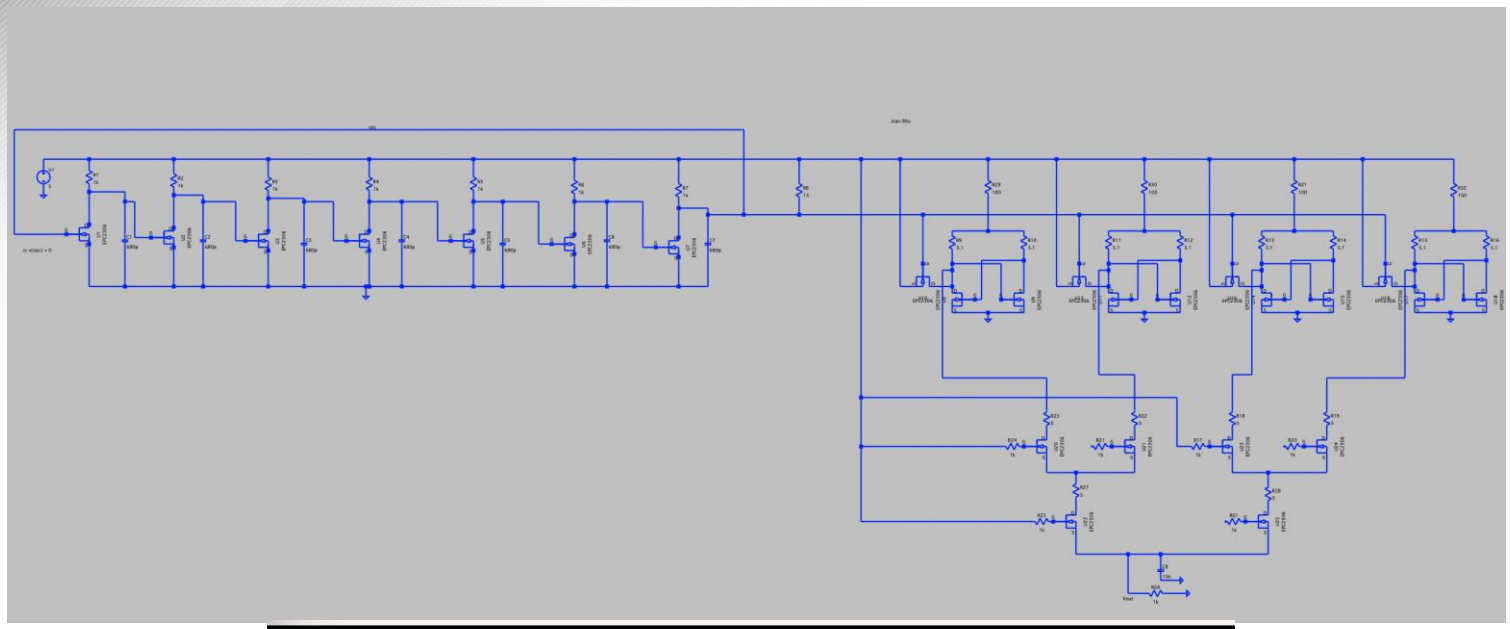


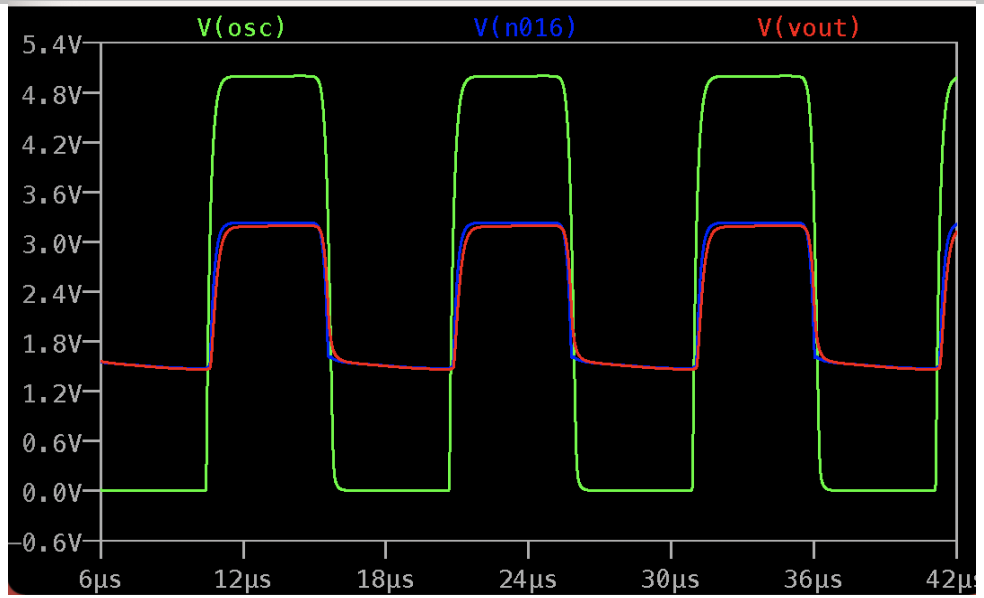


Nomar Lebron

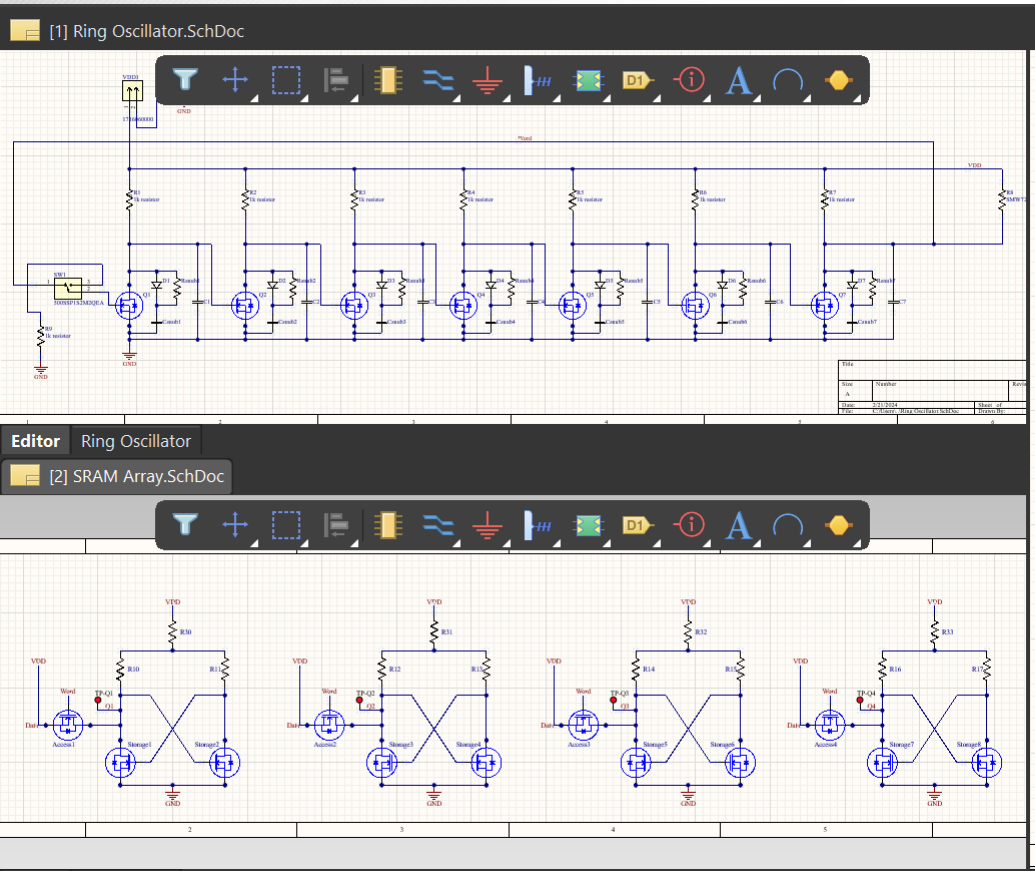
Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
• Completed Integration of 3 Subsystems in LTSpice • Completed Integrated Altium Schematic • On-Going Progress on Integrated Altium PCB	• Complete Integrated Altium PCB • Perform Testing and Validation on individual circuit before sending to Sandia

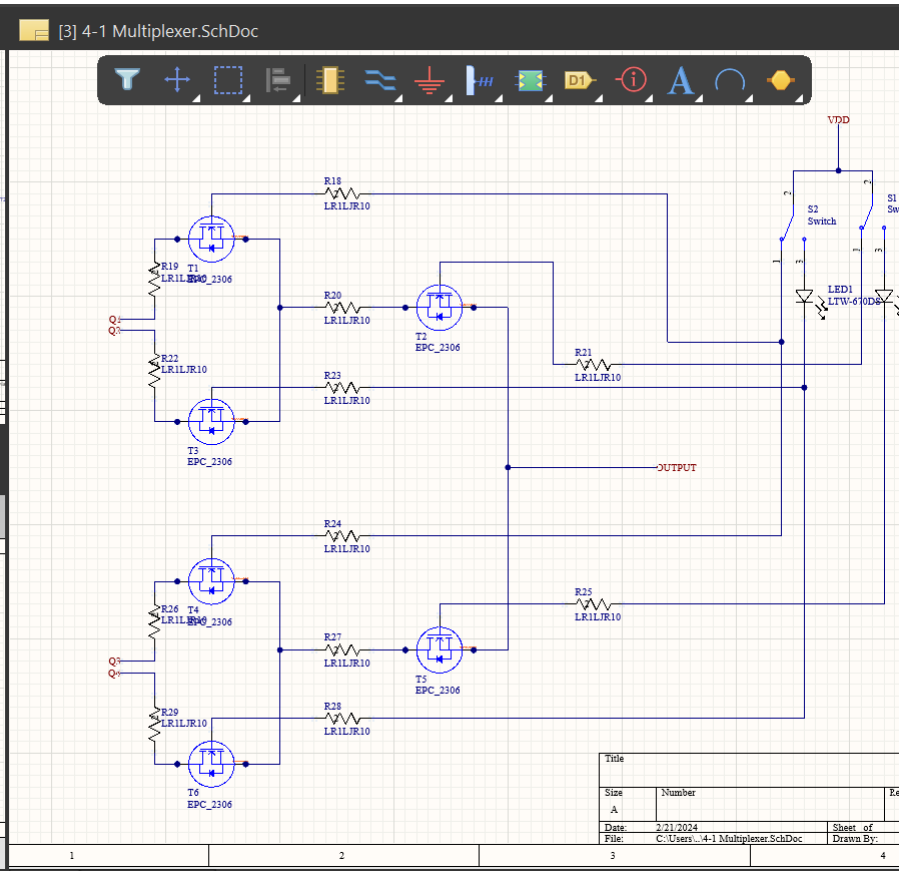
Nomar Lebron



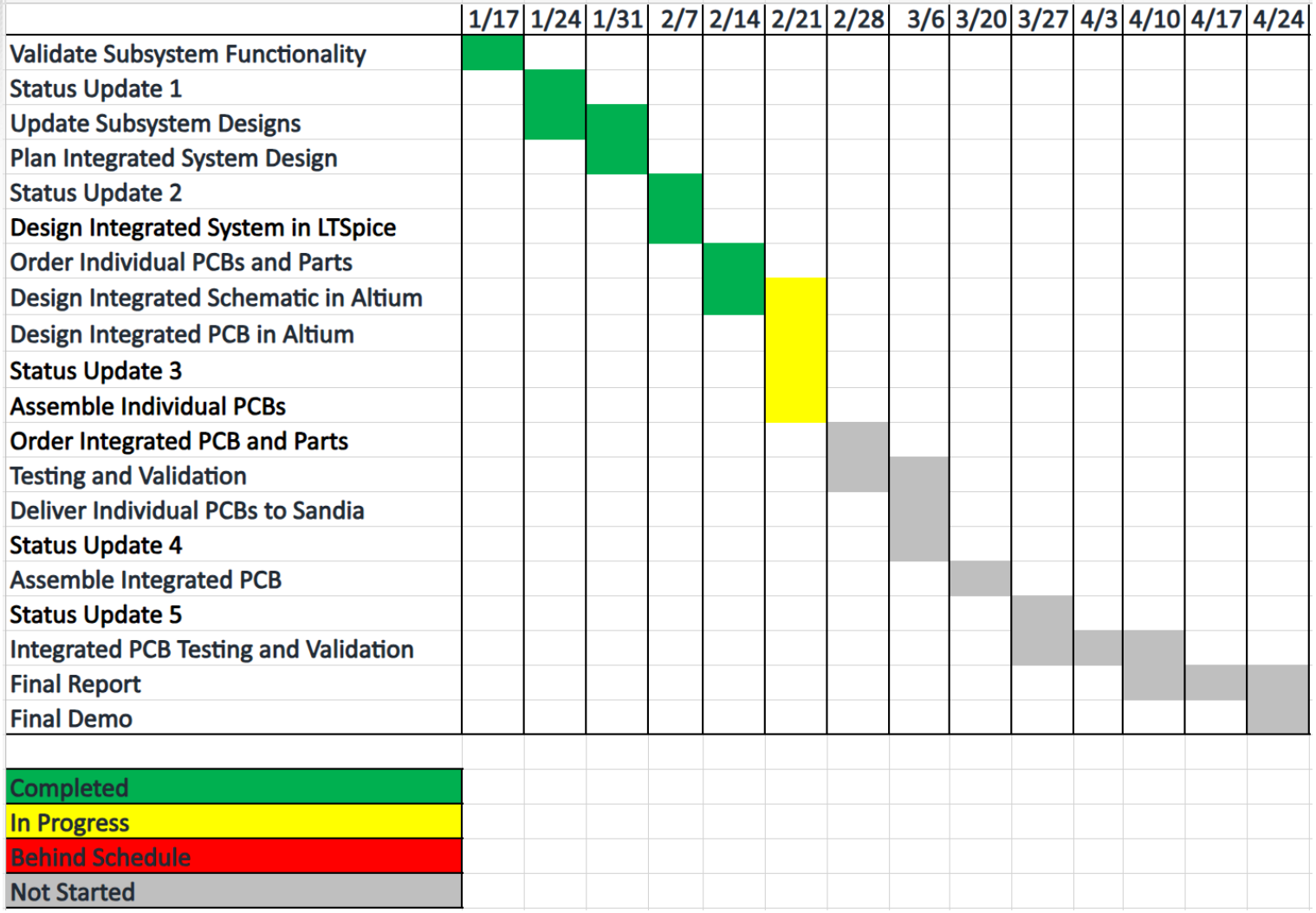


Integrated System in Altium





Execution Plan



Validation Plan

Ring Oscillator Task	Specification	Result (Sim)	Result (PCB)	Owner	Date
Voltage Input (max)	5V	Pass		Kaylee	3/6/2024
Square Wave	yes/no	Pass		Kaylee	3/6/2024
Frequency Range	100kHz	Pass		Kaylee	3/6/2024
Magnitude Variation	0-5V	Pass		Kaylee	3/6/2024
Power Consumption	~ 10 mW	Pass		Kaylee	3/6/2024
Supply Voltage Variation Test	Vdd +/- 10%	Pass		Kaylee	3/20/2024
Voltage Spike	50V	Pass		Kaylee	3/20/2024
Voltage Build Up	50V	Pass		Kaylee	3/20/2024
Current Spike	5A	Pass		Kaylee	3/20/2024
Current Build Up	5A	Pass		Kaylee	3/20/2024
1x4 SRAM Memory Cell Array Task	**Specification**	**Result (Sim)**	**Result (PCB)**	**Owner**	**Date**
Voltage Input Max (Vdd)	5V	Pass		Nia	3/6/2024
Read/Write Speed	~ 10 ns	Pass		Nia	3/6/2024
Read/Write Disturb	< 10 cycles	Pass		Nia	3/6/2024
Hold and Setup Time	~ 5 ns	Pass		Nia	3/6/2024
High/Low Voltage	Vdd +/- 10%	Pass		Nia	3/20/2024
Read/Write Stability Margin (Voltage)	Vdd +/- 10%	Pass		Nia	3/20/2024
Power Consumption (active)	~ 10 mW	Pass		Nia	3/20/2024
Power Consumption (idle)	~ 10 uW	Pass		Nia	3/20/2024
Data Recovery Test	~ 10 ms	Pass		Nia	3/20/2024
4:1 Multiplexer Task	**Specification**	**Result (Sim)**	**Result (PCB)**	**Owner**	**Date**
Voltage Input (max)	5V	Pass		Nomar	3/6/2024
Select Line Test	4 inputs	Pass		Nomar	3/6/2024
Data Stability	Vdd +/- 10%	Pass		Nomar	3/6/2024
High/Low Voltage	Vdd +/- 10%	Pass		Nomar	3/6/2024
Power Consumption Test	< 6W	Pass		Nomar	3/20/2024
User Interface Testing	Switches	Pass		Nomar	3/20/2024
User Interface Testing	LEDs on/off	N/A		Nomar	3/20/2024
Supply Voltage Variation Test	Vdd +/- 10%	Pass		Nomar	3/20/2024

Thanks and Gig ‘Em!

Questions?