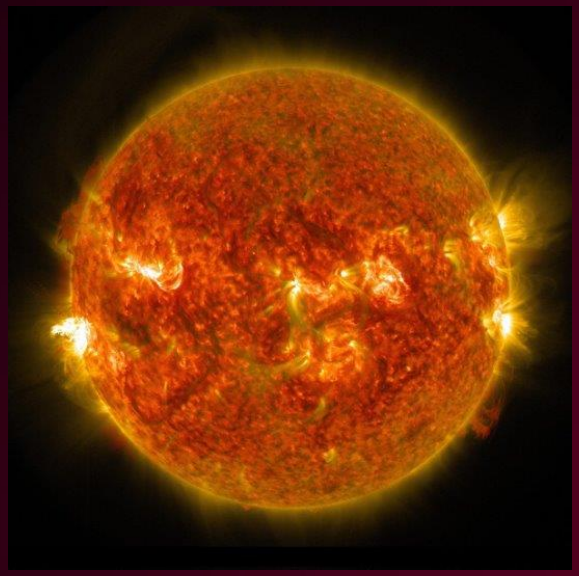


Dwight Look College of ENGINEERING
TEXAS A&M UNIVERSITY

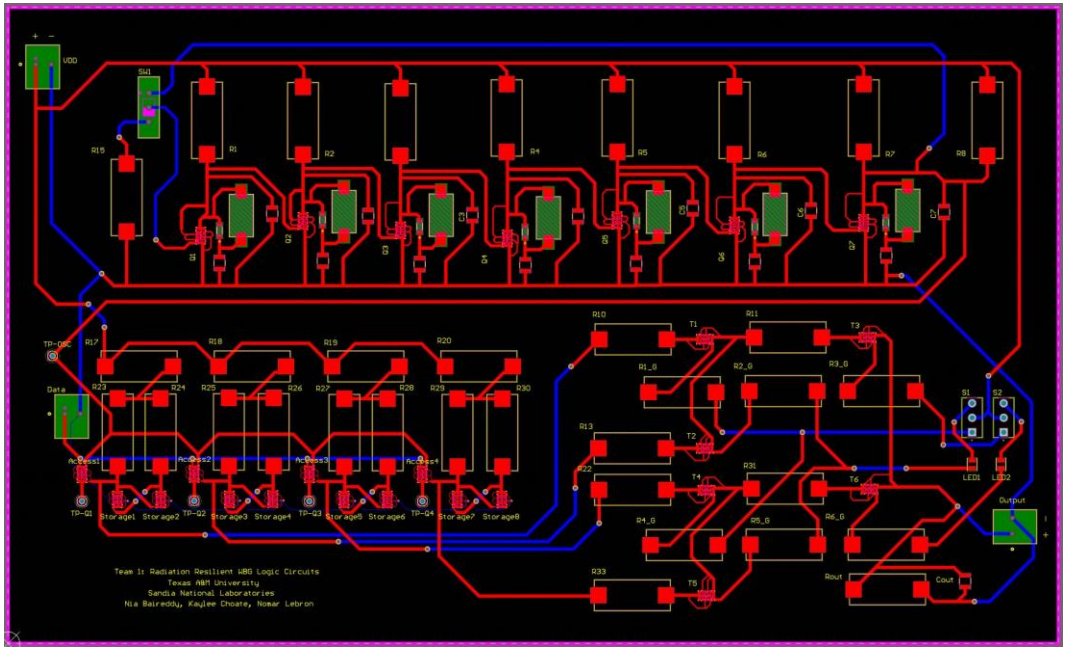
ECEN 404 Final Presentation
Team 1: Radiation Resilient Logic Circuit Study with WBG Devices

Nia Baireddy, Kaylee Choate, Nomar Lebron
Sponsor: Sandia National Laboratories
TA: Eric Robles

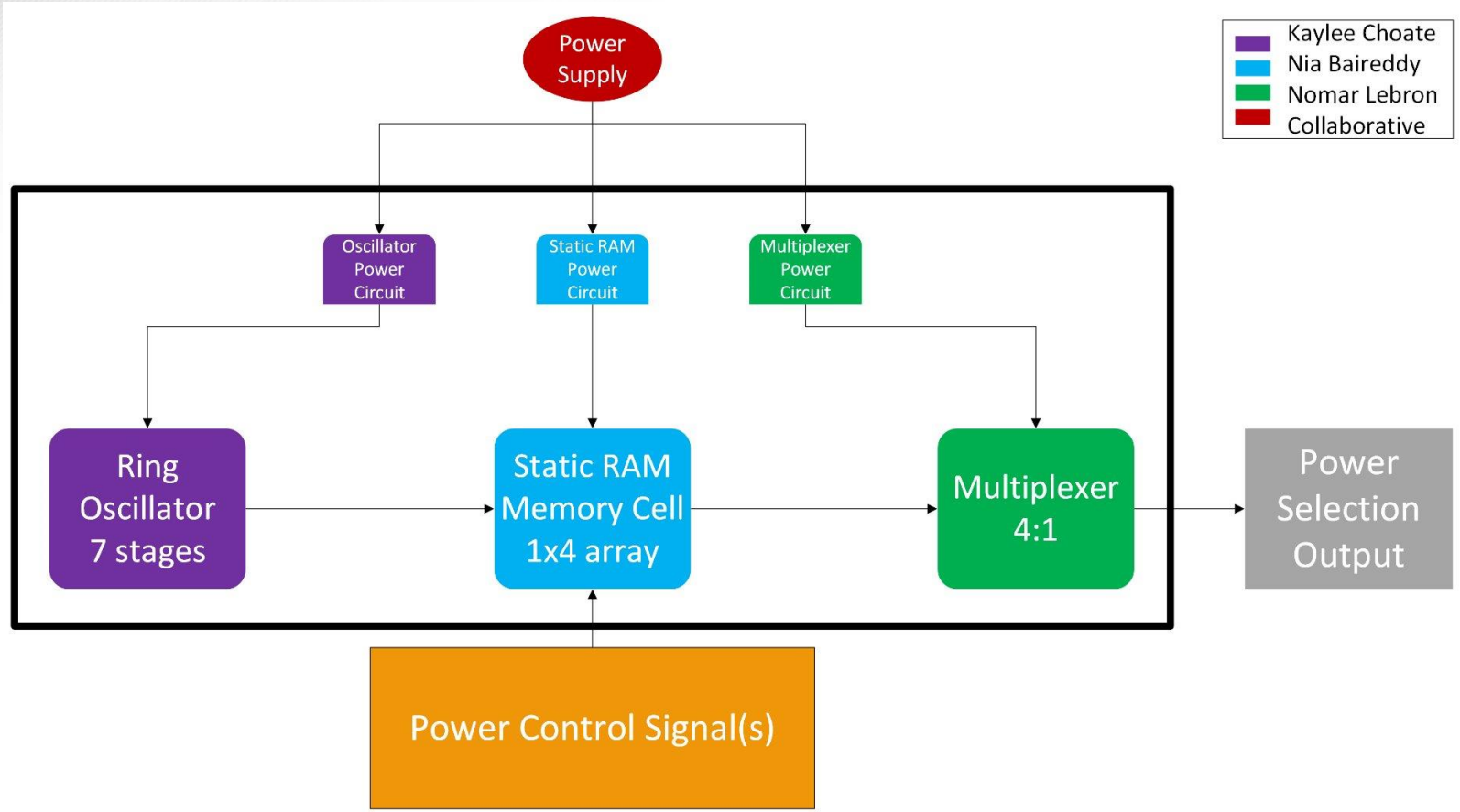
Problem Overview

- Radiation effects on circuits are detrimental and must be mitigated for robust applications in space, military, and nuclear industries.

- Use radiation hardening by design techniques to modify various logic circuits for reliable operation in radiation environments.



Integrated Project Diagram



Engineering Design Choices

- Radiation resilient wide bandgap material - GaN
  - Higher intrinsic radiation resilience
- Hardened components
  - Low resistance wirewound resistors
  - Multi-layer ceramic capacitors
- Alternative circuit layout
  - NMOS only
  - Trace width
  - Trace spacing

Engineering Design Accomplishments

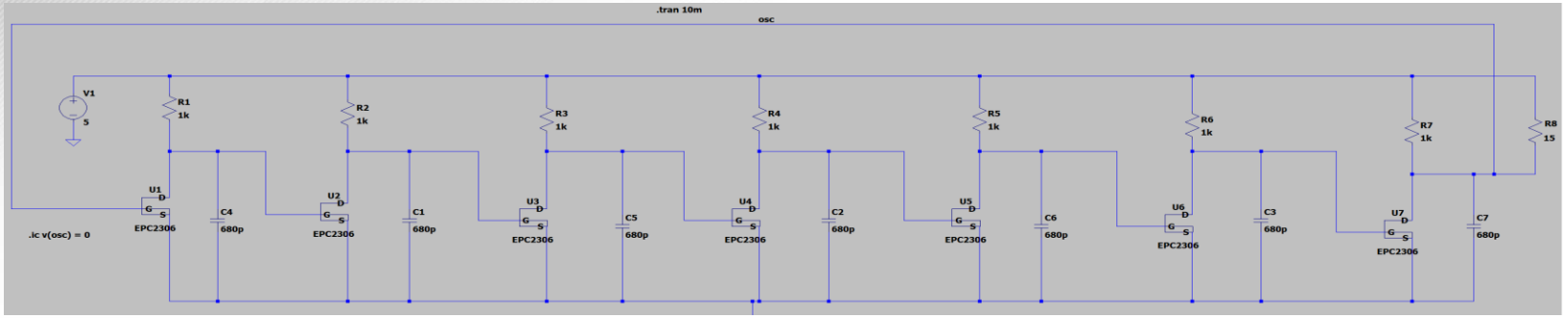
Kaylee Choate

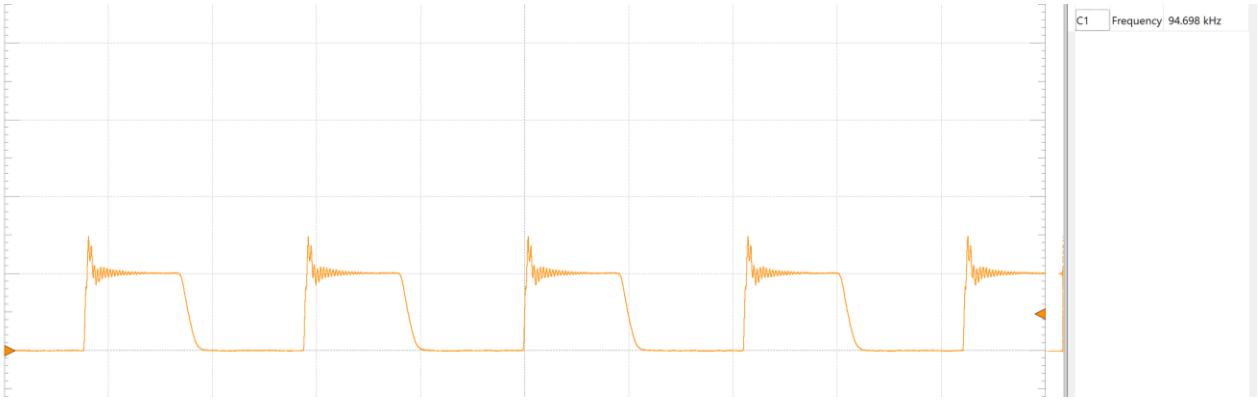
- Objective: Design a rad-hard ring oscillator to produce a clock signal with a frequency of 100kHz in the presence of radiation
  - Design Choices:
    - 7 stages
    - Chose capacitor values to fine-tune frequency
    - Chose resistor values to allow signal inversion
    - Added buffer to stabilize output waveform
- Challenge: 3.8V spike on output signal
- Solution: Added a RCD snubber to reduce inductance and lessen the spike

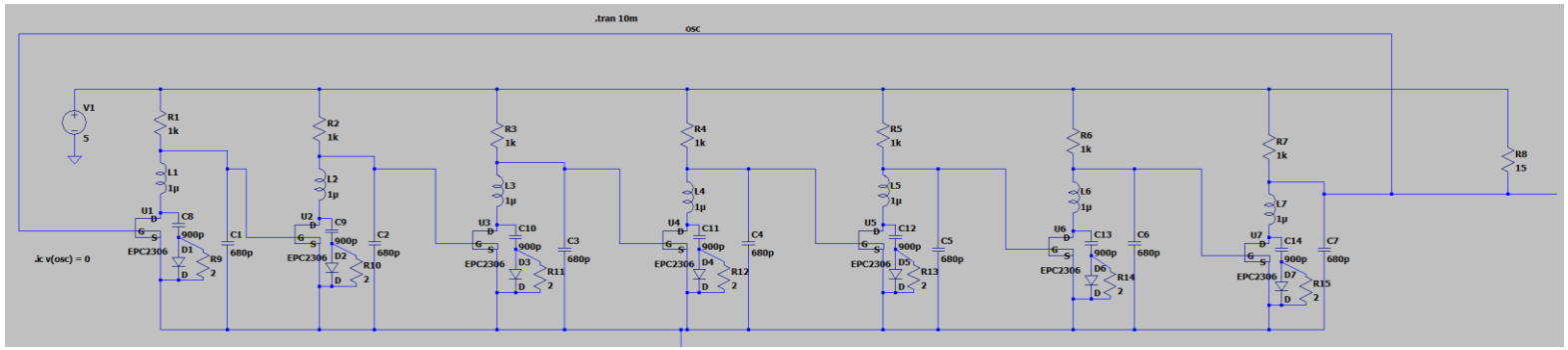
Dwight Look College of ENGINEERING
TEXAS A&M UNIVERSITY

Engineering Design Accomplishments

Kaylee Choate

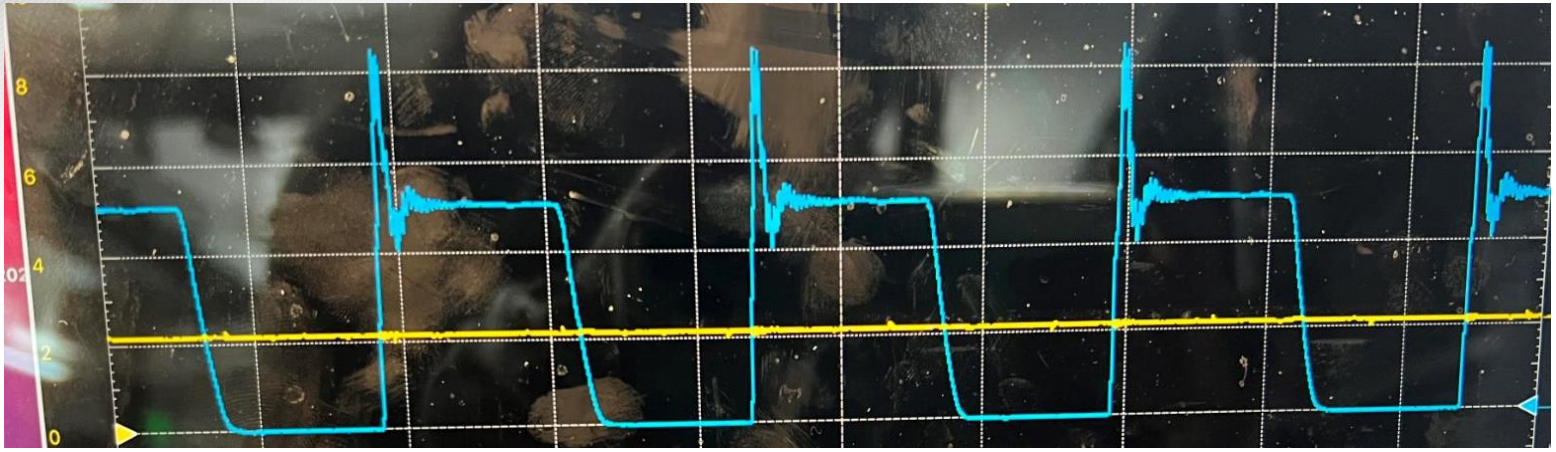


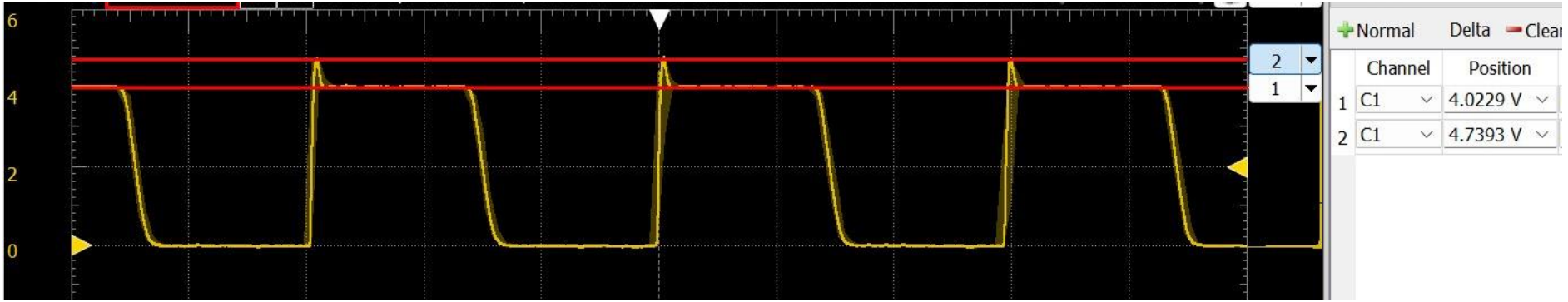




Engineering Design Accomplishments

Kaylee Choate





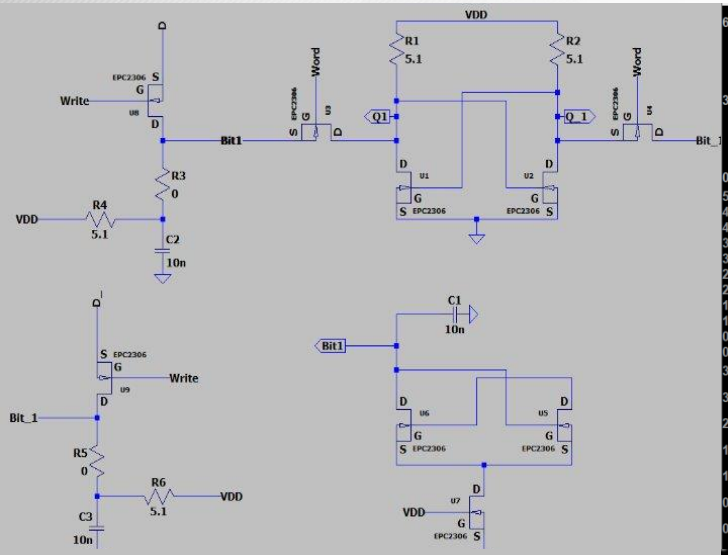
Engineering Design Accomplishments

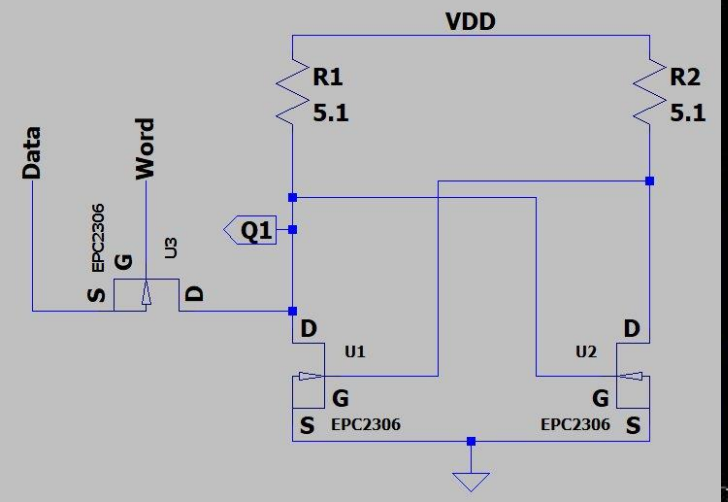
Nia Baireddy

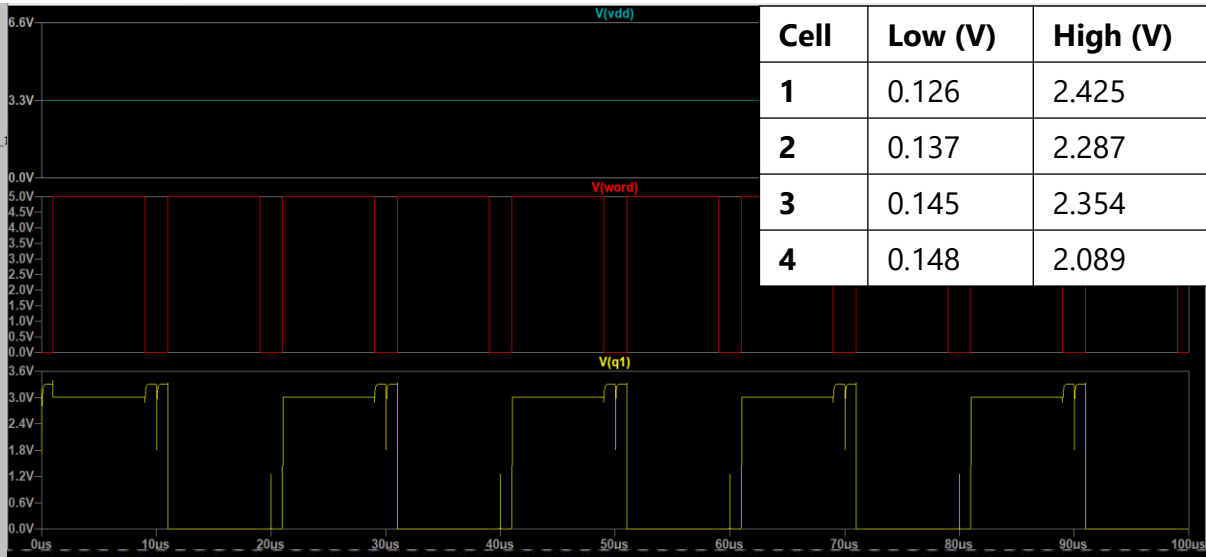
- Objective: Design a rad-hard SRAM cell that holds latched value during radiation event
  - Design Choices:
    - 4 cells in 1 row
    - Calculated resistor values for inverters
    - Calculated capacitor values for sense amplifiers
    - Modified write circuits (added resistors and capacitors)
- Challenge: Floating FET drain gave logic low value of 1.6V
- Solution: Remove write circuits and sense amplifiers, only use one access transistor for noninverting bitline

Engineering Design Accomplishments

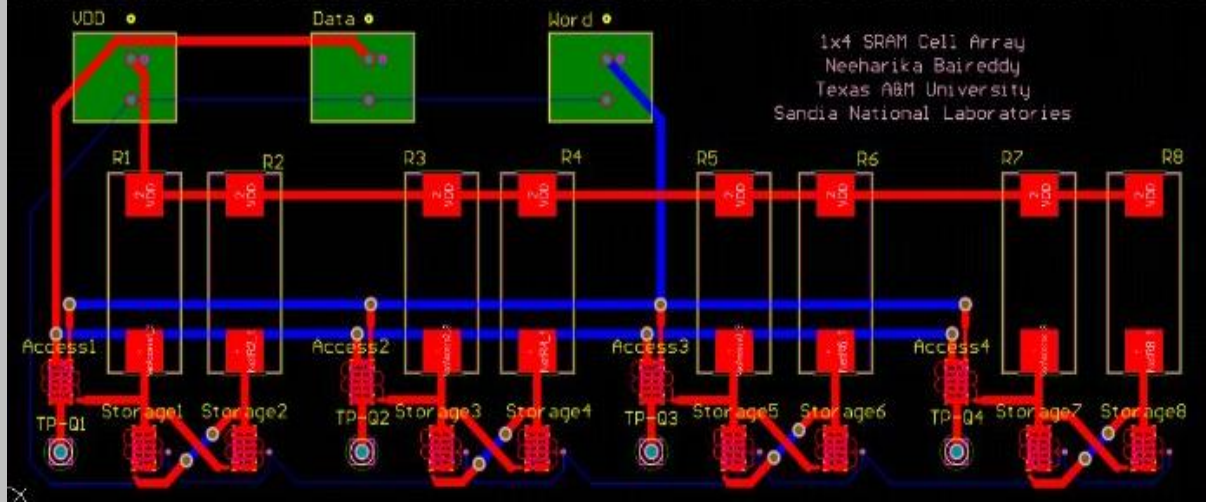
Nia Baireddy







Cell	Low (V)	High (V)
1	0.126	2.425
2	0.137	2.287
3	0.145	2.354
4	0.148	2.089



Engineering Design Accomplishments

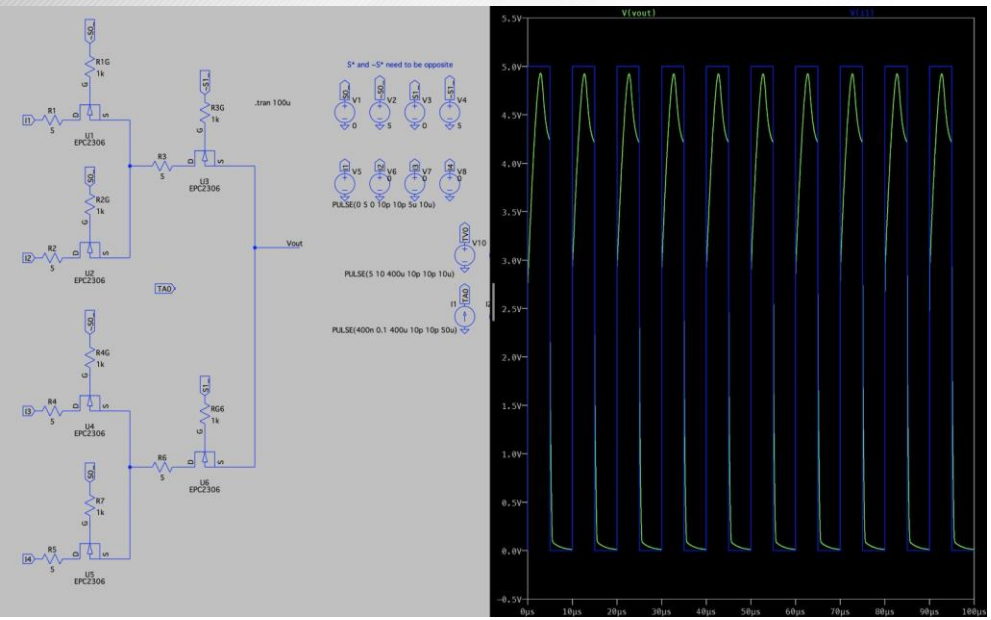
Nomar Lebron

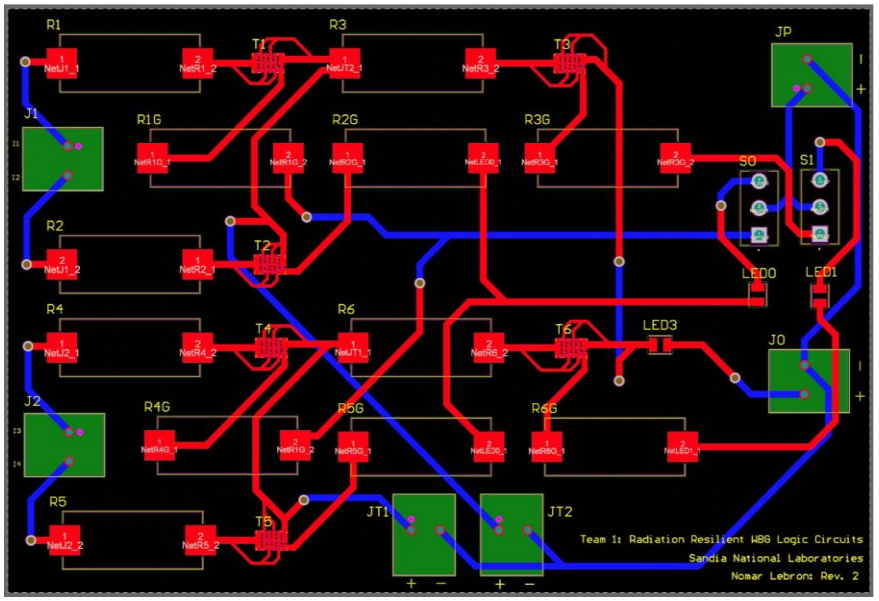
- Objective: Design a rad-hard 4:1 Multiplexer to select between the four cells of the 1x4 SRAM cell array in the presence of radiation
  - Design Choices:
    - Calculated resistor values
    - LEDs for User Interface
    - 5V to turn on transistors
    - Decoupling capacitor
- Challenge: Voltage spike when low cell value selected
- Solution: Added decoupling capacitor for better data stability

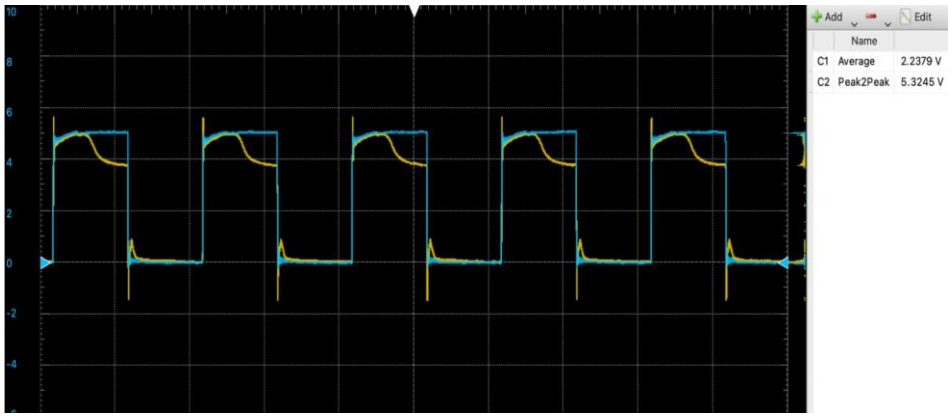
Dwight Look College of ENGINEERING
TEXAS A&M UNIVERSITY

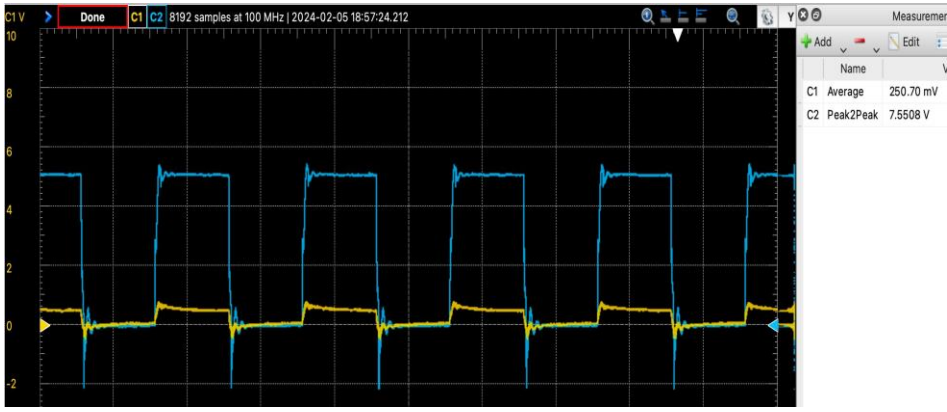
Engineering Design Accomplishments

Nomar Lebron









Engineering Design Accomplishments

Nomar Lebron

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	5 V	0	0	3.505 V
I2	0 V	1	0	2.968 V
I3	0 V	0	1	1.731 V
I4	0 V	1	1	1.304 V

Table 2: Output Voltages when 5VDC Applied to Input 1

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.011 V
I2	5 V	1	0	3.528 V
I3	0 V	0	1	1.723 V
I4	0 V	1	1	1.305 V

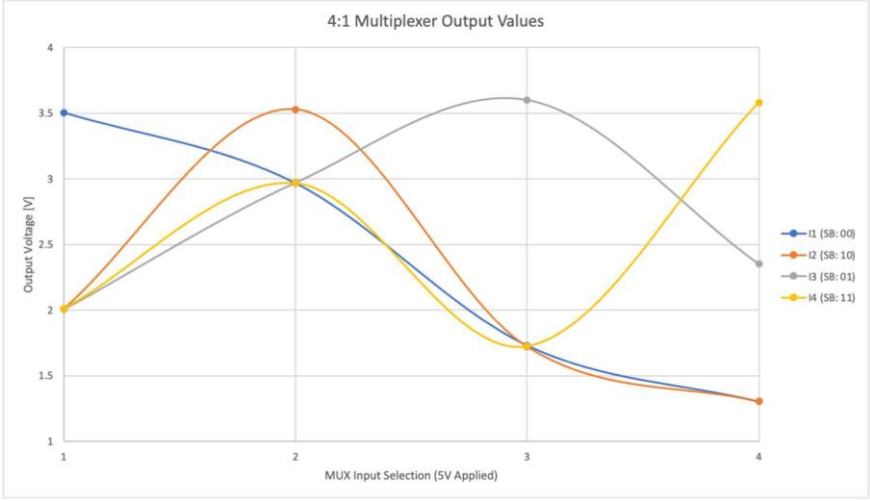
Table 3: Output Voltages when 5VDC Applied to Input 2

MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.004 V
I2	0 V	1	0	2.971 V
I3	5 V	0	1	3.602 V
I4	0 V	1	1	2.352 V

Table 4: Output Voltages when 5VDC Applied to Input 3

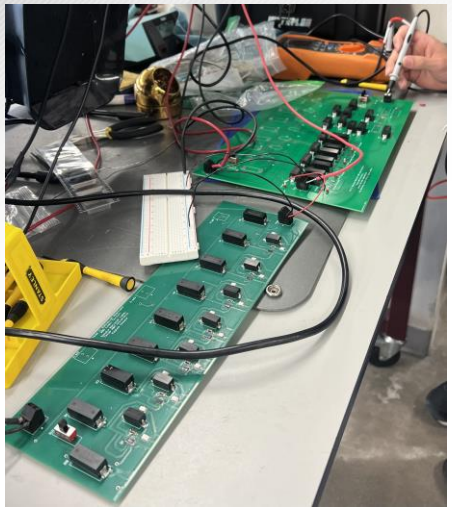
MUX Input	Input Voltage	Selection Bit 0	Selection Bit 1	Output Voltage
I1	0 V	0	0	2.012 V
I2	0 V	1	0	2.966 V
I3	0 V	0	1	1.726 V
I4	5 V	1	1	3.581 V

Table 5: Output Voltages when 5VDC Applied to Input 4

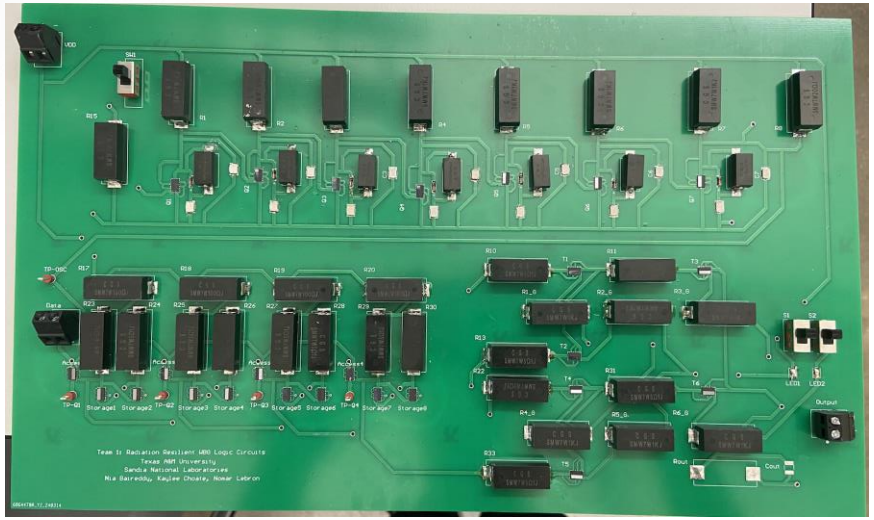


Integrated System Results

Connected individual 7-stage ring oscillator to integrated 1x4 SRAM with positive results



Fully integrated three subsystems onto one PCB



Nominal Operation Validation

	Ring Oscillator Frequency	SRAM High Output	4:1 MUX Output	SRAM Low Output	4:1 MUX Output
Cell 1	52.6 kHz	1.626	1.633	1.016	1.022
Cell 2		2.017	2.018	1.047	1.052
Cell 3		1.580	1.585	0.999	1.009
Cell 4		1.642	1.691	1.098	1.068

Conclusions

- Excessive circuit elements and large PCBs created a lot of noise
- Removed redundant circuit elements
  - Significant reduction of transistor counts
- Current Status
  - Completed nominal operation validation
    - Need to troubleshoot potential floating between oscillator and SRAM array
  - Began radiation operation validation