

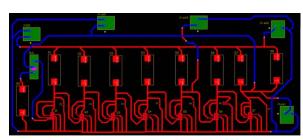
Team 1: Radiation Resilient Logic Circuit Study with WBG Devices Bi-Weekly Update 1

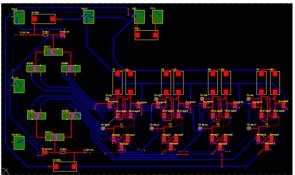
Nia Baireddy, Kaylee Choate, Nomar Lebron Sponsor: Sandia National Laboratories TA: Eric Robles

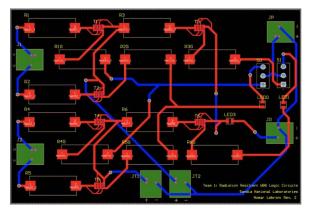


Project Summary and Solution

- Radiation effects on circuits are detrimental and must be mitigated for robust applications in space, military, and nuclear industries.
- Use radiation hardening by design techniques to modify various logic circuits for reliable operation in radiation environments

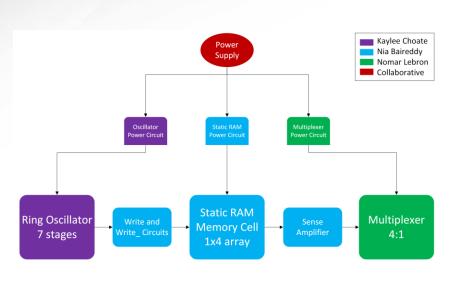








Project/Subsystem Overview



- Resilient wide bandgap material (GaN)
- Hardened components
 - Low resistance wirewound resistors
 - Multi-layer ceramic capacitors
- Alternative circuit layout
 - NMOS only
 - Trace width
 - Trace spacing

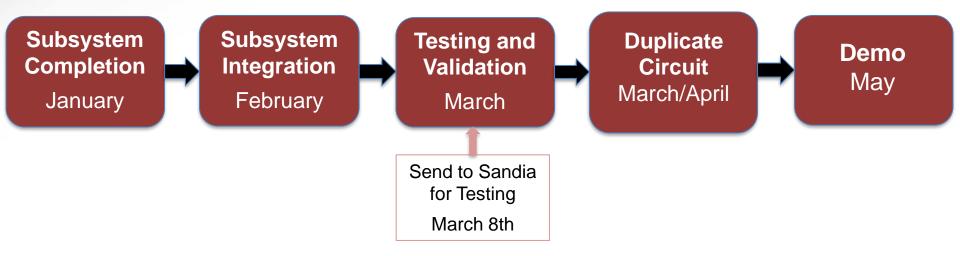


Major Project Changes for 404

- Condense PCB Designs
 - Implement 3 designs into 1 integrated PCB design
- Single power supply
 - Subsystem power circuits to distribute from single supply
- Additional subcircuits and circuit elements
 - Gate drivers
 - RC snubber



Project Timeline





Seven-Stage Ring Oscillator

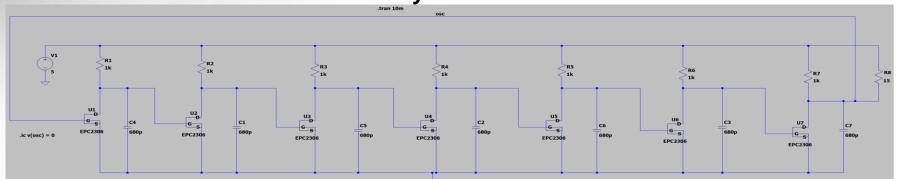
Kaylee Choate

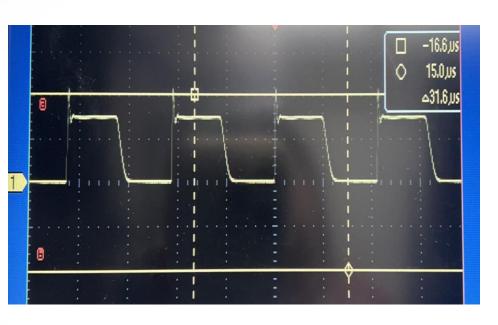
| Accomplishments since 403 ~5 hrs of effort | Ongoing progress/problems and plans until the next presentation | | | | | | | |
|---|---|--|--|--|--|--|--|--|
| Circuit oscillates as expected Researched implementation of RC snubber | Addition of RC snubber onto PCB schematic | | | | | | | |

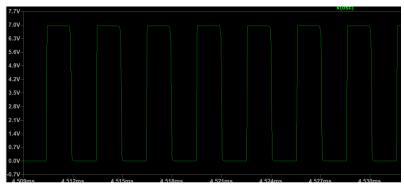


Seven-Stage Ring Oscillator

Kaylee Choate











1x4 SRAM Cell Array

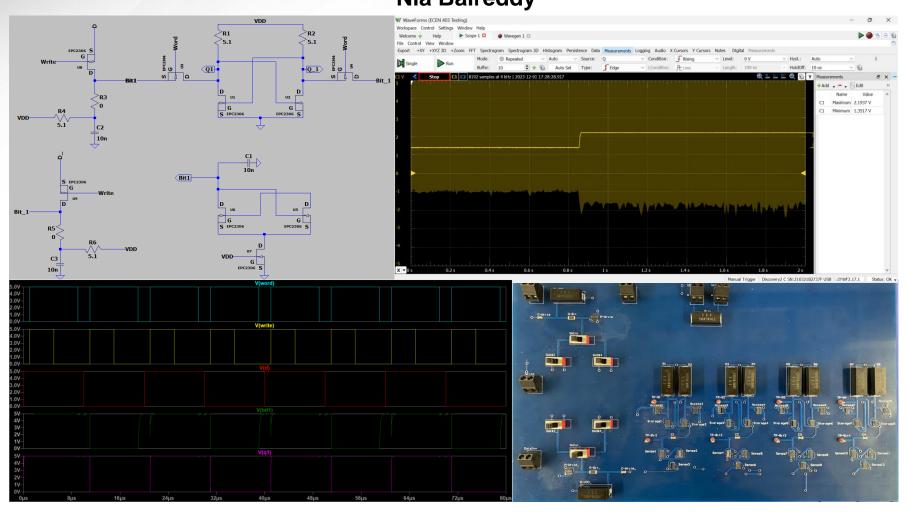
Nia Baireddy

| Accomplishments since 403 ~5 hours of effort | Ongoing progress/problems and plans until the next presentation |
|--|---|
| Verified circuit behavior | Implement gate driver subcircuits (simulations then board) |
| Researched GaN FET source to ground design | modifications) |
| Researched gate driver implementations | |



1x4 SRAM Cell Array

Nia Baireddy





4:1 Multiplexer

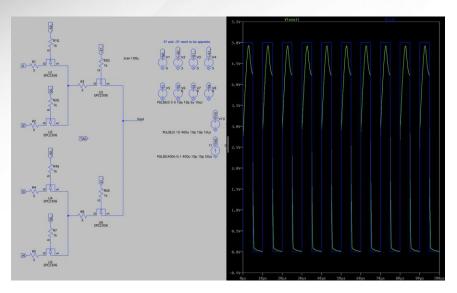
Nomar Lebron

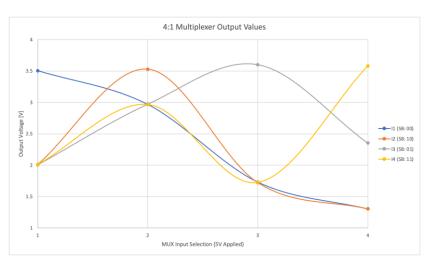
| Accomplishments since 403 ~5 hrs of effort | Ongoing progress/problems and plans until the next presentation | | | | | | | |
|---|---|--|--|--|--|--|--|--|
| Circuit Switches Between Inputs As Expected | Implement gate driver to fix data stability | | | | | | | |
| Research Gate Drivers | Begin researching LEDs for user interface | | | | | | | |
| Research Source to Ground Design | | | | | | | | |

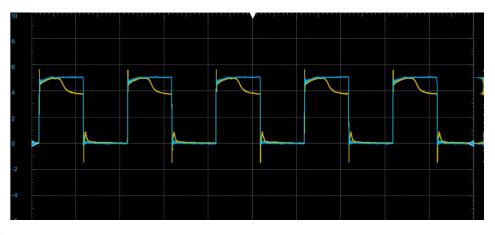


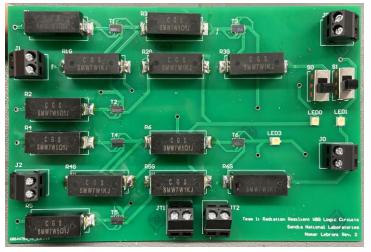
4:1 Multiplexer

Nomar Lebron











Parts Ordering Status

- Order EPC 2306 Transistors
- Order Wire-Wound Resistors & Multi-Layer Ceramic Capacitors
- Order 2 Fully Implemented Printed Circuit Boards
- Expected to receive them by mid-February



Execution Plan

| | 1/17 | 1/2/ | 1/31 | 2/7 | 2/1/ | 2/21 | 2/28 | 3/6 | 3/20 | 3/27 | 1/2 | 4/10 | 4/17 | 1/24 |
|-------------------------------------|------|------|------|-----|------|------|------|-----|------|------|-----|------|------|------|
| Validata Culturataria Functionalita | 1/1/ | 1/24 | 1/31 | 2// | 2/14 | 2/21 | 2/20 | 3/0 | 3/20 | 3/2/ | 4/3 | 4/10 | 4/1/ | 4/24 |
| Validate Subsystem Functionality | | | | | | | | | | | | | | |
| Status Update 1 | | | | | | | | | | | | | | |
| Update Subsystem Designs | | | | | | | | | | | | | | |
| Plan Integrated System Design | | | | | | | | | | | | | | |
| Design Integrated System in LTSpice | | | | | | | | | | | | | | |
| Status Update 2 | | | | | | | | | | | | | | |
| Design Integrated System in Altium | | | | | | | | | | | | | | |
| Order PCB and Parts | | | | | | | | | | | | | | |
| Status Update 3 | | | | | | | | | | | | | | |
| Assemble PCB | | | | | | | | | | | | | | |
| Testing and Validation | | | | | | | | | | | | | | |
| Deliver to Sandia | | | | | | | | | | | | | | |
| Status Update 4 | | | | | | | | | | | | | | |
| Duplicate PCB Assembly | | | | | | | | | | | | | | |
| Status Update 5 | | | | | | | | | | | | | | |
| Duplicate Testing and Validation | | | | | | | | | | | | | | |
| Final Report | | | | | | | | | | | | | | |
| Final Demo | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| Completed | | | | | | | | | | | | | | |
| In Progress | | | | | | | | | | | | | | |
| Behind Schedule | | | | | | | | | | | | | | |
| Not Started | | | | | | | | | | | | | | |

Thanks and Gig 'Em!

Questions?