



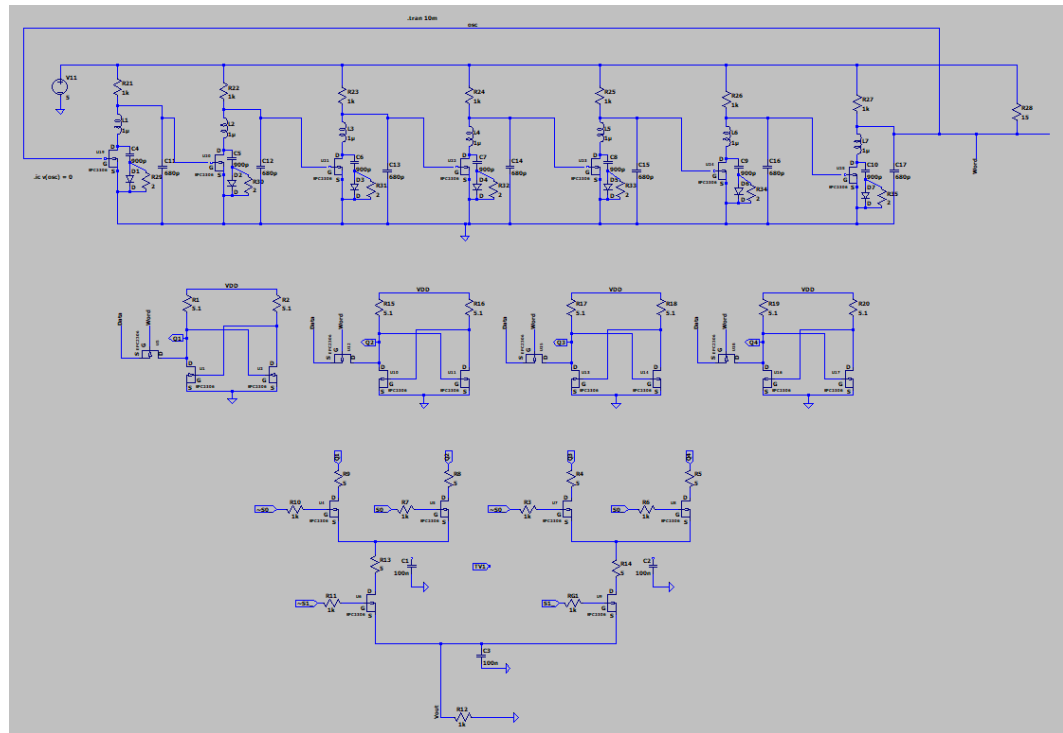
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Team 1: Radiation Resilient Logic Circuit Study with WBG Devices Bi-Weekly Update 2

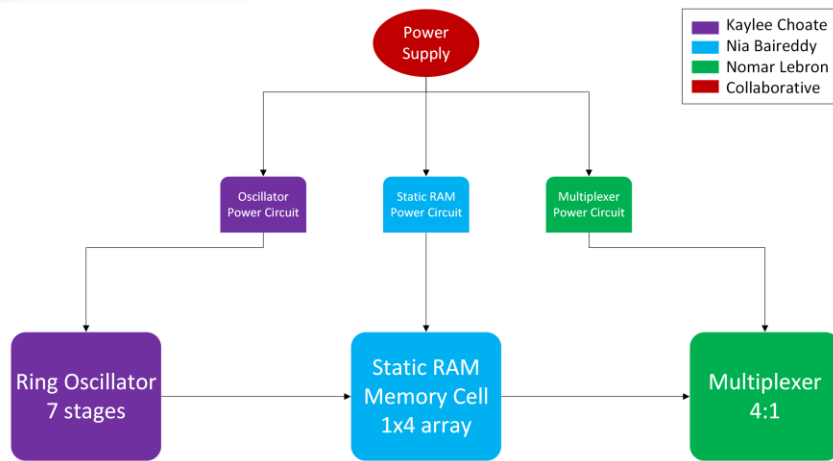
Nia Baireddy, Kaylee Choate, Nomar Lebron
Sponsor: Sandia National Laboratory
TA: Eric Robles

Project Summary and Solution

- Radiation effects on circuits are detrimental and must be mitigated for robust applications in space, military, and nuclear industries.
- Use radiation hardening by design techniques to modify various logic circuits for reliable operation in radiation environments.



Project/Subsystem Overview



- Radiation resilient wide bandgap material (GaN)
- Hardened components
 - Low resistance wirewound resistors
 - Multi-layer ceramic capacitors
- Alternative circuit layout
 - NMOS only
 - Trace width
 - Trace spacing



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Project Timeline

**Subsystem
Completion**
January

**Subsystem
Integration**
February

**Testing and
Validation**
March

**Duplicate
Circuit**
March/April

Demo
May

Send to Sandia
for Testing
March 8th



Seven-Stage Ring Oscillator

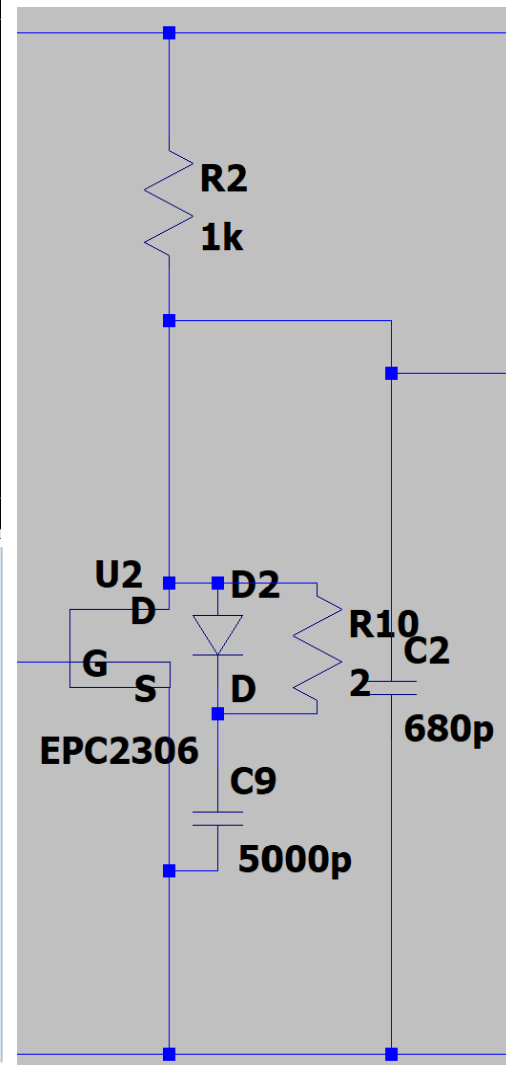
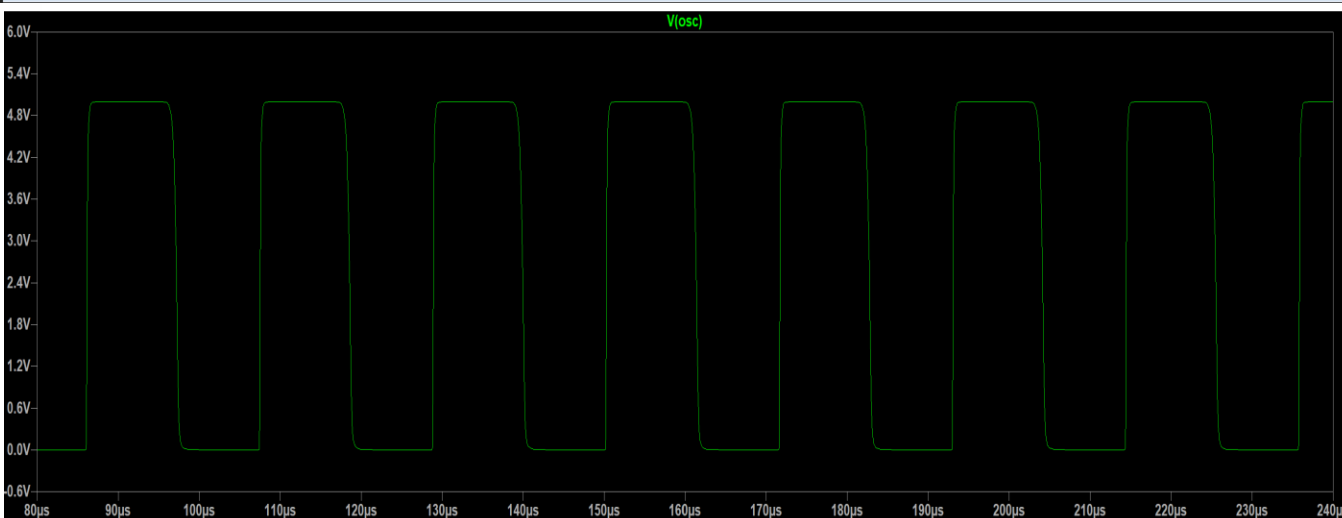
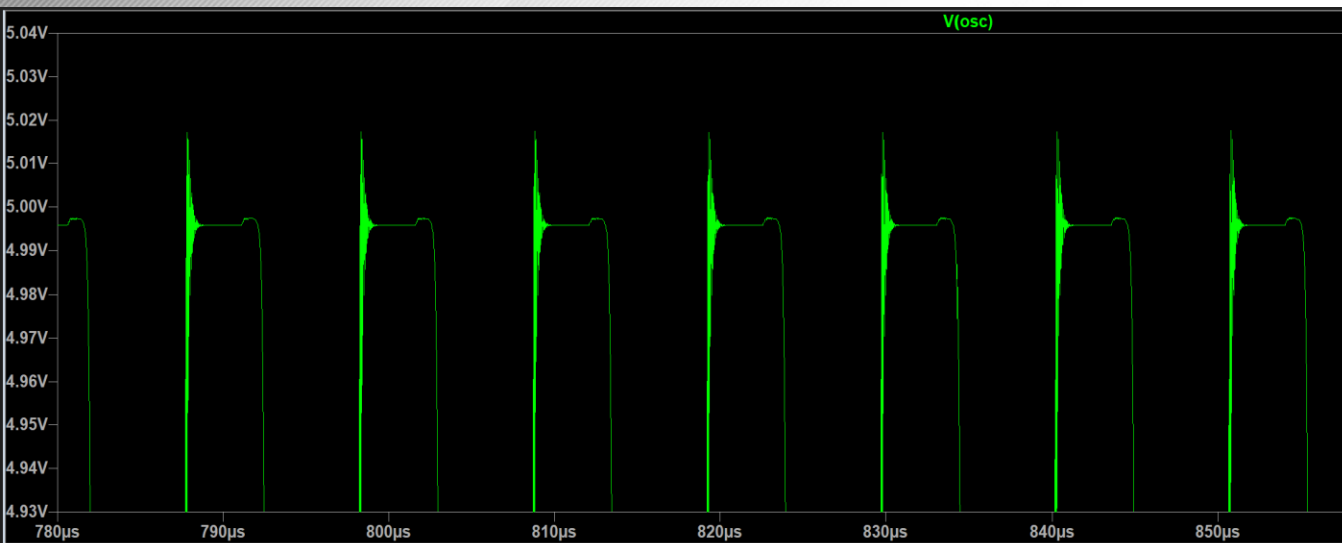
Kaylee Choate

Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
<ul style="list-style-type: none">• Simulated voltage spike in Itspice and corrected voltage spike by adding RCD snubber• Added RCD snubber to PCB design and ordered PCB for testing in preparation for integration	<ul style="list-style-type: none">• Assemble PCB/Test resistor and capacitor values• Finish integrated system simulation on LTSpice• Start integrated Altium PCB



Seven-Stage Ring Oscillator

Kaylee Choate



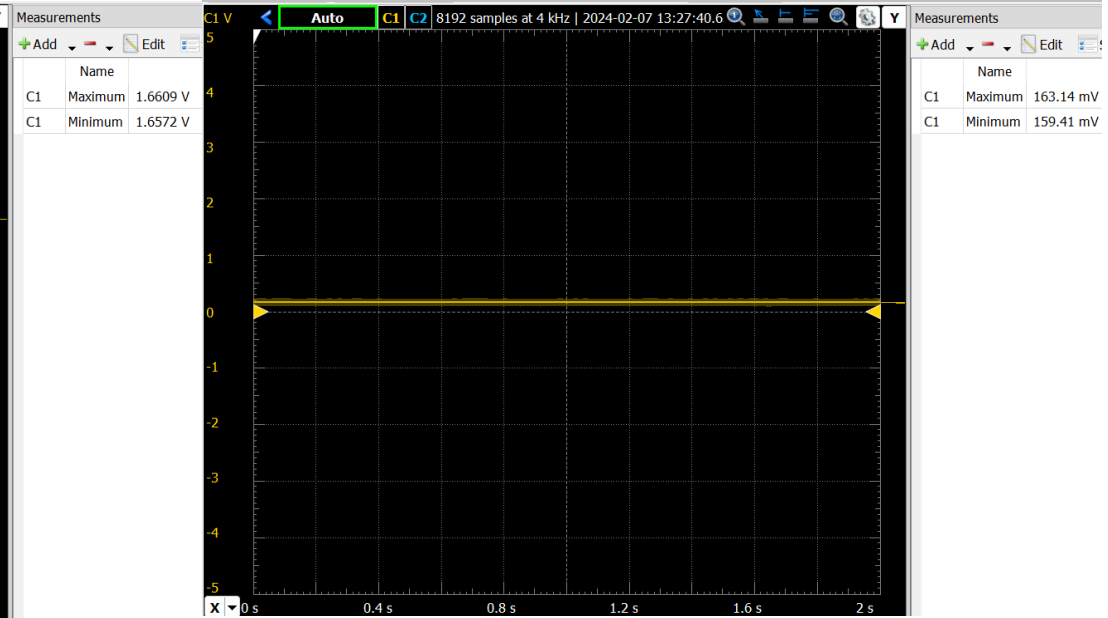
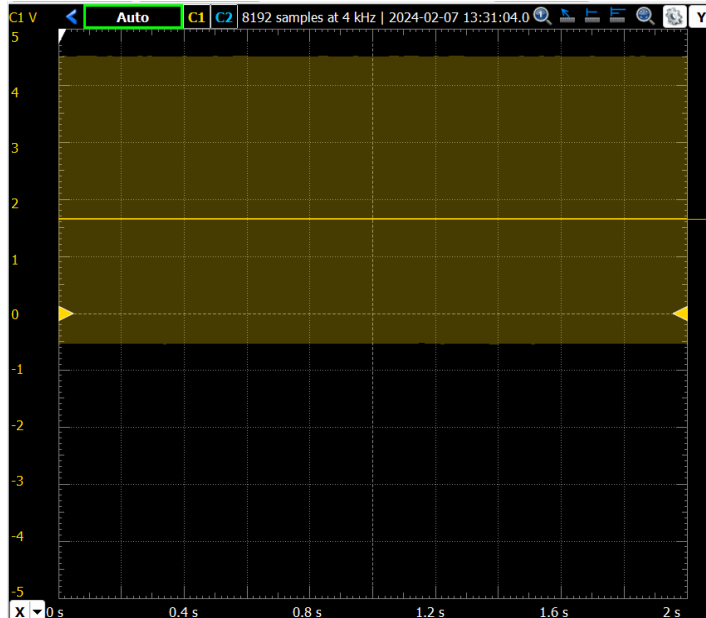
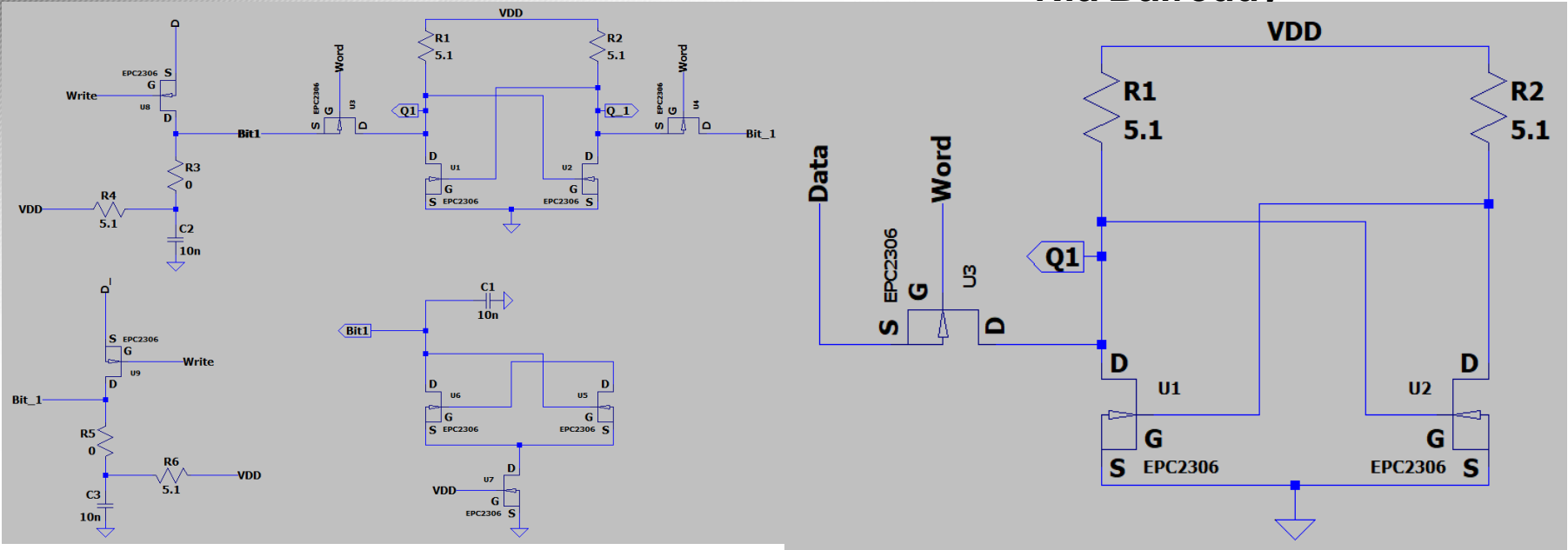
1x4 SRAM Cell Array

Nia Baireddy

Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
<ul style="list-style-type: none"> • Modified PCB and verified correct circuit behavior in preparation for integration • Worked on preliminary integrated design • Began design for subsystem power circuitry for integrated system power distribution 	<ul style="list-style-type: none"> • Finish integrated system simulations in LTSpice • Start integrated Altium PCB • Compile additional parts list for integrated system

1x4 SRAM Cell Array

Nia Bairedv





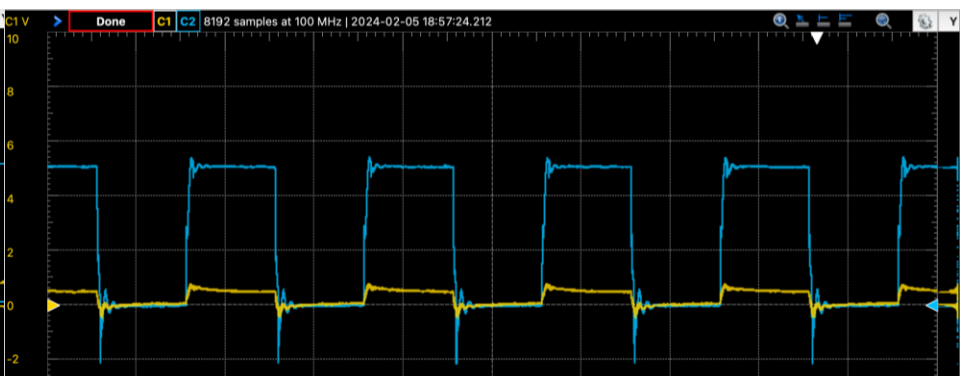
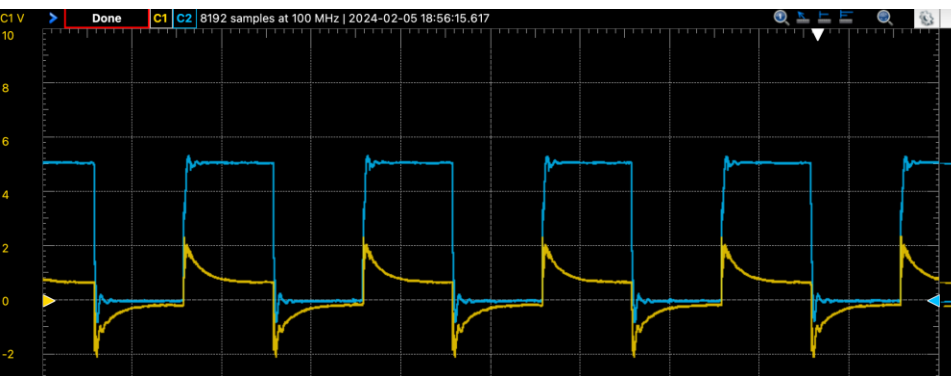
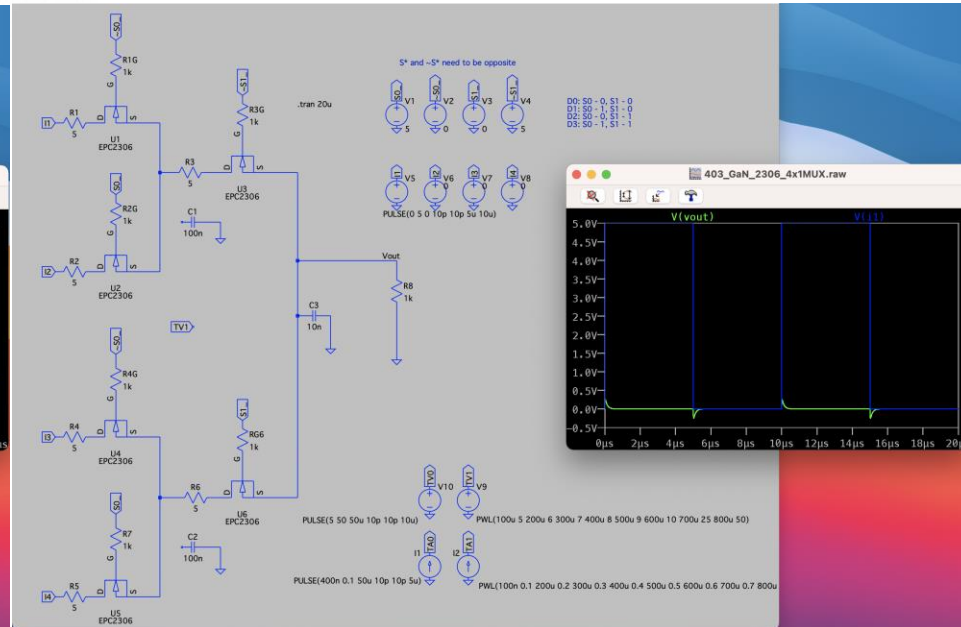
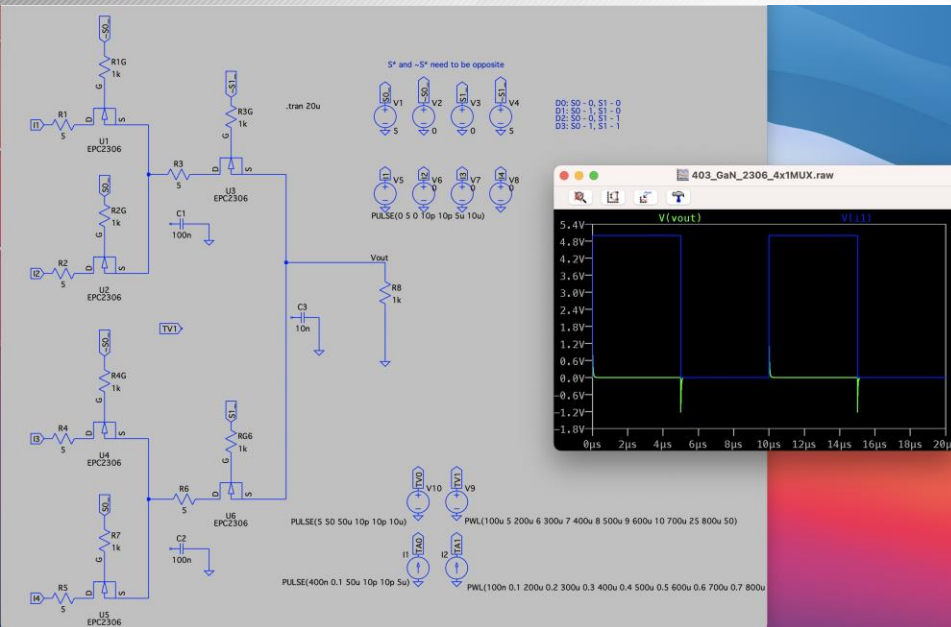
4:1 Multiplexer

Nomar Lebron

Accomplishments since last update 15 hrs of effort	Ongoing progress/problems and plans until the next presentation
<ul style="list-style-type: none">• Simulated voltage divider gate driver• Simulated decoupling capacitor• Tested decoupling capacitor on PCB in preparation for integration	<ul style="list-style-type: none">• Implement user interface LEDs for selection bits• Finish integrated system simulation on LTSpice• Begin integrated PCB design on Altium

4:1 Multiplexer

Nomar Lebron



Execution Plan

[illegible]

Thanks and Gig 'Em!

Questions?