Group #:

G

Final Project

Part 1

ENSC 350 2020

Last Name:

SID:

Last Name:

SID:

Last Name:

SID:

Last Name:

SID:

Table of Contents:

Final Project – Part 1

Part 1:

Main Objective:

1) To design a Logic Unit and Arithmetic Unit.
2) To perform Functional Verification on both units.
3) To Synthesise both units for a Cyclone IV FPGA.
4) To perform Timing Verification on both units.

Procedure:

Final Project (part 1) Setup:

Prepare your filing structure. (§Filing Structure)
Copy the files that I provide into the correct folders. (§Filing Structure)
Prepare your activity logging files. (§Activity Logging Procedure)
Prepare your Final Project Report (part 1) document. (§Documentation)
Prepare ModelSim project. (§Setting up ModelSim)
Prepare a Quartus Project. (§Setting up Quartus)

The Logic Unit:

Design the Logic Unit as shown in Lecture 7, handout page 6.
~~Write a Testbench~~. (§Creating a Testbench)
~~Create Test Vectors~~. (§Creating Test Vectors)
Run a Functional Simulation. (§Logic Unit - Functional Simulation)
Document the results of the Functional Simulation. (§Logic Unit – Saving Functional Waves)
Synthesise the Logic Unit and construct post-fit-Netlist and Timing files. (§Logic Unit – Synthesis)
Run Timing Simulation. (§Logic Unit - Timing Simulation)
Document the results of the Timing Simulation. (§Logic Unit – Saving Timing Waves)

The Arithmetic Unit:

Design the Arithmetic Unit as shown in Lecture 7, handout page 6,
The status signals can be formed either BEFORE or AFTER the MUX.
~~Write a Testbench~~. (§Creating a Testbench)
~~Create Test Vectors~~. (§Creating Test Vectors)
Run a Functional Simulation.
Document the results of the Functional Simulation.
Synthesise the Logic Unit and construct post-fit-Netlist and Timing files.
Run Timing Simulation.
Document the results of the Timing Simulation.

Complete the Final Project Report.
Prepare an archived package of all documents and submit to Canvas.

Filing Structure:

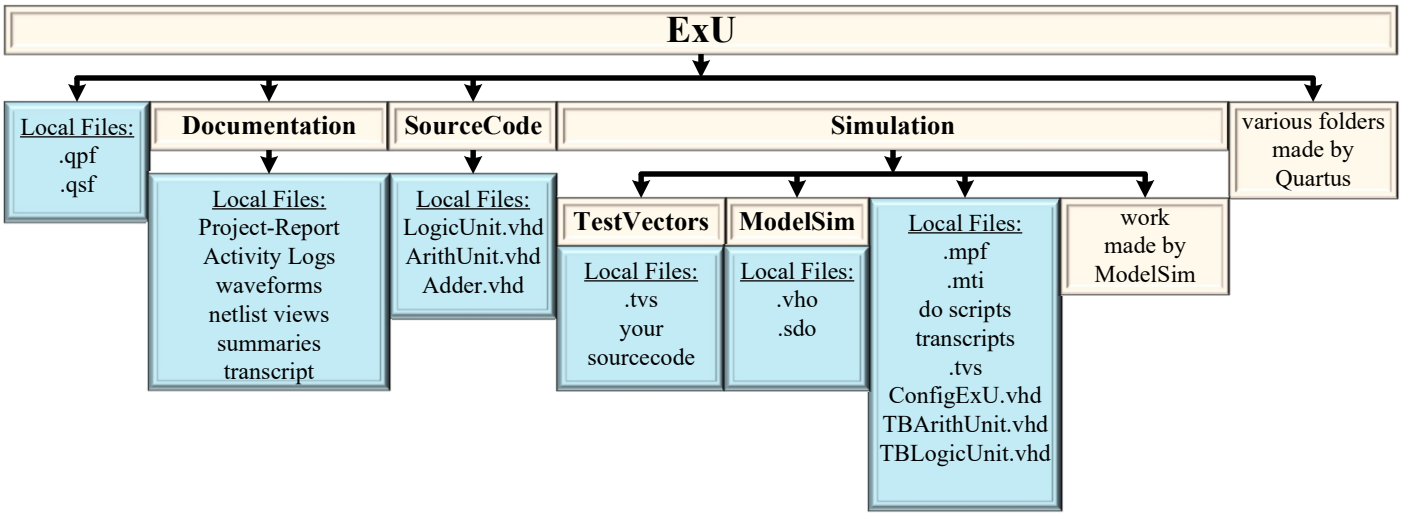
Create a tree of folders as shown.

Use the convention that files associated with the Logic Unit have the string "LogicUnit" or "**LU**" within their filename. Use the names that I specify to ensure that the scripts run smoothly.

Use the convention that files associated with the Arithmetic Unit have the string "ArithUnit" or "**AU**" within their filename. Use the names that I specify to ensure that the scripts run smoothly.

Testbenches have the same name as the entity that they test with the prefix "**TB**".

ExU: The top-level folder to be used as Quartus' project folder.
Documentation: Used to collect files needed for project documentation.
SourceCode: Used to store the synthesisable VHDL design files.
Simulation: Used a the ModelSim project folder.
ModelSim: Used by Quartus to store post-fit netlists and timing files.
TestVectors: Used by you to create Test Vectors using a programming language of your choice.



Files Provided:
unzip the archive, "FP1.1-350-1201.zip"

FP1-log-Gxx-xxxx-350-1201.xlsx → Documentation
WaveLogicUnit.do, WaveArithUnit.do → Simulation
ConfigExU.vhd, TBLogicUnit.vhd, TBArithUnit.vhd → Simulation
LogicUnit00.tvs, ArithUnit00.tvs → Simulation
FunctionalLogicUnit.do, TimingLogicUnit.do → Simulation
FunctionalArithUnit.do, TimingArithUnit.do → Simulation

Activity Logging Procedure:

Each group member must maintain a log of the work that they contribute to the project.
Each member should make a copy of the file "FP1-log-Gxx-xxxx-350-1201.xlsx"
Rename the file replacing the 'x's
in "Gxx" with your group numbers digits and
"xxxx" is replaced with the last four digits of your student ID number.

Write your group number, Name and Student ID in the top header.

You should create a log entries for all the time that you spend contributing to this project.

Whenever you begin a session, make note of the start time on a scrap piece of paper.
When working for extended periods, create a log entry approximately every two (or so) hours.
Whenever you take a break, make note of the end time, then create a log entry.

The descriptions should be short.
Break down your activities into small tasks.
Do not combine multiple tasks into a single log entry. Instead make multiple log entries.
Even a small task may have multiple entries because you take breaks.
When a single task has many entries, write "DONE" by the final entries description.

You should enter values for your last-4-digits in each entry. Do this every time, as I will be merging and sorting the entries for all group members.

If you become ill or are unable to continue contributing to the project, make a final brief entry noting this event. (A group member may make this entry on your behalf)

Documentation:

Full Documentation:

Your project documentation will contain many files. These files are to be zipped into a single archive called "FP1-Gxx-350-1201.zip"

The archive contents:

- Final project report
- VHDL sourcecode for all (three) design entities.
- 4 transcript files,
- A summary file – created by merging the four summary files.
- two – post-fit netlists (.vho)
- two – standard delay format files (.sdo)
- WaveLogicUnit.do and/or WaveArithUnit.do. (only if you modified them)

The Project Report:

You are to submit a Final Project Report, named "FP1-Report-Gxx-350-1201.pdf".

DO NOT add listings of your source code to the report.
Your report should be well organised. You choose how to divide the report into sensible sections.

You may wish to copy/paste specific statements from your VHDL sourcecode into the document.
If you use notepad++, you can copy the selected text to the clipboard with syntax highlighting.
Use the menu, Plugins->NppExport->Copy all formats to clipboard. You can also change the colours of the syntax highlighting using the menu, settings->style configurator. Then select the language VHDL (on the left) and choose your colours. I chose mine to best match the default colour of the ModelSim Editor.

Documenting Design Entities in the project report:

For each Design Entity, you should provide comprehensive information describing:

A paragraph describing the functional behaviour of the entity.

The VHDL interface (the entity declarations shown below).

(reference the name of the VHDL source file which is attached)

A circuit diagram for the entity.

(all labels must identically match your VHDL sourcecode.)

```
Entity ArithUnit is
Generic ( N : natural := 64 );
Port ( A, B : in std_logic_vector( N-1 downto 0 );
       Y : out std_logic_vector( N-1 downto 0 );
-- Control signals
       NotA, AddnSub, ExtWord : in std_logic := '0';
-- Status signals
       Cout, Ovfl, Zero, AltB, AltBu : out std_logic );
End Entity ArithUnit;
```

```
Entity Adder is
Generic ( N : natural := 64 );
Port ( A, B : in std_logic_vector( N-1 downto 0 );
       Y : out std_logic_vector( N-1 downto 0 );
-- Control signals
       Cin : in std_logic;
-- Status signals
       Cout, Ovfl : out std_logic );
End Entity Adder;
```

```
Entity LogicUnit is
Generic ( N : natural := 64 );
Port ( A, B : in std_logic_vector( N-1 downto 0 );
       Y : out std_logic_vector( N-1 downto 0 );
       LogicFN : in std_logic_vector( 1 downto 0 ) );
End Entity LogicUnit;
```

Documenting the Testbenches in the project report:

For Part 1, I have written the testbenches on your behalf.

You do not need to include documentation of the testbenches for part 1.

Documentation of a testbench should include

a diagram of the processes and signals within the architecture,

a description of the flow for the procedure STIM: (maybe including a flowchart)

and a description of the choice of Test Vectors.

Documenting Simulation Runs:

Simulation runs are to be with documented with the following content.

Transcript files:

The scripts that I provided produce transcript files,

FuncLogicUnitTranscript.txt,
FuncArithUnitTranscript.txt,
TimeLogicUnitTranscript.txt and
TimeArithUnitTranscript.txt,

All four transcript files should be included in your submitted archive.

Documenting Simulation Waves:

You should also make screen clippings of the waveforms.

You should capture a set of waveforms from each of the four simulation runs.

I have setup signals to display in the files waveLogicUnit.do and waveArith.do

These files are read by the four simulation run scripts.

You may wish to add internal signals from your entity.

You may wish to make change the colours of the waveforms.

You decide how best to effectively convey useful information.

When the wave window is active, type <ctrl-s> and save the changes, overwriting my file.

If you change the waveforms, then include the modified .do file in your submitted archive.

The simulation waveforms should be sensibly included in your project report, with titles and annotations. Use two images per landscape page as shown in the example on the next page.

Each set should be accompanied with a discussion that explains why this simulation run verifies the functional behaviour and timing of the tested entity. The highlights on the images should be chosem to enhance this discussion.

To make the good images,

Undock the wave window so that is occupies a large amount of the screen.

Resize the window. Adjust the bottom so that the time-axis is close to the bottommost waveform.

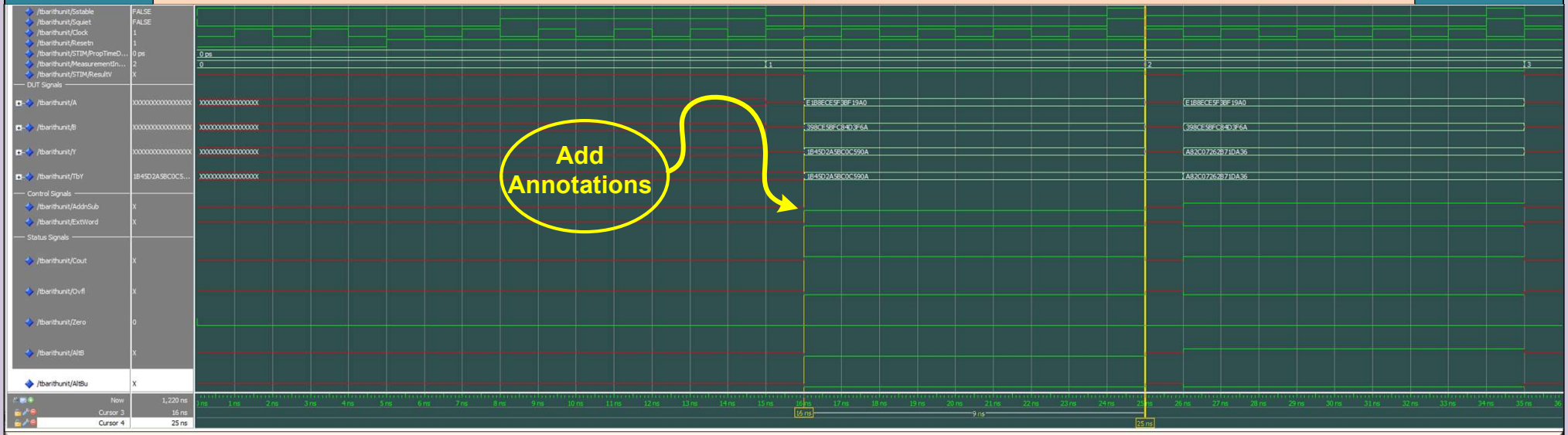
Type “r” - to select the zoom range specified in the procedure.

Add measurement cursors as specified in the procedure.

Clip the image - <window+shift+S>, then

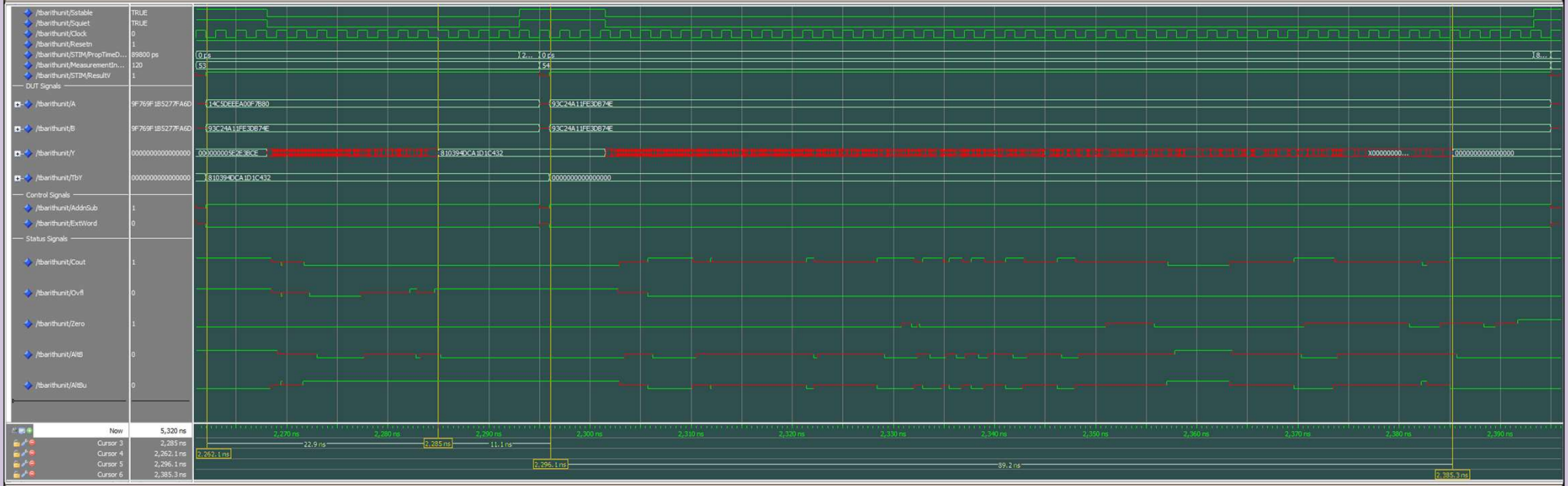
Paste the image to a file in the Documentation folder. <ctrl+shift+alt+V>

The following page shows an example of some captures.



Functional Simulation - ArithUnit:

add some description of which measurements are being observed. Also the placement of the cursors. Add annotations to the wave.



Timing Simulation - ArithUnit:

Add a brief description. Measurement 53, t_{pd} = 22.9 ns, Measurement 54, t_{pd} = 89.2 ns

Documenting Synthesis and Fitting:

Using Quartus you will synthesise and fit your design entities. Quartus will produce summary reports which you should be included in your submitted archive.

Summary file: "FP1-Summary-Gxx-350-1201.txt"

Merge the four summary files into a single file.

Insert title lines to ensure that the individual summary reports are easily distinguishable.

LogicUnit.map.summary,
ArithUnit.map.summary,
LogicUnit.fit.summary,
ArithUnit.fit.summary,

Screen Clipping from Netlist viewers:

You will need to collect screen clipping from the RTL netlist viewer and the Post-fitting netlist viewer.

These images should be included in the project report. (Refer to the example)

For the Logic Unit you may only need two wisely selected clippings from each viewer.

For the Arithmetic Unit you may need more clipping.

You decide how many is reasonable. Remember too many is BAD, not enough is also BAD.

You will be judged on your ability to sensible choose these images. You will score zero if it is clear that you are not making any effort to graphically convey useful information about the underlying circuit.

Refer to the example on the next page.

Documenting VHDL Sourcecode for the Design Entities:

The VHDL sourcecode files are included separately from the project report. The project report simply references the code by filename.

Your VHDL sources files must contain useful comments. When commenting your code, imagine that you were reading the text in the distant future. Consider the comments as notes to yourself so that you could efficiently continue working on the project.

Documenting post-fit netlists and timing information:

Include in your submitted archive, the post-fit netlist files,

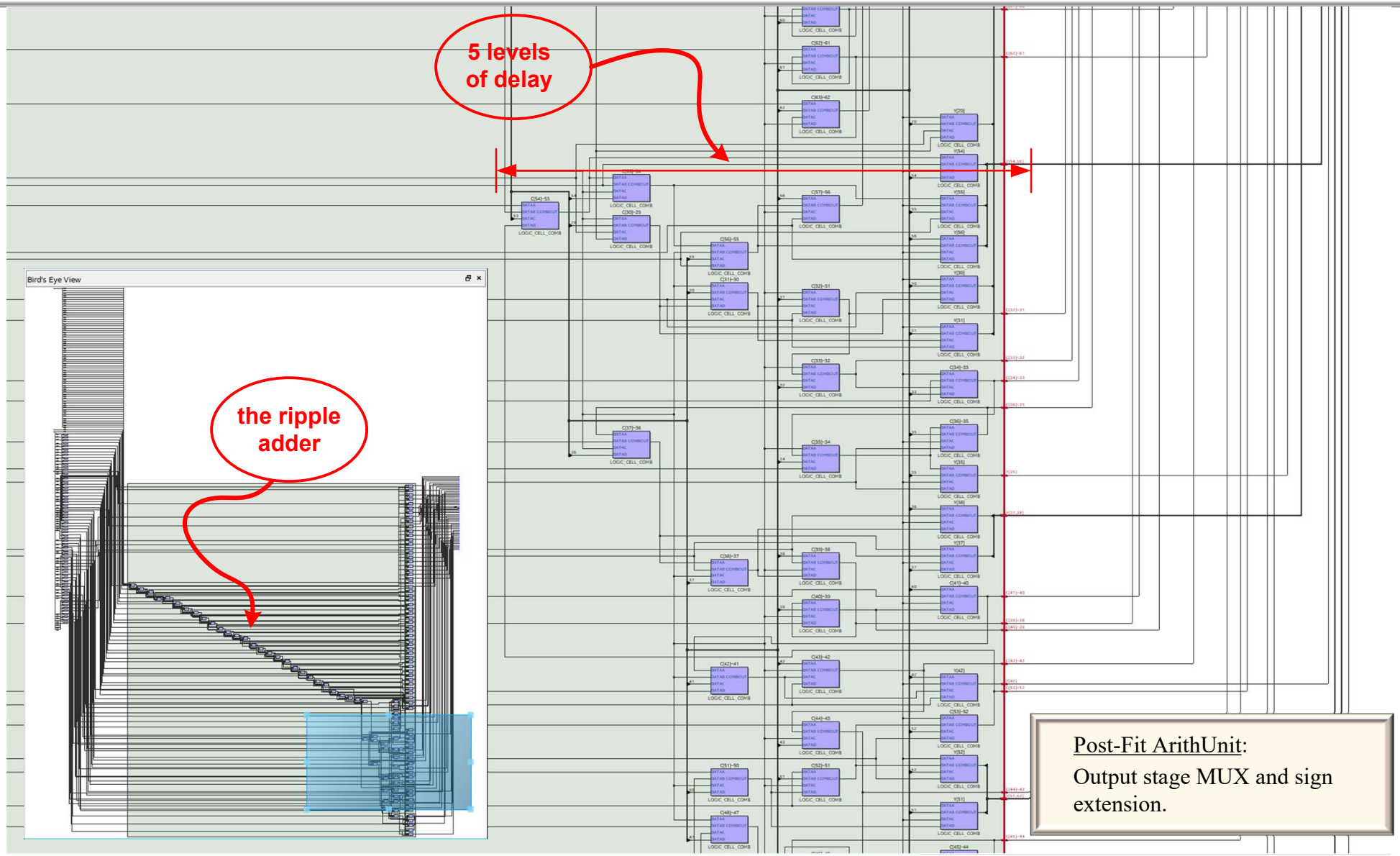
"LogicUnit.vho" and "ArithUnit.vho" and

the standard delay format files,

"LogicUnit.sdo" and "ArithUnit.sdo".

Final Project – Part 1

Each screen clipping from a netlist viewer should occupy a full page so that details are not lost. (Here is an example)
Choose the page to be either landscape or portrait, whichever best matches the aspect ratio of your image.
Each image should have a title and a brief description. The image should contain both the zoomed view and the window for the bird's eye view.
Position and size the bird's eye window so that it doesn't obscure too much of the zoomed circuit. Choose the zoomed region wisely.



Setting up ModelSim:

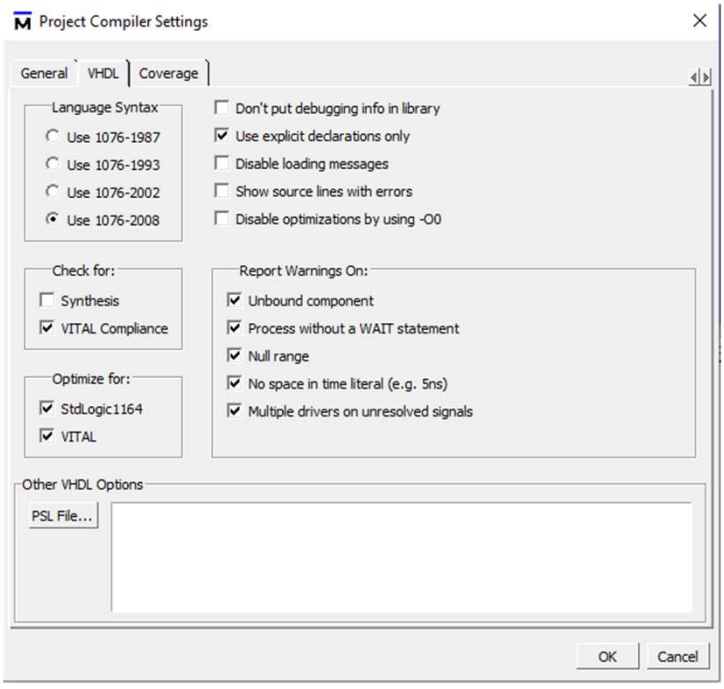
~~Create an Environment variable set to the project folder \ExU\.~~
~~Edit the four scripts so that the file reference use the local path on your computer. I couldn't make the environment variables work so you'll have to do this manually for now~~.

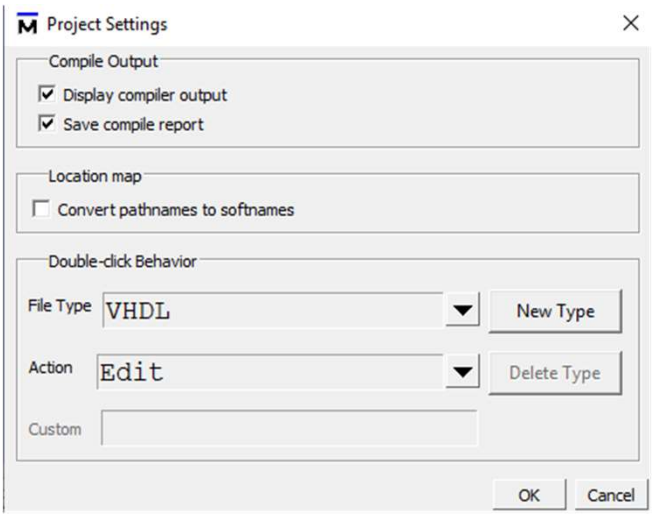
Start ModelSim
To ensure that you can start ModelSim by double-clicking on a ModelSim Project file (.mpf) use the menu help->register filetypes. (you will need to restart the OS)

The testbenches use File I/O which requires VHDL 2008 compatibility. You can check a source files setting by <right-click>->properties to bring up the dialog. Make sure that VHDL-2008 is selected. This may not be necessary because the scripts explicitly request 2008 compilation.

Make sure that the project generates full compiler reports.
With project pane active,
select menu, project->project settings.
Make sure that both compiler flags, are ON

You can create custom keyboard short cuts using the menu window->keyboard shortcuts.
Save the project called ExU.mpf in the folder /Simulation/ .
Quit ModelSim and restart your OS.
From now on always start ModelSim using the project icon, "ExU.mpf".



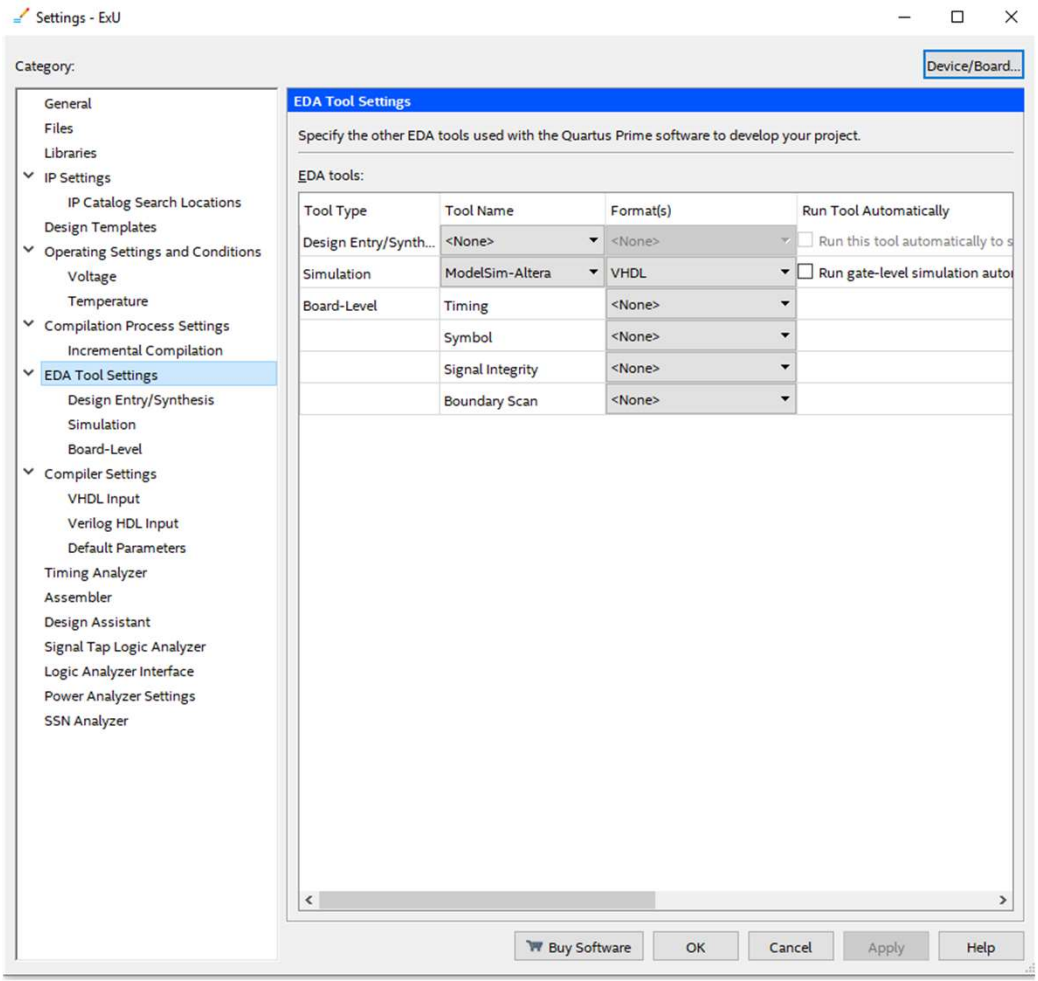


Setting up Quartus:

Use a single Quartus project for all activities. Use the folder /ExU/ as the Quartus project folder.

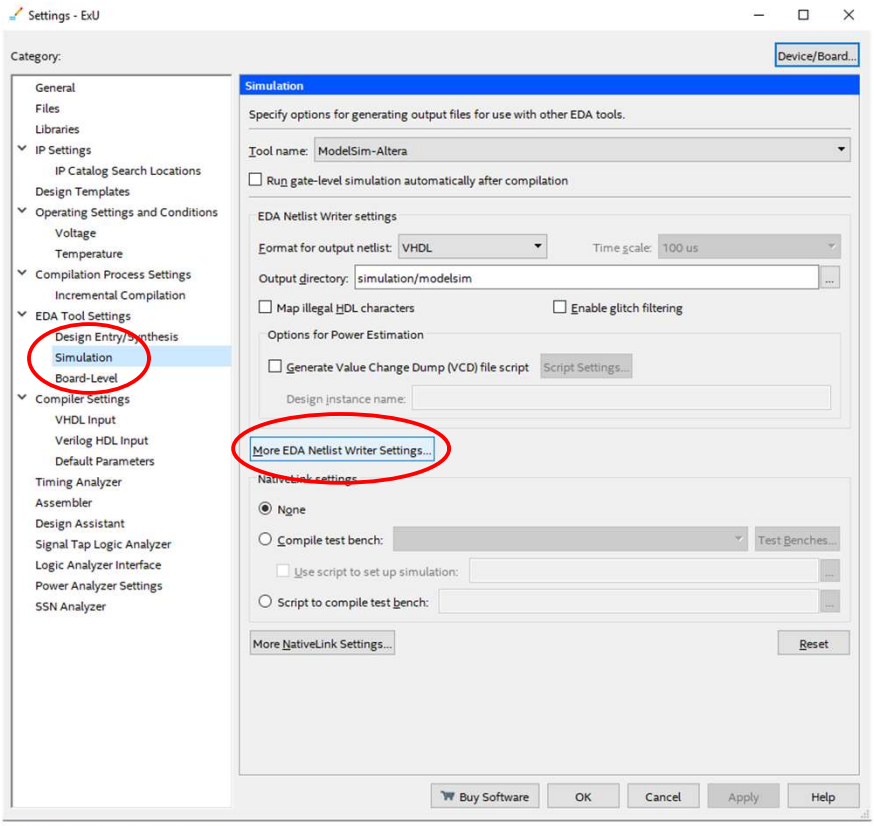
Start Quartus.
Make a new project using a Cyclone IV FPGA. – EP4CE115F29C7

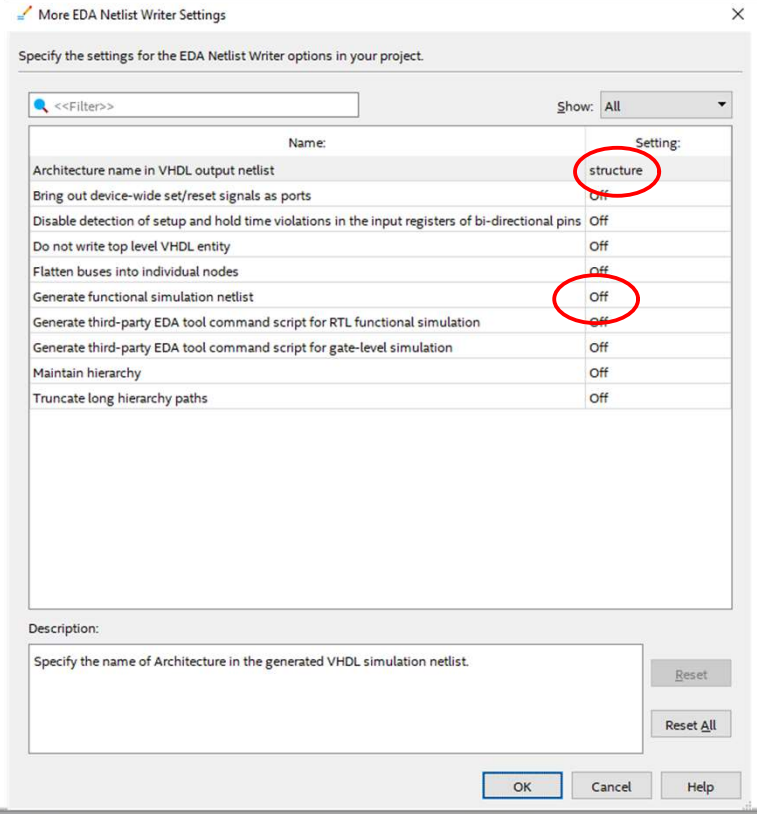
Under the EDA tool settings, choose ModelSim-Altera, format is VHDL
do not enable – "run gate-level
You can also activate this dialog by double-clicking the EDA Netlist writer – Edit settings.



Select EDA tool Settings – Simulation

Click – More EDA Netlist Writer Settings – turn **OFF** "Generate functional simulation netlist"





Close Quartus.

From now on always start Quartus by double-clicking on the project icon "ExU.qpf"

Create a Testbench:

I have created two testbenches on your behalf.
"TBLogicUnit.vhd" - used for both Functional Verification and Timing Simulation.
"TBArithUnit.vhd" - used for both Functional Verification and Timing Simulation.

- The AltB and AltBu are not tested unless the operation is a 64-bit subtraction.

"ConfigExU.vhd" - contains four VHDL configuration declarations.
Once compiled, the VHDL configurations will appear in ModelSim's work library. When starting a simulation, we select a configuration as the top-level, not the testbench.
You don't need to worry about this subtlety as the configurations are automatically selected by the scripts.

The testbenches use file i/o functions that became standard in VHDL-2008.

Study the testbenches as you will be creating your own testbenches one day.
If a measurement fails, you will see a blue message in the ModelSim command window.
A message "Simulation Complete" once the last measurement has run.

Don't modify the testbenches.
The only item that may need changing is the constant *PostStimTime*, at the top. This constant is used to wait for a stable result at the output.
When an output result is stable, the propagation delay is measured and the loop continues to the next measurement. You design may have weird periods of stable but incorrect intermediate garbage. It this is the case you can simply extend the *PostStimTime*.

Creating Test Vectors:

The testbenches read input stimuli from rows of a text file. These rows are called Test Vectors.
Using File I/O is quite useful because you can use any programming language to create the test vectors. It is very common to use an interpreted (not compiled) language such as Matlab or Python.

The order of the characters in the row is very important. The data elements must match the statements in the testbench.

- ArithUnit00.tvs – calculates status signals AFTER the MUX.
- ArithUnit01.tvs – calculates status signals BEFORE the MUX.

Logic Unit - Functional Simulation:

I assuming that you have created a VHDL design for the Logic Unit and added the file to the ModelSim project. (Lecture 7 – handout page 6.)
The Entity declaration is given
(§Documentation – Documenting Design Entities in the project report)

Add the Testbench and Configuration to the project.

Make sure that the Architecture is called "rtl"
A configuration declaration will bind entities/architectures to components. I have assumed that the architectures used for functional simulation are called "rtl" while the architectures used for timing simulation are called "structure" (as specified by Quartus)

Run the script by typing "do FunctionalLogicUnit.do" in the ModelSim command window.
The script "FunctionlLogicUnit.do"
compiles "LogicUnit.vhd", "TbLogicUnit.vhd" & "ConfigExU.vhd",
loads the simulator using the configuration, FuncLUSim,
sets up wave window using "waveLogicUnit.do",
run the simulation for 6500 ns,
results are written to "FuncLogicUnitTranscript.txt"

Check that no measurement errors have been asserted and that the window only displays "Simulation Complete".
Also check that you can see the last measurement, **#772** at the end of the run.
If you have measurements errors, you will need to debug.

Logic Unit – Saving Functional Waves:

Using the procedure described in §Documentation – Documenting Simulation Waves:
Make images
1) from t = 0 to 70 ns (after measurement #8)
2) from beginning of measurement #458 to end of measurement #464
3) from beginning of measurement #770 till 5 ns after the start of measurement #772.

Save these images using the filenames "waveFLU1.png", "waveFLU2.png" & "waveFLU3.png"

Logic Unit – Synthesis:

Start Quartus using the project file icon.
Add your design entity, "LogicUnit.vhd" to the project. Set this entity as the top-level entity.
Run a full synthesis, <ctrl-L>
Resolve any issue that make you unhappy. You will need to correct your VHDL sourcecode if your design is not synthesisable. Once these changes are made you must return to ModelSim and repeat the procedures for functional simulation.

Once the your design is both functional and synthesisable, run the full synthesis. <ctrl-L>

Verify that the folder ExU/Simulation/ModelSim/ now contains "ExU.vho" and "ExU_vhd.sdo".
The .vho files are VHDL models for your design after place-and-route on a Cyclone IV FPGA. The .sdo files contain the timing information for the logic elements and wires that were used by your design.
Rename these files, "LogicUnit.vho" and "LogicUnit.sdo".

Rename the summary files, "ExU.map.summary" and "ExU.fit.summary" to "LogicUnit.map.summary" and "LogicUnit.fit.summary".
Move these files to the /Documentation/ folder.
(§Documentation – Documenting Synthesis & Fitting)

Every time we use Quartus to create post-fit models we will need to rename the files as Quartus will always use the project name for these files.

Using the RTL netlist viewer capture images of the RTL synthesised circuit.
Using the post-fitting Netlist viewer capture images of circuit using FPGA elements.
(§Documentation – Documenting Synthesis & Fitting)

Using any text editor, open the netlist and verify that Quartus named the architecture "structure".
Close the netlist file and close Quartus.

Logic Unit - Timing Simulation:

Start ModelSim.
Add the file "LogicUnit.vho" to the project.
Run the script "TimingLogicUnit.do"

Run the script by typing "do TimingLogicUnit.do" in the ModelSim command window.
The script "TimingLogicUnit.do"

compiles "LogicUnit.vho", "TbLogicUnit.vhd" & "ConfigExU.vhd",
loads the simulator using the configuration, TimeLUSim,
sets up wave window using "waveLogicUnit.do",
run the simulation for 15600 ns,
results are written to "TimeLogicUnitTranscript.txt"

By observing the blue text in the command window, you should see the message, "Back Annotation Successfully Completed" when the simulator loads and when it is restarted.
This means that the .sdo file was successfully read and the timing information was mapped to the VHDL generic within the timing model.

Check that no measurement errors have been asserted and that the window only displays "Simulation Complete".
Also check that you can see the last measurement, #772 at the end of the run.
If you have measurements errors, you will need to debug.

The simulation is now running with timing delays that were accurately measured by the manufacturer of the Cyclone IV FPGA.

Logic Unit – Saving Timing Waves:

Using the procedure described in §Documentation – Documenting Simulation Waves:
Make images

1) from t = 0 to a few ns into the beginning of measurement #2
   Place two cursors that measure the propagation delay of measurements #1.
2) from beginning of measurement #400 to end of measurement #416
   Delete all cursors.
3) from beginning of measurement #772 till 5 ns after the end of measurement #772.
   Place two cursors that measure the propagation delay of measurements #772.

Save these images using the filenames "waveTLU1.png", "waveTLU2.png" & "waveTLU3.png"

Arithmetic Unit - Functional Simulation:

Design the Arithmetic Unit. (Lecture 7 – handout page 6.)
Design a simple ripple adder in a separate file called "Adder.vhd". We can change the design later if we find that we need a faster adder. Instantiate the adder within the ArithUnit entity.
The Entity declarations are given
(§Documentation – Documenting Design Entities in the project report)
Make sure that the Architectures are called "rtl"
Add both entities to the ModelSim project.

Add the Testbench "TBArithUnit.vhd" to the ModelSim project.

Run the script by typing "do FunctionalArithUnit.do" in the ModelSim command window.
The script "FunctionlArithUnit.do"
compiles "Adder.vhd", "ArithUnit.vhd", "TbArithUnit.vhd" & "ConfigExU.vhd",
loads the simulator using the configuration, FuncAUSim,
sets up wave window using "waveArithUnit.do",
run the simulation for 1220 ns,
results are written to "FuncArithUnitTranscript.txt"

Check that no measurement errors have been asserted and that the window only displays "Simulation Complete".
Also check that you can see the last measurement, **#120** at the end of the run.
If you have measurements errors, you will need to debug.

Arithmetic Unit – Saving Functional Waves:

Using the procedure described in §Documentation – Documenting Simulation Waves:
Make images
1) from t = 0 to 76 ns (after measurement #6)
2) from beginning of measurement #61 to end of measurement #66
3) from beginning of measurement #118 till 5 ns after the start of measurement #120.

Save these images using the filenames "waveFAU1.png", "waveFAU2.png" & "waveFAU3.png"

Arithmetic Unit – Synthesis:

Start Quartus using the project file icon.
Add your design entities, "ArithUnit.vhd" and "Adder.vhd" to the project.
Set ArithUnit as the top-level entity.
Run a full synthesis, <ctrl-L>

Resolve any issue that make you unhappy. You will need to correct your VHDL sourcecode if your design is not synthesisable. Once these changes are made you must return to ModelSim and repeat the procedures for functional simulation.

Once the your design is both functional and synthesisable, run the full synthesis. <ctrl-L>

Verify that the folder ExU/Simulation/ModelSim/ now contains "ExU.vho" and "ExU_vhd.sdo".
Rename these files, "ArithUnit.vho" and "ArithUnit.sdo".

Rename the summary files, "ExU.map.summary" and "ExU.fit.summary" to "ArithUnit.map.summary" and "ArithUnit.fit.summary".
Move these files to the /Documentation/ folder.
(§Documentation – Documenting Synthesis & Fitting)

Using the RTL netlist viewer capture images of the RTL synthesised circuit.
Using the post-fitting Netlist viewer capture images of circuit using FPGA elements.
(§Documentation – Documenting Synthesis & Fitting)

Using any text editor, open the netlist and verify that Quartus named the architecture "structure".
Close the netlist file and close Quartus.

Arithmetic Unit - Timing Simulation:

Start ModelSim.
Add the file "ArithUnit.vho" to the project.
Run the script "TimingArithUnit.do"

Run the script by typing "do TimingArithUnit.do" in the ModelSim command window.
The script "TimingArithUnit.do"

compiles "ArithUnit.vho", "TbArithUnit.vhd" & "ConfigExU.vhd",
load simulator using the configuration, TimeAUSim,
sets up wave window using "waveArithUnit.do",
run the simulation for 15600 ns,
results are written to "TimeArithUnitTranscript.txt"

By observing the blue text in the command window, you should see the message, "Back Annotation Successfully Completed" when the simulator loads and when it is restarted.
This means that the .sdo file was successfully read and the timing information was mapped to the VHDL generic within the timing model.

Check that no measurement errors have been asserted and that the window only displays "Simulation Complete".
Also check that you can see the last measurement, **#120** at the end of the run.
If you have measurements errors, you will need to debug.

The simulation is now running with timing delays that were accurately measured by the manufacturer of the Cyclone IV FPGA.

Arithmetic Unit – Saving Timing Waves:

Using the procedure described in §Documentation – Documenting Simulation Waves:
Make images

1) from t = 0 to a few ns into the beginning of measurement #2
   Place two cursors that measure the propagation delay of measurements #1.
2) from beginning of measurement #61 to end of measurement #66
   Place two cursors that measure the propagation delay of measurements #65.
   Place two cursors that measure the propagation delay of measurements #66.
3) from beginning of measurement #120 till 5 ns after the end of measurement #120.
   Place two cursors that measure the propagation delay of measurements #120.

Save these images using the filenames "waveTAU1.png", "waveTAU2.png" & "waveTAU3.png"